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Capacitive tracer design to mitigate incomplete I-V curves in outdoor tests

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ABSTRACT

The capacitance technique is the most straightforward and low-cost technique to trace the I-V curve of photovoltaic (PV) modules. Nevertheless, the sweep speed and number of samples to measure the I-V curve depend on the device under test (DUT), capacitance size, switching dynamic, lighting conditions, Etc. Therefore, two performance indexes were proposed to evaluate the I-V curve quality. The indexes were estimated from a circuital model considering the transient capacitance charging process as a function of the target irradiance levels and parameters of the DUT and tracer. In this way, a capacitance range is estimated to mitigate the likelihood of measuring incomplete curves in the I_{sc} and V_{oc} regions. Finally, the capacitance sizing design in terms of both indexes for monitoring PV technologies was validated in outdoor tests.

1. Introduction

The performance of Photovoltaic (PV) devices is described by the short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), fill factor (FF), maximum power (P_{max}), voltage and current at the maximum power point (V_{mpp}, I_{mpp}) and efficiency. These parameters are typically estimated from the I-V curve regarding light and temperature conditions (Velilla et al., 2017). In this context, the capacitance technique could be considered the most straightforward and low-cost technique to trace the I-V curve of PV modules. Nevertheless, it is possible to measure incomplete I-V curves and estimate inappropriate parameters concerning the performance because the sweep speed and the number of samples are functions of the device under test (DUT), capacitance value, switching dynamic, lighting conditions, Etc. These issues could be more relevant in outdoors because of the irradiance level changes, increasing the likelihood of measuring incomplete curves, highlighting the importance of measuring proper curves to improve the performance estimation.

The I-V curve is conventionally measured by scanning the device operating points starting at the short-circuit current point (0, I_{sc}), crossing the maximum power point (V_{mpp}, I_{mpp}) and ending at the open-circuit voltage point (V_{oc}, 0). Hence, several I-V tracers have been reported in the literature depending on the sensors and data-acquisition systems (Zhu and Xiao, 2020), which currently demonstrate more capabilities and lower cost. Thus, properties such as flexibility, fidelity, cost, fast-response, modularity, among other parameters, have been considered to evaluate the tracer performance (Duran et al., 2008).

Accordingly, the four-quadrant power supply, DC-DC converters and bidirectional power inverters coupled to DC/DC converters have been employed to trace the I-V curve by facilitating different sweep speeds and scan directions (forward and reverse), allowing testing the devices under dark or light conditions (Morales-Aragonés et al., 2021). On the other hand, resistive and capacitive load tracers have been widely used under light conditions because of the simplicity for measuring the curve regardless of the power dissipation drawbacks. However, the capacitance load or capacitance technique is the most straightforward technique to be implemented in the tracers because the dynamic behavior to scan the curve is inherent to the capacitor charging process. Therefore, the controllability and adaptability of the capacitance technique to scan the device operating points, facilitates for testing PV and arrays (Chen et al., 2018; García-Valverde et al., 2016), enables to design tracers with adaptive sampling period (Chen et al., 2020), tracers for estimation of the parameters of PV devices (Padilla et al., 2022; Velilla et al., 2021, 2019a; Velilla Hernández et al., 2022) or multi-module capacitive tracers for PV systems (Reischauer and Rix, 2019).

The capacitive technique requires large-high-quality capacitors (minor series resistance) to measure a proper I-V curve concerning light conditions. Accordingly, different approaches have been proposed for capacitance sizing. Most of them are based on the “fill factor one” or constant current approximation (Warner and Cox, 1982). Herein, the solar panel is modeled as an ideal current source with a magnitude value of I_{sc}. In this way, the current source charges the capacitor increasing the

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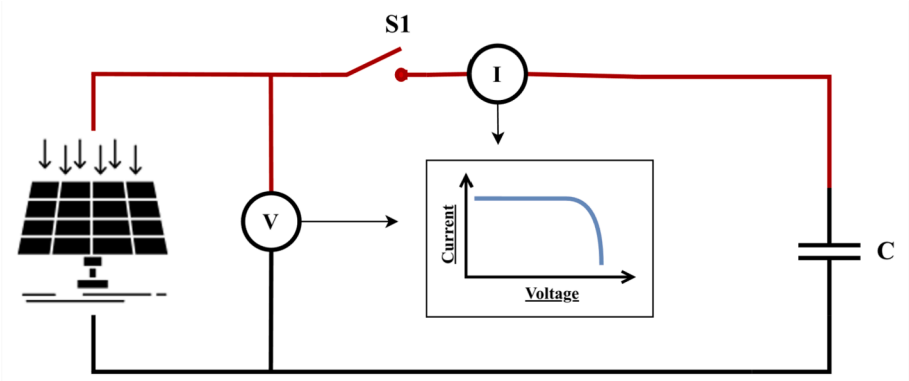

Fig. 1. Scheme of the capacitance technique to trace the I-V curve. The voltage and current signals are measured by the sensors V and I respectively.

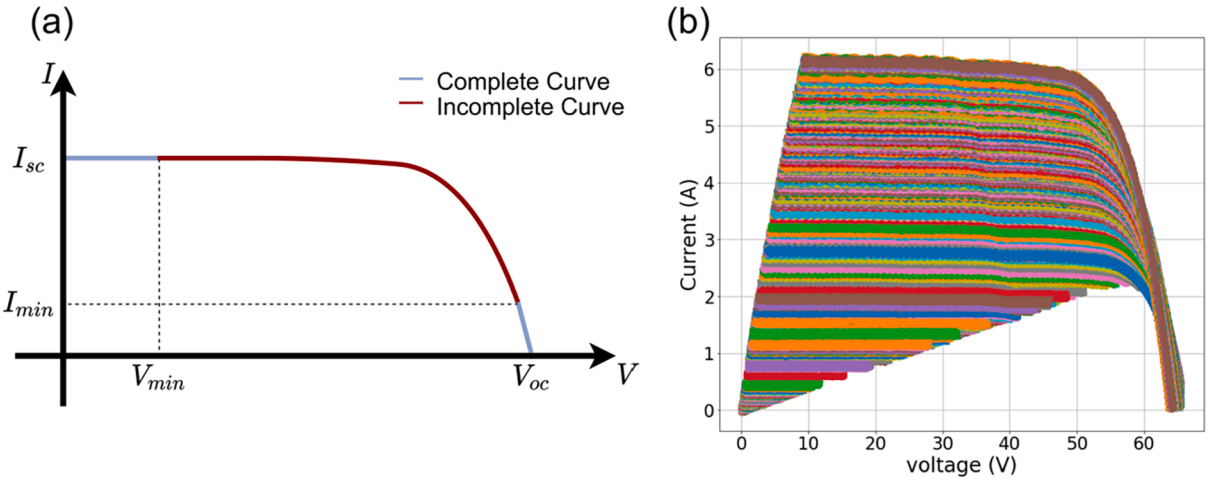

Fig. 2. I-V curve. Panel (a) corresponds to description of complete and incomplete I-V curve. Panel (b) corresponds to recorded I-V curves in outdoor tests to illustrate the regions affected by missing data because of the capacitor sizing and weather conditions.

voltage until the open-circuit voltage (V_{oc}). This charging process is considered by Eq. (1), indicating the relationship between the capacitance size (C), the DUT characteristics (I_{sc} and V_{oc}) and the charging time (t_s).

$$C = t_s \frac{I_{sc}}{V_{oc}} \tag{1}$$

Intended to generalize the fill factor approach modeling, a proportionality factor (k) value of 0.5 was included in Eq. (1) to consider the maximum sweep speeds (Mahmoud, 2006). Moreover, empirical k values ranging between 0.5 and 0.9090 were recommended depending on the application type (module or array of modules) (Sayyad and Nasikkar, 2020). Another approach for sizing the capacitance was proposed using a two-steps model to consider the transient effects in the charging process (Spertino et al., 2015). In this approach, the first step is modeled using a current source of value I_{sc} to produce a constant current charge, obtaining the I-V curve behavior close to I_{sc} value. Then, the second step is modeled as a voltage source (V_{oc}) in series with an equivalent resistance for obtaining the I-V curve behavior close to V_{oc} value. In this case, the charging time can be estimated using the 5RC criterion. Besides, this approach was modified to adjust the sampling period according to the irradiance changes using additional hardware (Chen et al., 2020).

It is worth noting that the approaches are only based on the total time required to charge the capacitor and do not consider specific characteristics of the data-acquisition system as the commutation delay of switches. Therefore, the transient behavior at the beginning of the I-V curve (close to I_{sc}) is not considered. Besides, the capacitance sizing is conventionally calculated considering only one irradiance condition, i.e., Standard Test Conditions (STC) or Nominal Operative Cell Temperature (NOCT) commonly reported in the datasheet of PV modules, thus, the dependence of the DUT parameters with irradiance is not considered. In this context, incomplete I-V curves and uncertainty in the estimated parameters are expected for evaluating PV modules in outdoor tests considering only one capacitance value, because the capacitor charging time also depends on the weather conditions according to Eq. (1). Therefore, this work proposes an alternative approach by proposing two performance indexes to verify the I-V curve completeness and estimate a capacitance range for the tracer concerning the target irradiance levels, panel characteristics, and acquisition system parameters.

2. Capacitance technique

The capacitance technique traces the I-V curve by measuring and recording the current (I) and voltage (V) signals when the switch (S1) is closed to connect the capacitor (C) to the DUT or solar module, Fig. 1. In this case, it is expected to trace complete I-V curves from voltages values approaching zero (correlated to the short-circuit point) to the open-circuit voltage (V_{oc}) during the capacitor charging process, Fig. 2. Nevertheless, it is possible to obtain incomplete curves close to V_{oc} depending on the maximum measurement time or tolerance in the current measurement (uncertainty), or close to I_{sc} depending mainly on the switching behavior (transient effects). Therefore, it highlights the principal role of the switch operation in this technique, which must be

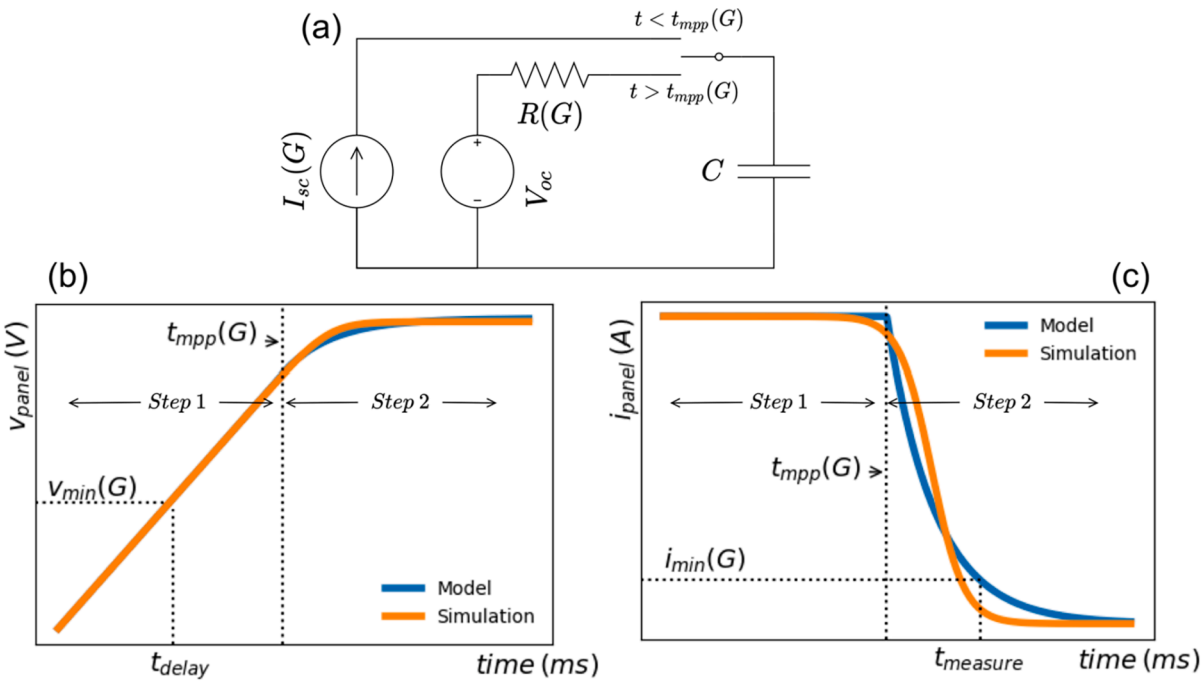

Fig. 3. Transient Charging Circuital Model. Panel (a) corresponds to the equivalent circuit. Panel (b) corresponds to the voltage comparison between the two-Step model (blue line) and one-diode model simulation (orange line). Panel (c) corresponds to the current comparison. The Two Step model is divided in two regions to show the starting capacitance charging process (Step 1) and the exponential current behavior at the end of the capacitance charging process (Step 2). Adapted from (Spertino et al., 2015) and (Chen et al., 2020). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

programmed and synchronized with the data acquisition systems to mitigate the transient effects when the switch is closed and properly record the voltage and current signals during the test.

In a nutshell, a I-V tracer equipment that implements the capacitance technique includes the capacitor, switch, sensors, data acquisition system and control system to perform the tasks. From the hardware point of view, this technique only involves a few elements (switch and capacitor at least), demonstrating the simplicity of performing the I-V curve. From the software point of view, few steps are required to record the data. Moreover, it is possible to include an external resistance (R) to discharge the capacitor and reduce the death time between measurements. In this case, another switch is required and taken into account in the logical process (switches sequence) to trace the I-V curve (Velilla et al., 2019a; Velilla Hernández et al., 2022). Therefore, these advantages allow observing why this technique is a simplest and low-cost technique to trace the I-V.

3. Design methodology for capacitance sizing

This section shows the impact of the capacitance value in the I-V curves to determine the variables and models required for sizing the capacitive tracer concerning light condition and DUT parameters.

3.1. Impact of light conditions on the I-V curve behavior

Fig. 2a shows in a general way the distinction between a complete and incomplete I-V curve. This distinction is highlighted considering the minimum voltage measured (V_{min}) and the minimum current measured (I_{min}), in this case, an appropriate I-V curve is recorded as both parameters tend to zero. Thus, the transient effects due to the switching dynamic and commutation delay involved in the technique could be correlated to the missing or dirty data close to the I_{sc} region. Hence, V_{min} close to zero indicates a quasi-ideal curve and V_{min} close to V_{oc} indicates a poor-quality curve. On the other hand, an insufficient time to fully charge the capacitor or shorter available time for the measurement could be correlated to missing data correlated to the V_{oc} region. Hence, I_{min} close to zero indicates a successful measurement of the V_{oc} while I_{min} close to I_{sc} indicates an incomplete charging process of the capacitor.

Fig. 2b shows the impact of light conditions (G) on both regions (I_{sc} and V_{oc}) of the I-V curve recorded in outdoor tests considering a fixed capacitance value. Here, the behavior close to V_{oc} can be explained regarding Eq. (1), because the DUT parameters (I_{sc} and V_{oc}) depend on weather conditions. Thus, the charging time mainly depends on light conditions (G) producing insufficient time to fully charge the capacitor as the irradiance levels decrease. Nevertheless, this equation does not allow explanation of the behavior close to the I_{sc} region, which is mainly a function of the sweep speed and switching dynamic (I-V tracer specific-parameters), being more evident as G increases (see Supplementary Information Fig. S1).

3.2. Success rates (SR) indexes

In order to evaluate the performance of the I-V curve concerning the missing data, the regions affected by this missing data related to I_{sc} and V_{oc} are described in terms of the parameters shown in Fig. 2a. Herein, it is possible to determine the performance of the recorded I-V curve considering two normalized indexes. The first index called success rate of current (I_{SR}) is related to the I_{sc} region considering the ratio between V_{min} and V_{oc} as shown in Eq. (2). The second index called success rate of voltage (V_{SR}) is related to the V_{oc} region considering the ratio between I_{min} and I_{sc} as shown in Eq. (3). Thus, a proper I-V curve (mitigating missing data) is expected when both indexes are close to 100 %.

$$I_{SR} = 100\left(1 - \frac{V_{min}}{V_{oc}}\right) \tag{2}$$

$$V_{SR} = 100\left(1 - \frac{I_{min}}{I_{sc}}\right) \tag{3}$$

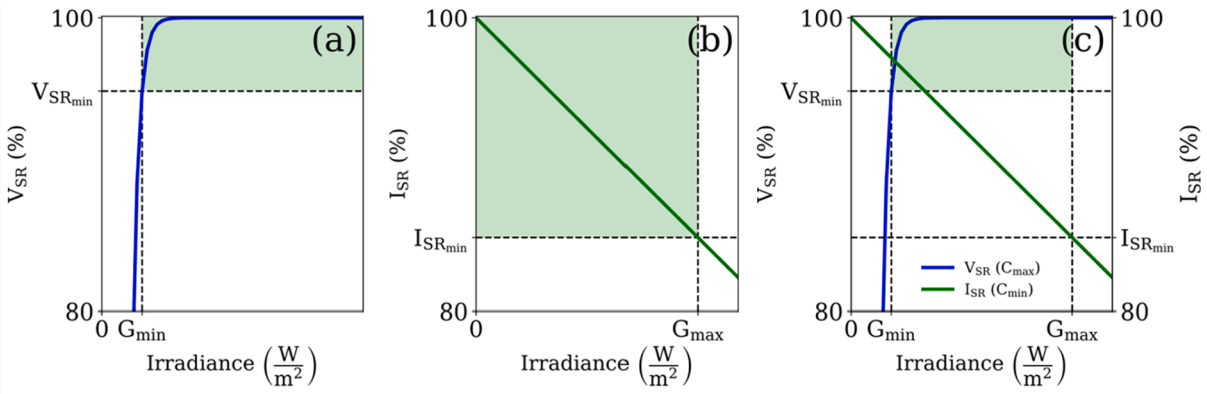

Fig. 4. Definition of target success rates at minimum and maximum irradiances. Panel (a) corresponds to V_{SR}, panel (b) to I_{SR} and panel (c) to the combination of both parameters (V_{SR} and I_{SR}) defined by Eqs. (2) and (3). Green region represents the success area for the parameters. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

It is worth noting that both indexes depend on the irradiance levels (G), as is depicted in Fig. 2b. Accordingly, high irradiance levels are conditions that facilitate the complete capacitor charge, registering the V_{oc} value and improving V_{SR}. Nevertheless, these conditions increase the data loss at the beginning of the capacitor charge (I_{sc} region) because of the switching behavior. In contrast, low irradiance levels are conditions that constrain the capacitor charging process (V_{oc} region). Thus, the V_{oc} value could not be registered. However, under these conditions, current values close to I_{sc} are registered, improving I_{SR}.

3.3. Capacitor charging model

In order to estimate both indexes (I_{SR} and V_{SR}) as a function of G considering the behavior of the DUT and capacitive tracer during the tracing I-V curve process, the two-Step model proposed in the literature (Chen et al., 2020; Spertino et al., 2015) was adapted to consider the dependence of the circuital model with G (Fig. 3a). Therefore, in Step 1, the PV device is assumed as a constant current source charging the capacitor up to a voltage equal to the maximum-power point voltage (V_{mpp}) at the time t_{mpp}, Fig. 3b. In Step 2, the PV device is a constant voltage source in series with a resistor, producing an exponential decay behavior for the current, Fig. 3c.

The circuital model involves the electrical parameters of the DUT such as V_{oc}, I_{sc}, V_{mpp} and I_{mpp}, which are functions of weather conditions (G and temperature). It is possible for design purposes to express I_{sc} and I_{mpp} as a function of irradiance (Eqs. (4) and (5)). Where G is the irradiance in W/m^2, and the subindex STC corresponds to Standard Test Condition (STC). On the other hand, we neglect the effect of G in the DUT voltage (V_{oc} and V_{mpp}).

$$I_{SC}(G) = \frac{Isc_{stc}}{1000} G \tag{4}$$

$$I_{mpp}(G) = \frac{Impp_{stc}}{1000} G \tag{5}$$

Notice that in Step 1 the capacitor voltage increases linearly with time (Fig. 3b). Therefore, I_{sc} at the target irradiance condition (G) is estimated to calculate the time at which the capacitor rises the V_{mpp} value in Step 1 (t_{mpp}), following Eq. (6).

$$t_{mpp}(G) = \frac{CV_{mpp}}{I_{sc}(G)} \tag{6}$$

It is possible in Step 2 to calculate the equivalent resistance R(G) by calculating the inverse of the slope between the maximum power point (V_{mpp}, I_{mpp}) and the open-circuit point (V_{oc}, 0) at the target G, following Eq. (7).

$$R(G) = \frac{V_{oc} - V_{mpp}}{I_{mpp}(G)} \tag{7}$$

Finally, the resulting piecewise expression for the capacitor current in both steps as a function of time (Eq. (8)) is estimated by solving the equivalent circuits taking into account the initial and continuity conditions.

$$i(t) = \begin{cases} I_{sc}(G) & t < t_{mpp}(G) \\ I_{sc}(G) e^{\frac{-(t - t_{mpp}(G))}{RC}} & t > t_{mpp}(G) \end{cases} \tag{8}$$

3.4. Estimation of V_{SR} and I_{SR}

The I_{SR} can be affected by the time delay (t_{delay}) to start the measurement process and charge the capacitor, affecting the I_{sc} region of the I-V curve. Hence, this time must consider the sampling period (t_{sample}) by the acquisition system and commutation delay of the switch (t_{switch}). Thus, t_{delay} can be calculated as follows Eq. (9).

$$t_{delay} = Max\left(t_{sample}, t_{switch}\right) \tag{9}$$

t_{delay} must be smaller than t_{mpp} ($t_{delay} < t_{mpp}$) for guaranteeing a constant charge current in Step 1 (Eq. (8)). Thus, a linear behavior of the capacitor voltage as a function of the time is obtained (Eq. (10)), allowing estimation of the minimum measured voltage (V_{min}) as shown in Eq. (11) (see Fig. 3b), considering the DUT and I-V tracer.

$$V = \frac{I_{sc}(G)}{C} t \tag{10}$$

$$V_{min} = t_{delay} \frac{I_{sc}(G)}{C} = t_{delay} \frac{Isc_{stc} G}{1000C} \tag{11}$$

Finally, I_{SR} (Eq. (12)) is estimated by replacing V_{min} in Eq. (2) to express I_{SR} in terms of G and DUT characteristics related to Step 1, describing the behavior of the I-V curve in the I_{sc} region.

$$I_{SR} = 100\left(1 - \frac{V_{min}}{V_{oc}}\right) = 100\left(1 - \frac{t_{delay} Isc_{stc} G}{1000 C V_{oc}}\right) \tag{12}$$

On the other hand, the V_{oc} region of the I-V curve can be affected by the charging time. Thus, the total acquisition time ($t_{measure}$) can be calculated as the product of the t_{sample} and the maximum number of samples ($n_{samples}$) settled by the acquisition system following Eq. (13).

$$t_{measure} = n_{samples} t_{sample} \tag{13}$$

Accordingly, considering that $t_{measure}$ is greater than t_{mpp}, Eq. (8) related to Step 2 is employed for estimating I_{min} at $t_{measure}$, Eq. (14).

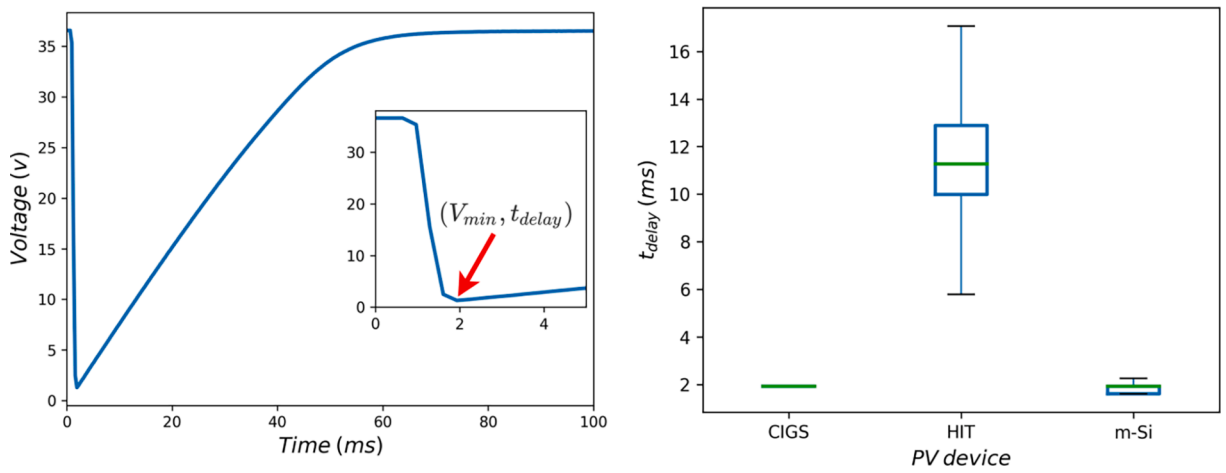

Fig. 5. Switching time (t_{switch}) estimation. Panel (a) corresponds to voltage signal during the I-V curve tracing in outdoor tests. The inset corresponds to the initial behavior of voltage related to the switching process. Panel (b) corresponds to estimated t_{switch} distribution in a form of boxplot considering one year of outdoor testing.

$$I_{min} = I_{sc}(G)e^{\frac{-\left(t_{measure} - t_{mpp}(G)\right)}{R(G)C}} \tag{14}$$

Then, the V_{SR} (Eq. (15)) is calculated by replacing I_{min} in Eq. (3) to express the index in terms of G and corresponding times of Step 2 (see Fig. 3c), describing the I-V curve behavior in the V_{oc} region.

$$V_{SR}(G) = 100\left(1 - \frac{I_{min}(G)}{I_{sc}(G)}\right) = 100\left(1 - e^{\frac{-\left(t_{measure} - t_{mpp}(G)\right)}{R(G)C}}\right) \tag{15}$$

Notice that for t_{mpp} greater than $t_{measure}$, a negative value for V_{SR} is estimated. In those cases, the I-V curve tracer is not able to register the V_{mpp} value.

3.5. Capacitance sizing design

Once I_{SR} and V_{SR} are described in terms of G and the parameters related to the I-V curve tracer, DUT and acquisition system (Eqs. (12) and (15) respectively), it is possible to define acceptable or target values for the success rates to design an appropriate capacitor size. Therefore, defining the SR targets values as V_{SRmin} (Fig. 4a) and I_{SRmin} (Fig. 4b), the operative irradiance range ($G_{min} < G < G_{max}$) for the tracer is constrained (Fig. 4c). In this regard, the capacitances correlated to the I_{sc} and V_{oc} regions could be estimated from Eqs. (12) and (15) respectively. Thus, the maximum capacitance (C_{max}) value is estimated from V_{SR} considering the minimum irradiance (G_{min}) following Eq. (16). The minimum capacitance (C_{min}) value is estimated from I_{SR} considering the maximum irradiance (G_{max}), following Eq. (17). Therefore, both capacitances limit the required operative capacitance range ($C_{min} < C < C_{max}$) for the tracer to guarantee the I-V curves quality concerning the operative irradiance range defined by the target conditions.

It is worth noting that it is also possible to tune-up the design by selecting different target indexes for current and voltage based on the required application or define the irradiance range of interest to estimate the SR values (I_{SR} and V_{SR}) and calculate the capacitor size. Finally, it is highlighted that the proposed design process for sizing the capacitance was validated by the equations involved in two-Step model and by simulation using for instance the one-diode model to include the transient behavior during the capacitance charging process, as is shown in Supporting Information section S2.

$$C_{max} = \frac{t_{measure}}{V_{mpp}/I_{sc}(G_{min}) - R(Gmin)ln(1 - V_{SRmin}/100)} \tag{16}$$

$$C_{min} = \frac{t_{delay} Isc_{stc} G_{max}}{1000\left(1 - \frac{I_{SRmin}}{100}\right)Voc} \tag{17}$$

4. Results

This section shows the validation of the proposed design methodology for selecting the capacitor values to improve the quality of recording I-V curve in outdoor tests. Therefore, three modules of different technologies (Table S1) were monitored in natural sunlight without a tracker (Table S2) (6°15′ 38″N 75°34′ 05″W, facing south at a fixed tilt angle of 13°) by adjusting the corresponding capacitance of the I-V tracers (Table S3). The I-V curves and environmental variables (irradiance, device temperature and ambient temperature) were recorded every minute during light-hours, as was performed in previous work (Padilla et al., 2022; Velilla et al., 2021, 2019a, 2019b). In this way, the outdoor data allowed estimating the t_{delay} of the evaluated Panasonic VBHN330SJ47 (HIT), Miasolé FLEX–02 120 N (CIGS) and Znshine solar ZX55(17.8)M (m-Si) modules (Table S1). These values were used as input in the proposed modeling for estimating the capacitance range of the tracer considering the target indexes V_{SR} and I_{SR} and corresponding irradiance range.

4.1. Time delay estimation

Fig. 5a shows in a general way the voltage signal during the capacitor charging process for tracing the I-V curve. The time delay (t_{delay}) corresponds to the maximum time between t_{switch} and sampling period (t_{sample}) according to Eq. (9). It corresponds to the time to reach the minimum voltage (V_{min}) once the switch is closed, changing the voltage from V_{oc} to V_{min} (transitory state), as is shown in the inset. Therefore, the recorded data during the t_{delay} are not considered in the I-V curve (missing data), affecting the I_{sc} region as was shown in Fig. 2b.

In this regard, t_{delay} was estimated as the required time to register the minimum voltage (V_{min}) in outdoor tests for the evaluated PV devices, considering that t_{switch} is greater than t_{sample} (See Table S2 and S4). Fig. 5b shows the estimated t_{delay} in the form of a boxplot, observing that median values of t_{delay} approach 11.27 ms for HIT and 1.932 ms for other modules. Besides, the data distribution suggested that t_{delay} is almost constant during the outdoor tests for CIGS and m-Si modules, indicating that t_{delay} mainly depends on the switching process or commutation delay (t_{switch}) according to Eq. (9). On the contrary, the estimated t_{delay} distribution for HIT module indicates that t_{delay} changed during the tests, which could be explained because this switch can operate at high voltages (up to 250 V). Nevertheless, results allowed validation of t_{delay} because they are in the range reported by the manufacturers, concerning the typical and maximum values for t_{delay} (see Supporting Information section S.3.1). Finally, it is worth noting that

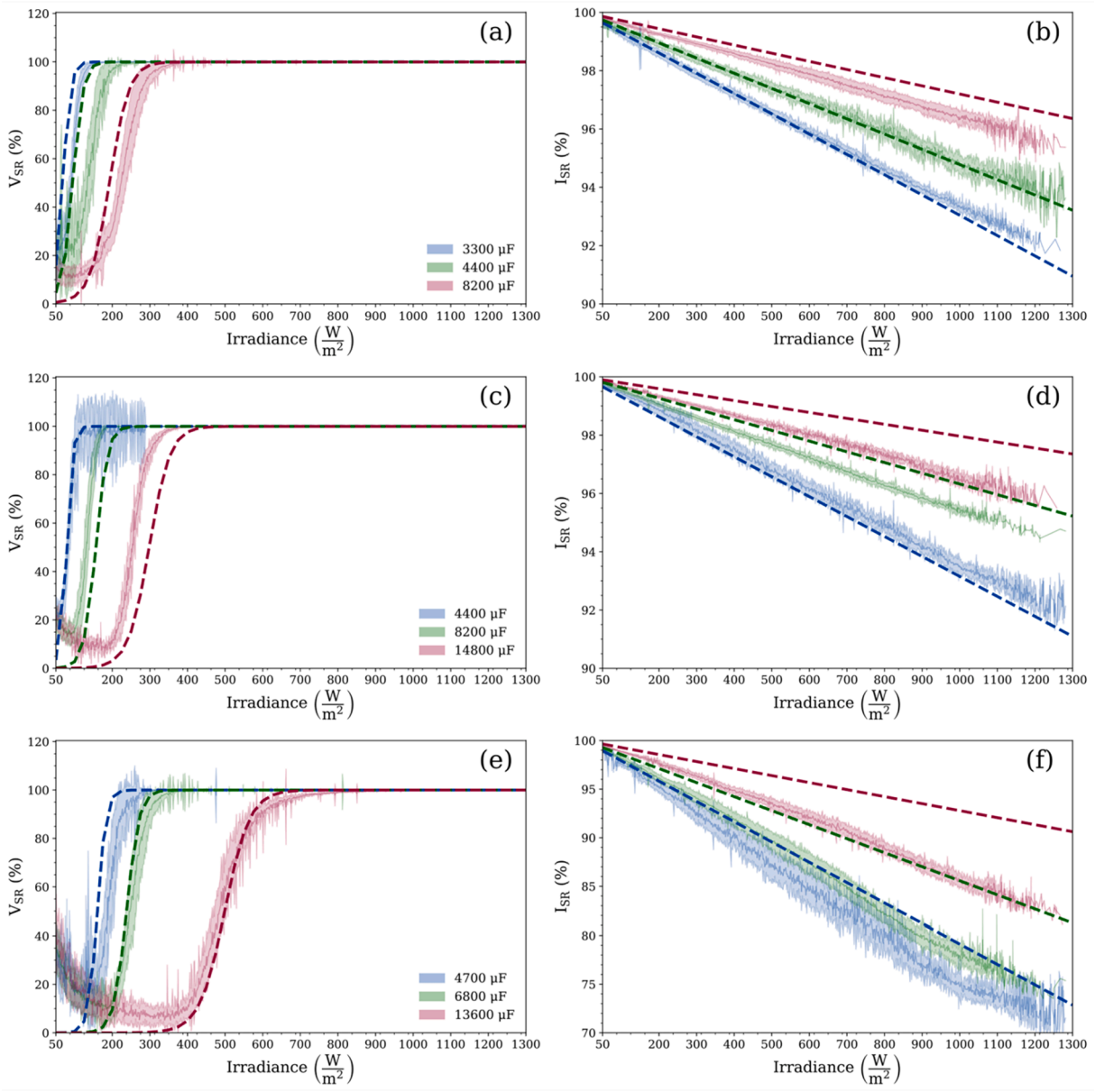

Fig. 6. Impact of irradiance and capacitance on V_{SR} and I_{SR}. Panels (a-b) correspond to CIGS - Miasolé module, (c-d) to m-Si – Znshine module, and (e-f) to HIT - Panasonic module. The dashed lines correspond to the results following the proposed capacitor sizing design, Eq. (15) for V_{SR} and Eq. (12) for I_{SR}. The contour is a visual guide of the corresponding recorded outdoor data, considering one standard deviation with respect to the median values. The insets show the installed capacitance in the tracer.

t_{delay} must be estimated by testing because it is required to mitigate the missing data in the I_{sc} region, according to Eq. (12).

4.2. Capacitance size impact on performance indexes

Different capacitance values were installed in the tracers during the outdoor tests to compare the outdoor performance of I-V curves concerning the proposed capacitance sizing design (proposed modeling). Thus, V_{SR} and I_{SR} were estimated for the DUTs considering the outdoor records corresponding to the I-V curves. In the case of the proposed modeling, V_{SR} and I_{SR} were estimated for the DUTs as a function of G following Eqs. (12) and (15), considering the estimated t_{delay} median values (Fig. 5b), an acquisition time ($t_{measure}$) of 322 ms, DUT parameters (see Table S2), and corresponding installed capacitance value in the tracers.

Fig. 6 shows, in a general way, the agreement between the outdoor tests and proposed modeling. Results allowed observing the impact of irradiance and capacitance on V_{SR} and I_{SR}, characterized by a sigmoidal and linear behavior concerning irradiance, respectively. These behaviors suggest an irradiance range to guarantee the quality of I-V curves concerning the capacitance value, as shown in Fig. 4. V_{SR} indicates a value of G (G_{min}) for improving the index (100 %). Thus, in order to reduce the likelihood of missing data in the I_{sc} region, lower C values must be considered to improve the index by reducing G_{min}. On the contrary, to reduce the likelihood of missing data in the V_{oc} region, greater C values must be considered to improve I_{SR} by increasing the irradiance range (G_{max}). Besides, Fig. 6 demonstrates the dependence of V_{SR} and I_{SR} on the DUT parameters (P_{max}, V_{oc} and I_{sc}), highlighting the principal role of the DUT parameters in the capacitance sizing design.

It is worth noting that differences between the outdoor and proposed modeling can be explained mainly because of the tolerance of the electrolytic capacitors (±20 % at 120 Hz/+20 °C)[1]. This tolerance could

Table 1
Capacitance range estimation according to target conditions, DUT and I-V curve tracer characteristics.

DUT	I-V tracer		Estimated indexes		Capacitance values	
	t_{delay} (ms)	$t_{measure}$ (ms)	V_{SRmin} (%)	I_{SRmin} (%)	C_{min} (uF)	C_{max} (uF)
CIGS	1.932	322	93	93	3280	5420
m-Si	1.932				4140	7030
HIT	11.27				14,020	4290
				75	3930	

affect the estimation of V_{SR} and I_{SR}, as was shown in Fig. S5 of supporting information, considering the lower (dashed lines) and upper (dotted lines) capacitance limits.

4.3. Capacitor sizing design

Eqs. (16) and (17) were followed for capacitance sizing estimation of tracers considering the DUTs parameters and estimated t_{delay} (Fig. 5b). Table 1 shows the calculated values to guarantee the quality of I-V curve in the target irradiance range between 200 and 1000 W/m^2 ($G_{min} < G < G_{max}$).

Notice that HIT calculations were repeated twice because of the long t_{delay} of the corresponding I-V tracer (the switch was slower because of the high V_{oc} constraints). Thus, it was impossible to find a valid capacitance range for target values of 93 % for V_{SRmin} and I_{SRmin}, therefore I_{SRmin} was settled to 93 %. It emphasizes the relevance of using fast commutation switches in the design of capacitive I-V curve tracers in order to guarantee good performance in the I_{sc} region of the curves.

Fig. 7 shows the I-V curve performance regarding V_{SR} and I_{SR} indexes in outdoor tests considering the estimated capacitance shown in Table 1.

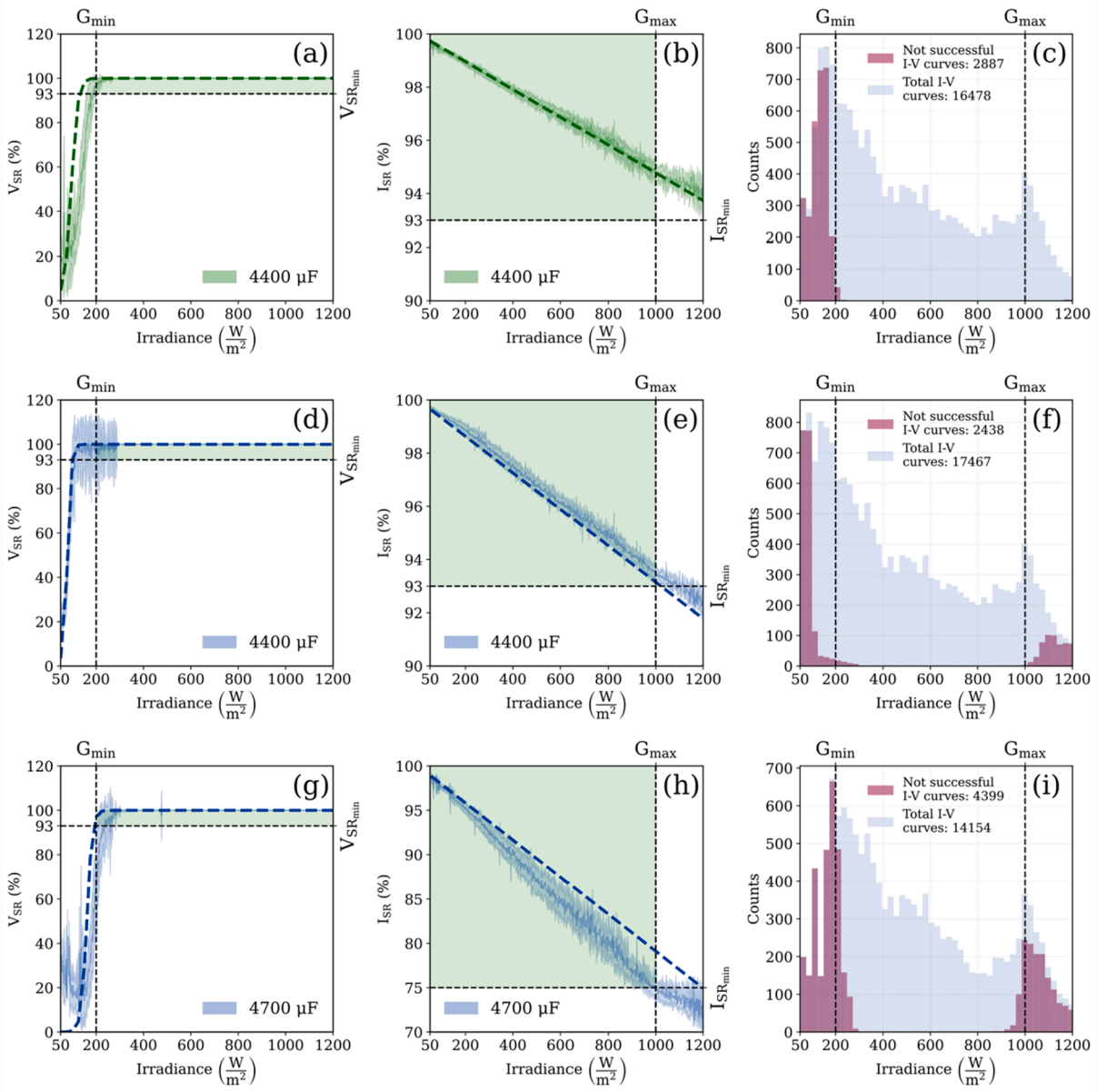

Fig. 7. Capacitor Sizing Verification. Panels (a-c) correspond to CIGS - Miasolé module, (d-f) to m-Si - Znshine and panels (g-i) to HIT - Panasonic module. In panels (a, b, d, e, g, h) the dashed lines correspond to the proposed equations, Eq. (15) for V_{SR} and Eq. (12) for I_{SR} using the estimated t_{delay} corresponding to each DUT (Fig. 5b), the contour area corresponds to real data standard deviation with respect to median values and the green area represents the success area. The insets show the installed capacitance in the tracer. The colors of V_{SR} and I_{SR} plots are correlated with the colors shown in Fig. 6. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

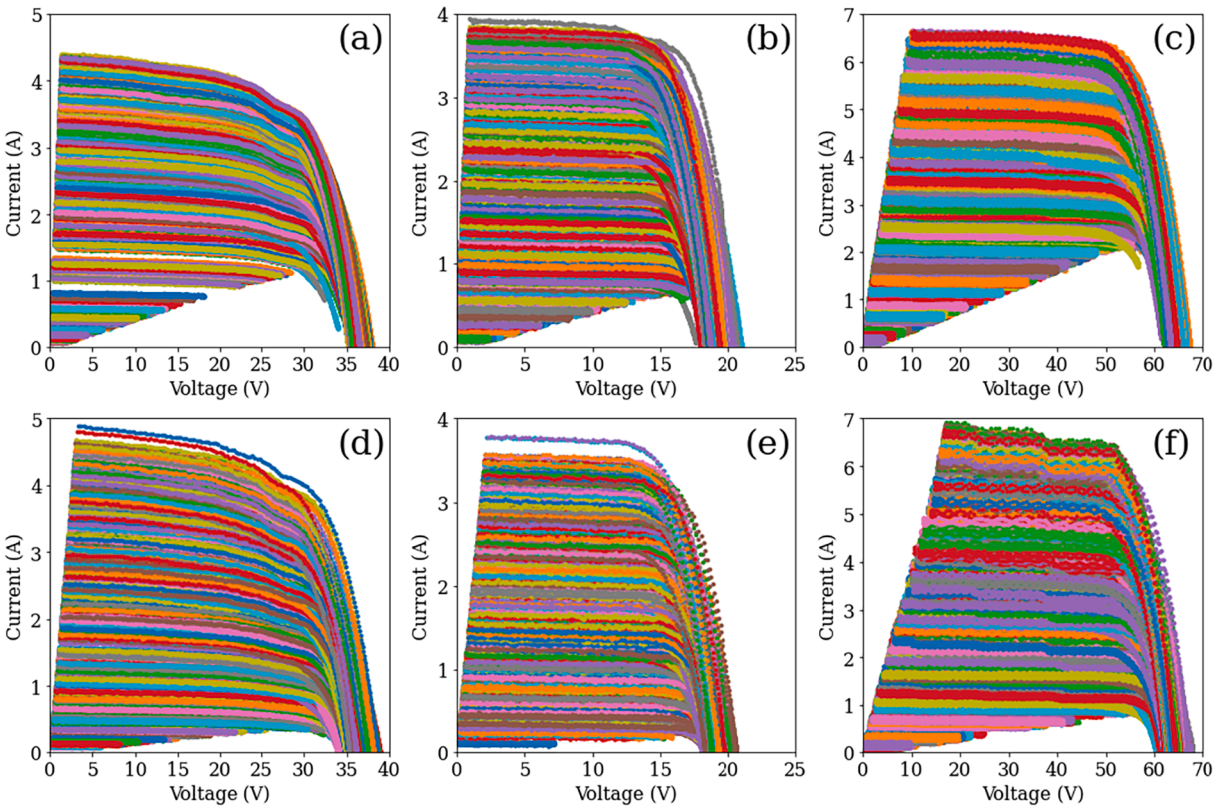

Fig. 8. Impact of capacitance sizing in the I-V curves in outdoor conditions. Panels (a-c) correspond to I-V curves of modules using larger capacitor values. Panels (d-f) correspond to I-V curves of modules using the estimated capacitors. Panels (a and d) correspond to CIGS - Miasolé module, (b and e) to m-Si - Znshine and (c and f) to HIT - Panasonic module. Panels (a and b) correspond to capacitor value of 14,800 μF, panel (d and e) to 4400 μF, panel (c) 13,600 μF and panel (f) 4700 μF.

Accordingly, capacitors of 4400 μF were installed in the tracer for monitoring the CIGS and m-Si modules. It is worth noting that for the HIT module it was necessary to install in the tracer a capacitor of 4700 μF (out of the calculated range) because of the available commercial capacitors. In this regard, the behavior of V_{SR} and I_{SR} indexes (Fig. 7a, b, d, e, g, h) allows validating the agreement between the capacitor sizing design (Eq. (15) for V_{SR} and Eq. (12) for I_{SR}) and outdoor tests considering the target values for G (G_{min} and G_{max}), because the defined minimum target values for V_{SRmin} and I_{SRmin} (Table 1) were properly reached in the target irradiance ranges. This fact can be observed in a better way considering the indexes distribution regarding the irradiance in the form of histograms (Fig. 7c, f, i), indicating that most success measurements are in the target irradiance range. Therefore, the selected capacitance values effectively guarantee the quality of the I-V curve according to the indexes for the target values in outdoor conditions.

Fig. 8 shows the impact of the capacitor values in the I-V curves behavior in outdoor tests by comparing larger capacitor values (Fig. 8a, b and c) regarding the estimated capacitor values shown in Table 1 (Fig. 8d, e, and f). These results highlight the improvement of the proposed design methodology for capacitor sizing because it allows mitigating incomplete I-V curves, observing a noticed improvement in the V_{oc} regions (without significantly affecting the I_{sc} region). This fact indicates that the capacitor charging time was improved concerning the target irradiance range. In the case of HIT - Panasonic module (Fig. 8c, f), although is also observed the improving in the V_{oc} regions, it is worth noting that due to the t_{delay} restriction, the I_{sc} region was affected.

5. Conclusions

In this paper, a capacitor sizing design for I-V tracing in outdoor conditions was proposed considering two performance indexes (V_{SR} and I_{SR}). The indexes were correlated with the performance and quality of I-V curves measurements in the I_{sc} and V_{oc} regions. The indexes were estimated from a circuital model to consider the capacitor charging process dependence with irradiance considering the DUT and I-V curve tracer characteristics. In this way, by defining the target values for both indexes, an irradiance range is limited allowing estimation of an appropriate capacitance range for guaranteeing the constraints regarding the completeness of the I-V curve in the I_{sc} and V_{oc} regions.

The proposed capacitor sizing design was tested and validated by simulation and extensive outdoor measurements using three PV devices of different technologies (CIGS, m-Si and HIT). Results demonstrate that the design considerations and simplifications from the circuital model are appropriated, allowing to tune-up the design for different measurement scenarios, mitigating the incomplete I-V curves in outdoor tests.

Finally, it was shown the relevance of t_{delay} (due to switch commutation) in the design process, which plays a principal role at the beginning of the capacitor charging process affecting the I_{sc} region. Indicating that fast commutation devices must be considered for I-V tracers' development. In this regard, it is worth noting that the switching delay time can be influenced by different factors (temperature, electrical operation point, parasitic elements, etc.). Thus, for an appropriate I-V tracer design, it is required to perform an on-site characterization of t_{delay}, as was shown in this work. However, the maximum values reported by manufacturers in the datasheet can be used in the design as a first approximation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solener.2022.08.021.

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