

Comparison of Electrical Fault Response In Z-source Circuit Breaker Topologies For D.C. Microgrid Applications

by

Bayron Perea Mena

A thesis presented to the University of Antioquia in fulfillment of the thesis requirement for the degree of Master of Applied Science: Magister en Ingeniería

Director

Jaime Alejandro Valencia Velásquez, Doctor (PhD) en Ingeniería Eléctrica

Codirector

Nicolás Muñoz Galeano, Doctor (PhD) en Ingeniería Electrónica

Universidad de Antioquia Facultad de Ingeniería Maestría en Ingeniería Medellín, Antioquia, Colombia 2023

Cita		Perea Mena [1]
	[1]	B. Perea Mena, "Comparison of Electrical Fault Response In Z-source Circuit
Referencia		Breaker Topologies For D.C. Microgrid Applications", Tesis de maestría,
Estilo IEEE (2020)		Maestría en Ingeniería, Universidad de Antioquia, Medellín, Antioquia, Colombia, 2023.

© creative commons

Maestría en Ingeniería, Cohorte XXXI.

Grupo de Investigación Manejo Eficiente de la Energía (GIMEL).

Centro de Investigación Ambientales y de Ingeniería (CIA).



Biblioteca Carlos Gaviria Díaz

Repositorio Institucional: http://bibliotecadigital.udea.edu.co

Universidad de Antioquia - www.udea.edu.co

El contenido de esta obra corresponde al derecho de expresión de los autores y no compromete el pensamiento institucional de la Universidad de Antioquia ni desata su responsabilidad frente a terceros. Los autores asumen la responsabilidad por los derechos de autor y conexos.

Abstract

With the increasing prominence of DC microgrids in recent years, addressing the challenges faced by DC microgrid protection systems, particularly in relation to the absence of current zero-crossing and arc mitigation during circuit switching, has become crucial. In this regard, Z-source circuit breakers and their modifications have emerged as promising solutions for medium-voltage DC microgrid protection. These devices offer natural commutation, simple control, low losses, and high fault-clearing speed. This project select and compare different Zsource topologies and their modifications for both unidirectional and bidirectional operation, using comparable performance parameters for medium-voltage microgrid applications. The topologies were simulated using the OpenModelica software to evaluate their functionality and performance.

keywords: Fault, Circuit Breaker, Topologies, Z-source, DC microgrid

Acknowledgements

My beloved children Santiago Perea Valencia and Samanta Perea Valencia, I greatly appreciate your patience during the completion of my thesis project. Their support were fundamental to achieve the objectives and goals established.

I would also like to extend my gratitude to my parents Mirza Mena de Perea and Plutarco Perea Pandales for their unconditional support and encouragement throughout this process.

I would also like to thank professors Jaime Alejandro Valencia Velásquez and Nicolás Muñoz Galeano for their constant support and valuable teachings that allowed me to advance in this project and achieve satisfactory results.

To professors Jesús María López Lezama and Juan Bernardo Cano Quintero, I am grateful for their guidance and suggestions that helped me to improve my project.

Thanks to my Heavenly Father, the God of the land of the living, for this opportunity.

Finally, I would like to emphasize that few people have the opportunity to learn as much as I did during this project. I am very grateful and proud to have had the support of such valuable people in my academic and personal life. Thank you very much.

"Bayron Perea Mena"

Contents

1	Intr	roduction	1
	1.1	Problem statement	3
	1.2	Research question	3
	1.3	Project Objectives	4
		1.3.1 General Objective	4
		1.3.2 Specific Objectives	4
		1.3.3 Methodology	4
	1.4	Structure of chapters	6
2	Stat	te of the art fault current protection DC microgrids	7
	2.1	Introduction	7
	2.2	DC Microgrid Faults	7
	2.3	DC Circuit Breakers	9
		2.3.1 Fuses	9
		2.3.2 Mechanical Circuit Breakers	10
		2.3.3 Solid-State Circuit Breakers	12
		2.3.4 Hybrid Circuit Breakers	16
	2.4	DC CB Evolution	17
3	Z-so	ource topologies and their modifications	21
	3.1	Introduction	21
	3.2	Mono-directional topologies	21
		3.2.1 Topologies without magnetic couplings	21
		3.2.2 Topologies with magnetic couplings	28
	3.3	Bi-directional topologies	36
		3.3.1 Topologies without magnetic couplings	36
		3.3.2 Topologies with magnetic couplings	11
4	Res	sults obtained from the Z-source topologies simulations 5	51
	4.1	Introduction	51
	4.2	Mono-directional topologies results	52
			52
		4.2.2 Result Parallel Z-source topology	56
		4.2.3 Result Series Z-source topology	59
			52

7	Abb	oreviat	ions	119
6	Cor	clusio	ns	117
	5.4	Future	e challenges	116
	5.3		sion	
	5.2	-	arative analysis	
	5.1	Introd	uction	111
5	Cor	nparat	ive analysis, discussion and future challenges	111
		4.3.8	Result simulation of Bi-directional topology based on T-source	107
		4.3.7	Result simulation of Bi-directional topology based on T-source	
		4.3.6	Result Bi-directional topology based on T-source	101
		4.3.5	Result Bi-directional topology based on T-source	97
		4.3.4	Result Bi-directional topology based on T-source	
		4.3.3	Result Bi-directional topology based on the series Z-source	
		4.3.2	Result Bi-directional topology based on the series Z-source	
		4.3.1	Result Bi-directional topology based on the classic Z-source	
	4.3		s Bi-directional topologies	
		4.2.11	Result O-Zsource topology	
		4.2.10	Result τ -source topology	
		4.2.9	Result T-Source topology	
		4.2.0	duced capacitance	
		4.2.7	Result Series Z-source using magnetic coupling topology Result Classic connected Z-source using magnetic coupling with re-	
		$4.2.6 \\ 4.2.7$	Result Classic Z-source using magnetic coupling topology	
		4.9.C	ogy	
		4.2.5	Result Series connected Z-source with response to load variations topol-	
		105		

List of Figures

2.1	Conceptual diagram of a DCMG
2.2	Types of faults: (a) line–line fault, (b) line–ground fault
2.3	(a) MCB with passive resonance, (b) MCB with active resonance [7] 11
2.4	General circuit of an ACZ-VCB
2.5	Conceptual diagram of a typical SSCB
2.6	Galvanic isolation circuit for SSCBs
2.7	Diagram of conventional HCBs [7]
2.8	Timeline evolution of DC CBs before the definition of DCMGs
2.9	Timeline evolution of DC CBs after the definition of DCMGs 19
3.1	Classic Z-source circuit breaker [13]
3.2	Classic Z-source commutation states, adapted from [13]
3.3	Parallel Z-source topology [13] 25
3.4	Series connected Z-source[10]
3.5	Alternative classical Z-source topology [35]
3.6	Series connected Z-source with response to load variations [53]
3.7	Classic Z-source using magnetic coupling [43]
3.8	Series Z-source using magnetic coupling [43]
3.9	Classic connected Z-source using magnetic coupling with reduced capacitance[53] 32
3.10	T-source topology $[53]$
3.11	τ -source topology [92]
3.12	
3.13	Bi-directional topology based on the classic Z-source [72]
3.14	Bi-directional topology based on the series Z-source [67]
	Bi-directional topology based on the series Z-source [32]
3.16	Bi-directional topology based on T-source [72]
3.17	Bi-directional topology based on T-source [87]
3.18	Bi-directional topology based on T-source [78]
3.19	Bi-directional topology based on T-source [71]
3.20	Bi-directional topology based on T-source [71]
4.1	OpenModelica simulation of classic Z-source topology
4.2	Classic Z-source behavior i_f , i_{SCR} , v_{scr} , v_0
4.3	Classic Z-source behavior i_c , i_L , v_c , v_L , i_{RL} , i_s
4.4	Classic Z-source behavior i_f , i_c
4.5	
4.0	OpenModelica simulation of parallel Z-source topology

4.6	Parallel Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0	57
4.7	Parallel Z-source behavior i_C , i_L , v_C , v_L , i_{RL} , i_s	58
4.8	OpenModelica simulation of series Z-source topology	59
4.9	Series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0	60
4.10	Series Z-source behavior i_C , i_L , v_C , v_L , i_{RL} , i_s	61
4.11	OpenModelica simulation of Alternative Z-source topology	62
4.12	Alternative Z-source topology behavior i_f , i_{SCR1} , i_{SCR2} , V_{SCR1} , V_{SCR2} , v_0	63
	Alternative Z-source topology behavior i_{C1} , i_{L1} , v_{C1} , v_{L1} , v_{C1} , i_{Ls}	64
4.14	OpenModelica Simulation Series connected Z-source with response to load variations	65
4.15	Series connected Z-source with response to load variations behavior i_{SCR}	66
	OpenModelica Simulation Classic Z-source using magnetic coupling topology	67
	OpenModelica Simulation Classic Z-source using magnetic coupling topology	co
4 1 0	behavior i_f , i_{SCR} , v_{SCR} , v_0	68
4.18	Classic Z-source using magnetic coupling topology behavior i_C , i_L , v_C , v_L ,	00
4 10	i_{RL}, i_s	69 70
	OpenModelica simulation of Series Z-source using magnetic coupling topology	70
	Series Z-source using magnetic coupling topology behavior i_f , i_{SCR} , v_{SCR} , v_0	71
4.21	Series Z-source using magnetic coupling topology behavior i_C , i_L , v_C , v_L , i_{RL} ,	
4.00	i_s	72
4.22	Z-source in series with magnetic coupling topology does not include an induc-	70
4.00	tance at the source L_s behavior i_c, i_L, v_c, v_L	73
4.23	OpenModelica simulation of Classic connected Z-source using magnetic cou-	- 4
4.04	pling with reduced capacitance topology	74
4.24	Classic connected Z-source using magnetic coupling with reduced capacitance	
	behavior i_f , i_{SCR} , v_{SCR} , v_0	75
4.25	Classic connected Z-source using magnetic coupling with reduced capacitance	-
1.00	behavior $i_c, i_L, v_c, v_L, i_{RL}, i_s$	76
	OpenModelica Simulation of T-Source topology	77
4.27	T-Source topology behavior i_f , i_{SCR} , v_{SCR} , v_0	78
	T-Source topology behavior i_c , i_L , v_c , v_L , i_{RL} , i_s	79
	OpenModelica simulation of τ -source topology	80
	τ -Source topology behavior i_f , i_{SCR} , v_{SCR} , v_0	81
	τ -source topology behavior i_c , i_{L1} , i_{L2} , v_c , v_L , v_{L1} , v_{L2} , i_{RL} , i_s	82
4.32	τ -Source topology with inductor values optimized for lower i_C behavior i_c , i_{L1} ,	
	$i_{L2}, v_c, v_L, v_{L1}, v_{L2} \ldots \ldots$	83
	OpenModelica simulation of O-Zsource topology	84
	O-Zsource topology behavior i_f , i_{SCR} , v_{SCR} , v_0	85
	O-Zsource topology behavior i_c , i_{L1} , i_{L2} v_c , v_{L2} , i_{RL} , i_s	86
4.36	OpenModelica simulation of Bi-directional topology based on the classic Z-	
	source	87
	Bi-directional topology based on the classic Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0	88
4.38	Bi-directional topology based on the classic Z-source behavior i_c , i_L , v_c , v_L ,	
	i_{RL}, i_s	89
4.39	OpenModelica simulation of Bi-directional topology based on the series Z-	
	source	90

4.40	Bi-directional topology based on the series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0	91
	Bi-directional topology based on the series Z-source behavior i_c , i_L , v_c , v_L ,	
	i_{RL},i_{Ls}	92
4.42	OpenModelica simulation of Bi-directional topology based on the series Z-	
	source	93
4.43	Bi-directional topology based on the series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0	94
4.44	OpenModelica simulation of Bi-directional topology based on T-source behav-	
	ior i_f , i_{SCR} , v_{SCR} , v_0	95
4.45	Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0	96
4.46	Bi-directional topology based on T-source behavior i_c , i_{L2} , v_c , v_{L1} , i_{RL} , i_s .	97
4.47	OpenModelica simulation of Bi-directional topology based on T-source	98
	Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0	99
4.49	Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{RL} , i_s	100
4.50	OpenModelica simulation Bi-directional topology based on T-source	101
4.51	Result Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0	102
4.52	Result Bi-directional topology based on T-source behavior i_c , i_{L1} , i_{L2} , v_c , v_{L1} ,	
	i_{RL}, i_s	103
	1 00	104
	\mathbf{j}	105
	Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{SCR2} , i_{RL} , i_s	106
	1 1 00	107
	$\mathbf{j} \in \mathcal{S} \cup $	108
4.58	Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{SCR2} , i_{RL} , i_s .	109

List of Tables

5.1	Table with Descriptions and Abbreviations	112
5.2	Comparative table of mono-directional topologies	113
5.3	Comparative table of mono-directional topologies	113
5.4	Comparative table of bi-directional topologies	114

Chapter 1

Introduction

Topics related to DCMGs have achieved popularity in recent years, due to the advantages that these present compared to their counterparts, the so called alternating current microgrids (ACMGs). Some of the advantages of DCMGs include higher efficiency, greater expandability, greater stability, easier control, greater reliability, greater compatibility with renewable energy sources, and fewer conversion steps [61, 48, 20]. However, implementation of DCMGs involves new technical challenges to reach their full potential; among them, the implementation of a suitable protection of the system [5, 36]. Moreover, it has been highlighted that there are currently no standards or guidelines for DCMG implementation [89, 38, 23, 73, 88, 1].

DCMGs are projected as the stage for modern distribution systems due to the proliferation of distributed generation (DG) [8, 51]. DCMGs can be defined as a group of loads and DC sources that function as a single controllable system, providing energy to its local and clearly defined area [20, 51]. DCMGs are composed of sources that are driven by power electronics devices. These devices, under certain operative conditions, may handle currents between two and three times the nominal current for at least tens of microseconds [75, 74], while conventional AC sources can sustain a fault current greater than 20 times their nominal current for hundreds of milliseconds [17]; in consequence, the protective devices used for ACMGs do not fulfill the minimal requirements for DCMGs. The proliferation of DCMGs is an important step in making the future power system load-adaptive, an important requirement for DG. Nonetheless, conventional MCBs for DC protection struggle to extinguish the arc generated when interrupting the fault current, and they also feature relatively slow tripping times, which represents a potential risk for sources and loads [38, 36].

The design criteria for electrical fault-protection circuit breakers in DCMGs must consider the following characteristics: low power loss, reliability, speed, continuity, economy, and simplicity [61, 23, 55]. Regarding microgrid protection, three aspects are addressed: protective circuit-breaker circuits, protection system design, grounding and ground fault isolation [38]. Regarding microgrid fault protection circuits, the most common protections are fuses, MCBs, SSCBs, and HCBs [38]. Circuit breakers' evolution for DCMGs has basically consisted of fuses, MCBs, SSCBs, and HCBs.

Fuses are divided into two types: fast-acting fuses and time-delay fuses. Fast-acting fuses are used to protect the output of converters and are widely used in stationary battery protection [4, 21]. Time-delay fuses are used for high-frequency current peaks that occur when energizing certain loads or when starting motors. The selection of a fuse for an ACMG

requires a response time between 10–100 ms to correctly operate and interrupt the fault; however, DCMGs require a maximum of 0.5 ms [4]. Although the fuse is an inexpensive protection device with very simple construction characteristics, it has the disadvantage of having to be replaced after each fault, and does not have the possibility of discriminating between a transient or a permanent fault.

MCBs are devices that use mechanical parts to interrupt the flow of current in the event of a fault. The current interruption process is always accompanied by an electric arc at the moment of interruption. To mitigate the impact of the arc, passive and active current circuits have been proposed, in which a resonant LC series circuit is used for creating a zero-crossing that extinguishes the arc [2]. The main advantages of mechanical switches consist of having low losses and low investment costs; however, the fault clearance time is between 30 and 100 ms, which is too high for DCMG requirements.

SSCBs constitute an alternative to MCBs, since they do not have mechanical moving parts to operate. Additionally, the operation of SSCBs is performed by semiconductor devices. In general terms, SSCBs have the following characteristics: fast operation, arc-free, soundless, long operation useful life, and reliability. SSCBs are used for a variety of applications [17]. Different types of silicon semiconductor devices are used for the SSCB gate-turnoff thyristor (GTO), the silicon insulated-gate bipolar transistor (IGBT), integrated gatecommutated thyristor (IGCT), and cathode metal oxide semiconductor controlled thyristor (CS-MCT), each having its advantages and disadvantages. The main characteristic of these switches is their speed, with operating times lower than 100 μ s; however, SSCBs present highpower losses, and are expensive and also too large for some applications, since they require heat sinks [7]. Another group of SSCBs is devices in which the predominant material is a wide band gap (WBG), such as silicon carbide (SiC) JFETs, SiC metal-oxide-semiconductor field-effect transistors MOSFETs, SiC static induction transistors (SiC) SITs, gallium nitride (GaN) high electron mobility transistors (HEMTs), and gallium nitride (GaN) FETs. WBG semiconductors exhibit superior material properties than those based on silicon, which enables the operation of these power devices at higher-temperature operation, higher blocking voltage capabilities, and higher switching frequencies; however, WBG technology itself is still evolving towards its maturity [90].

HCBs are a combination of the best features of mechanical and solid-state switches in a single device, overcoming their corresponding drawbacks. Indeed, hybrid switches feature small conduction losses, very short operating times, long service life, and high reliability, and do not require special cooling equipment, which shows a new direction in the research and development of switches for engineering applications [17]. However, the switching speed strongly depends on the mechanical parts of the system [49].

Solid-state switches generally use an auxiliary circuit to bring the current to zero through voltage or current switching in order to prevent arc formation. However, the auxiliary devices must be ready to act before the fault current exceeds the switch's maximum capacity value, so the fault detection time is a critical issue for conventional solid-state switches. To mitigate this issue, a creative design called the Z-Source circuit breaker has been proposed, which possesses significant characteristics such as natural commutation, automatic disconnection of the faulted load, simple control circuit, fault source isolation, inherent coordination capability, Z-source impedance fault limiting capability, and bidirectional power capability. This circuit breaker utilizes a portion of the large transient current that occurs during a fault and directs it through capacitors to naturally trigger a Silicon-Controlled Rectifier (SCR) for switching purposes [14].

In the present project, a comparison was made between the classic Z-source topology and its modifications to observe their behavior in the presence of electrical faults caused by overcurrents in medium voltage DC microgrids. A total of 19 representative topologies, designed for either uni-directional or bi-directional operation, have been selected from the literature. These topologies have been classified based on their intended purpose, and simulations using the OpenModelica software have been performed for all of them. Through these simulations, the topologies are analyzed and compared using parameters that provide insights into their functionality and suitability for operating in a medium voltage DC microgrid (DCMG).

1.1 Problem statement

DC microgrids (DCMGs) offer numerous advantages over AC microgrids, such as higher efficiency, greater stability, and compatibility with renewable energy sources. However, the implementation of DCMGs presents technical challenges, particularly in terms of achieving suitable protection. Currently, there are no standardized guidelines for DCMG protection. The existing protection devices such as fuses, mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs), and hybrid circuit breakers (HCBs) have limitations in terms of response time, arc extinction, power losses, and size. To address these challenges, Z-source circuit breaker (ZCB) topologies comparison was performed which offers features like natural commutation, fault isolation, coordination capability, and bidirectional power flow.

Publications on topologies based on modifications of the classic Z-source have been growing in recent years. The reviewed topologies in the literature have specific focuses, such as addressing speed-triggering issues, resolving the number of elements in conduction, optimizing switching losses, applications for low-voltage networks, and accommodating load current variations. Each topology is simulated with specific parameters for a particular purpose. However, it is not clear whether all these topologies are suitable for medium-voltage DCMGs, as they need to be compared using the same parameters as those used for medium voltage DCMGs. Furthermore, it remains unknown whether the modifications made to the classic Z-source topology for both uni-directional and bi-directional operation have fully resolved the applicability of Z-source topologies and their modifications in any medium-voltage microgrid. Additionally, understanding the different implemented switching strategies to shut down the circuit breaker is important as a knowledge base for future research endeavors. It is imperative to select the topologies according to the solutions.

1.2 Research question

In the context of the protection of medium voltage DC microgrids, there is a doubt as to whether the Z-source topologies and their modifications have already solved the problem of the absence of zero crossing of the current before faults in DC microgrids; the arcing problem in switching; the fault clearance times necessary to protect DC microgrids; high conduction losses; the total safety of the source and the load before an overcurrent in the load and the reduction of the weight and volume of the switching circuits. It is also important to know what is the difference between the strategies used by some topologies that have allowed to have a differentiating factor or advantage over the operation of others topologies?

1.3 Project Objectives

1.3.1 General Objective

To compare the overcurrent fault response of Z-source circuit breaker topologies for DC microgrid applications.

1.3.2 Specific Objectives

- To classify Z-source topologies according to the type of solution they propose.
- To select a suitable software to develop topology simulations: Matlab, ATPdraw, Python, LTS SPICE, OpenModelica.
- To simulate the different topologies of the Z-source circuit breaker with emphasis on fault clearing time and series resonance behavior, according to the minimum requirements of DC microgrids.
- To evaluate whether Z-source topologies are suitable for DC microgrid applications.

1.3.3 Methodology

Z-source circuit breakers are strong candidates for providing overcurrent fault response protection in DC microgrids due to their autonomous and natural commutation that utilizes the fault current for commutation. However, their performance under a fault is still under research. There are a large number of researchers that are proposing new topologies with the aim of improving performance. In this project, overcurrent fault response of various Z-source circuit breaker topologies for DC microgrid applications are compared. To compare different Z-source topologies, the following factors were considered :

- Z-source topologies in the literature was reviewed and classified into two main groups: 1) mono-directional topology, and 2) bi-directional topology. Within these two groups a second classification was made into topologies that do not use magnetic couplings and topology that use magnetic couplings. In addition, within the different topology groups with the same principle of operation and similarity of design and behavior, a representative topology was selected.
- Z-source topologies are constantly evolving, Z-source topologies with features that adhere to the fundamental characteristics of the clasic Z-source were chosen[59]. These features include the exclusive use of SCRs by reverse current switching, diodes for current flow blocking, natural commutating, and passive elements such as resistors, capacitors, and resistances as loads. In addition, it was chosen topologies that use RD damping circuits for power dissipation. Topologies using solid-state devices such as IG-BTs or IGCTs were excluded. In total, eleven single-directional and eight bidirectional topologies were analyzed.
- Several Z-source topologies have been simulated in the literature for different voltage levels and parameters depending on the proposed applications. In this project, all

topologies were simulated for a medium voltage DC microgrid using the same parameters, which facilitates the comparison of results and allows observing differences in behavior. However, it should be noted that the topologies can optimize their behavior for specific applications by varying their parameters.

- The study of losses in circuit breakers is not included in this project because the selected circuit breakers' characteristics allow for an estimation of conduction and commutation losses based on the number of elements interacting in each state.
- This project does not cover the operation or characteristics of control circuits or fault detection systems. Regarding the types of faults, serial fault currents are not considered. Only parallel fault currents are considered.
- Taking into account the aforementioned considerations, the simulations were carried out using ideal elements in order to facilitate comparison purposes. OpenModelica software, which includes the "Electrical" library, was selected for the simulations due to its efficient numerical methods for dynamic simulations of electrical circuits at various voltage levels and dynamic systems, as well as its user-friendly graphical interface. The numerical method used was DASSL, since it is an implicit numerical method suggested by the OpenModelica community. The simulation data is exported to CSV files for further analysis using free Python software tools, including Pandas and Matplotlib. Pandas is ideal for handling large amounts of data with minimal memory resources, while Matplotlib offers more advanced graph editing options than OpenModelica.
- All topologies are simulated in the time domain to observe the behavior of variables in fault current, commutation, resonance and power dissipation events. Analysis in the frequency domain is not included.
- The main parameters used for all circuits are: voltage source V_s of 6.000V, source inductance L_s of 10μ H, capacitors C of 200μ F, inductors L of 2.4mH, R damping resistors of 0.1Ω , fault resistor R_f of $20m\Omega$ SCRs and Ideal diodes with the minimum resistor assigned by the simulation software.
- The following variables are analyzed in this research: fault current, which indicates the occurrence of a short circuit event; the current flowing through the SCR to visualize the switching process; the currents flowing through the capacitors and inductors involved in the switching and resonance processes; the voltages across the capacitors and inductors involved in the series resonance of the circuits. Additionally, the voltage and current in the load, as well as the current in the source inductance that are monitored to verify whether there is any current returning to the source due to series resonance.
- Finally Analysis of the results of simulations is performed that allows comparison of: peak currents during energization of the commutation circuit, fault clearance, commutation times, common connections between source and load, power losses involving steady state and commutation elements, galvanic isolation, behavior under abrupt variations of load current other than faults, current return to the source due to series resonance, and operating directions.

• Once the comparisons have been made, you can have more clarity on the suitability of Z-source topologies and their modifications, within the scope of the simulations, to be the overcurrent fault protections in DC microgrids or what are the future challenges for these topologies to reach their maximum development.

1.4 Structure of chapters

This master thesis has being divided in the following Chapters: Chapter 2 includes a review of circuit breakers that have being used for protecting MGs, in this chapter, there are included the evolution of DC Breakers .Part of this chapter was taken from a paper that was published in applied sciences Journal and is part of the contribution of this research work [59]. Chapter 3 includes the most recently Z-sources topologies that were found in technical literature. This chapter includes, for each topology, the diagram, the description of components, and a complete explanation of the principle of operation. Chapter 4 corresponds to the simulation results of the Z-source topologies described in chapter 2. Chapter 5 is a comparison analysis of z-sources topologies in terms of their performance. Finally, Chapter 6 concludes the most relevant aspects of this thesis.

Chapter 2

State of the art fault current protection DC microgrids

2.1 Introduction

This chapter aims to provide context on the general characteristics of DC microgrids, types of faults, challenges faced by overcurrent protection in DC microgrids, overcurrent protection devices, and the evolution of DC microgrid fault protections. The information presented in this chapter is based on the article "Circuit Breakers in Low- and Medium-Voltage DC Microgrids for Protection against Short-Circuit" [59], which is an integral part of the current project.

2.2 DC Microgrid Faults

A DCMG is defined as a MG in which the power interchange is given in the DC bus [21]. A DCMG may be powered from AC sources, although these sources must be connected to the DCMG through AC to DC interfaces (power inverters) [55]. Figure 2.1 shows a conceptual diagram of a DCMG with the location of the protection devices (PDs) that are covered in this document.

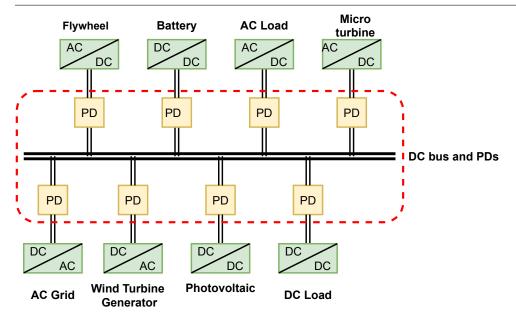


Figure 2.1: Conceptual diagram of a DCMG.

Faults in DCMGs can be divided into two principal types: the short-circuit fault current, and arc fault current [1]. This paper focuses on the short-circuit fault current.

Figure 2.2 depicts the types of short-circuit faults that may take place in DCMGs produced by over-current and short-circuit events. The following two types of faults are considered: line-to-line fault and line-to-ground fault. A line-to-line fault occurs when an undesirable connection is established between the positive and negative lines, creating a short circuit that connects the supply voltage terminals. In line-to-line faults, the wires are directly connected to each other; therefore, line-to-line faults are of low impedance, which are more dangerous, though they are easier to detect. In line-to-ground faults, one or both conductors are connected to the ground. Therefore, line-to-ground faults are high-impedance faults in most cases; nonetheless, they can be low-impact depending on the grounding setting used for the DCMG [9, 61, 37]. The ground fault is the most common type of fault in industrial systems [21].

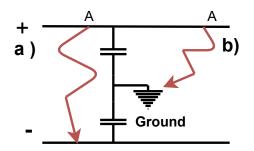


Figure 2.2: Types of faults: (a) line–line fault, (b) line–ground fault.

Concerning the behavior of the fault in DC systems, in steady-state operations, if the current ripple is small, it can be affirmed that the effect of the inductance is negligible. However, under a short circuit, the CB must act by opening the circuit which produces

9

a quick change in the current; under a fault, the effect of the inductance is considerable, and over-voltages are generated. These over-voltages may produce arcs in terminals of the CB. It is important to mention that the arc is easily extinguished in AC systems where the voltage waveform crosses through zero; however, this does not occur in DC systems in which the voltage waveform is constant and not crossing through zero. In consequence, arcextinguishing devices are required to effectively clear faults in DCMGs [54, 58]. Therefore, protection systems for DCMGs must be faster than those of AC systems. In DCMGs, protection must be configured for all faults on the upstream side of the microgrid because all resources feed the faults, which can have different characteristics in terms of magnitude, wave-front, fault current direction, and operation mode (island or grid-connected modes).

Fault response characteristics of DC systems can be divided into (a) transient state and (b) steady-state. These correspond to the transient part of the fault injected from the DC connection capacitors, the converter cable discharge, and the steady-state part injected from the power sources [69]. The transitory part of the fault currents can also be split into slow, medium, and fast front transients. Voltage-dependent charges, converter control, and batteries cause slow front transients. Over-current in capacitors used as filters cause medium front transients, while recovery voltage transients at the opening of the protective devices (PDs) cause fast front transients [16, 19].

2.3 DC Circuit Breakers

CBs for DCMGs have basically been composed of fuses, MCBs, SSCBs, and HCBs. All of these circuit breakers are still in use. This section explains their characteristics in detail, as well as their most relevant technical aspects.

2.3.1 Fuses

The fuse consists of an element in the form of a metallic conductor with a pair of contacts between them, and a box or cartridge to carry the fuse element. Depending on the voltage level, the cartridge is usually fitted with a device using material such as quartz sand for arc extinction inside. The principle of operation of the fuse is the heating effect of the electric current. If the current passes through a conductor with a certain resistance, the loss due to the resistance of the conductor dissipates in the form of heat. Under normal operating conditions, the heat produced in the fuse element is easily dissipated into the environment due to the current flowing through it. When a fault occurs, such as a short circuit, the current flow through the fusible element exceeds the prescribed limits. This creates excess heat, which melts the fuse and breaks the circuit.

Fuses are usually made of copper or silver and are mainly installed in series with the line. During a fault, the heat from the increased current blows out the fuse, causing the line to open. Fuses are used as the simplest and most economical form of protection in DC systems [7].

The selection of a fuse for an ACMG requires a response time in the range of 10–100 ms to operate and interrupt the fault; however, the nature of a DCMG requires a maximum operating time of 0.5 ms, which represents a limitation [4, 24]. For the selection of fuses, it must be guaranteed that the time constant of current rise during the fault is lower than a certain limit, since a slow rise in temperature allows the heat-absorbing material to extinguish

the arc [21]. Fuses are ideal for applications in low-inductance DC systems, because the time for the fuse to blow out must be minimal [29]. Although a fuse is a very simple and inexpensive form of protection, it has several disadvantages: it must be replaced after operation and does not have the possibility of discriminating between a transient and a permanent fault [29]. Additionally, when a fault occurs in a single line, fuses only isolate the failed pole, leaving the other pole active; despite this, fuses are considered a good option to protect batteries and photovoltaic systems when trip time and cost are considered, as well as the protection of load-feeders working together with mechanical switches and relays [9]. In the Ref. [68], fuses were considered as a viable alternative to mechanical DC breakers; however, fuses installed in DCMGs must be provided an auxiliary device to extinguish the arc produced in the opening of the fuse during a fault. The authors in the Ref. [68] recommended a time constant to faults of >6 ms; however, this could decrease the fuse's ability to interrupt the current and extinguish the arc. In the Ref. [64], a detailed analysis of fuses used in power converters was presented. Fuses were found to be an effective means of protection, although the required amount of capacitance at the output of the voltage-balancing converter can be high, which affects the total cost of the system; therefore, in terms of power converters, the ideal application is to use the fuses as backup protection for the main switch. Fuses are not recommended as backup protection in DCMGs with ring configuration, since in this case, there are bidirectional current flows which require a communication system and the isolation of the cable in case of a fault [64].

2.3.2 Mechanical Circuit Breakers

MCBs are devices that use mechanical parts to interrupt the flow of current in the event of a fault. The operating mechanisms of MCBs can be divided into hydraulic, spring, pneumatic, and magnetic [7]. Spring and magnetic operating mechanisms are more common in vacuum CBs (VCBs). When a MCB reacts to a fault, its moving contact starts to separate, and the contact area is reduced. The current density increases and the energy begins to evaporate the metal, resulting in a plasma arc, which restarts due to the capacitance and inductance of the system. Although the contacts are physically separated, the arc keeps the current flowing. As the contact separation increases, the degree of the arc column is influenced by the characteristics of the surrounding medium. The arc current will be terminated when the arc plasma becomes a dielectric medium. Moreover, the ability to limit the current is determined by the difference between the arc voltage and the system voltage. To mitigate the impact of the arc, several solutions have been proposed: (a) MCBs with passive current switching, (b) MCBs with active current switching, and (c) artificial current zero vacuum switch (ACZ-VCBs). In MCBs with passive and active current switching and ACZ-VCBs, a voltage opposite to the system that conducts zero-crossing artificial currents is created by a resonant inductive (L) capacitive (C) series circuit [2]. In the passive switching method, when the switch is open, a current flows through the LC circuit with a capacitor that has not been pre-charged, and it starts to oscillate and creates a zero crossing current, in which case the mechanical switch completely interrupts the current flow, increasing the voltage to a certain specific value. Once the voltage reaches such a value, the current flows to energize the energy-absorbing circuit, which is, in most cases, a metal oxide variator (MOV) used to dissipate the stored energy.

Figure 2.3a shows a MCB with passive commutation. Its components are: (1) the branch

of the switch, (2) branch of the series resonant circuit, and (3) branch of the energy-absorbing circuit. In the case of active switching, the capacitor has already been pre-charged, and when the switch opens, the capacitor injects a negative current equal to the fault current to make a zero crossing of the current. During the interruption process, the magnetic energy is stored in the inductor and the varistors are connected in parallel with the switch to mitigate the over-voltage and absorb the energy stored in the inductor. Figure 2.3b shows the mechanical switch with active current switching.

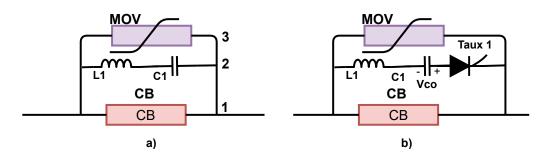


Figure 2.3: (a) MCB with passive resonance, (b) MCB with active resonance [7].

In the VCB, once the contacts are separated, the arc current generated across the electrodes is extinguished using a vacuum chamber so that a vacuum arc is initiated at the contacts. This arc is then extinguished and the conductive metal vapor condenses on the metal faces, and the dielectric strength in the electrode is reduced. VCBs feature arc voltages lower than 100 V, and they do not limit the arc currents of MVDC MG. VCBs are effective because they avoid re-ignition of the arc after zero current. The most frequently used approach of VCBs in MVDC interruption is based on artificial current zero (ACZ). Figure 2.4 depicts a general circuit of an ACZ-VCB. The interruption process begins with the separation of the VCB followed by the formation of a vacuum arc conducting line current i1. As the electrode gap of VCB reaches a certain safe stroke to withstand the recovery voltage, the commutation circuit breaker (CB) injects a high-frequency oscillating commutation current i2, which is generated by discharging a pre-charged commutation capacitor C1 through inductance L1. In consequence, the superimposition of i2 forces i1 to drop to zero. Then, VCBs can be interrupted by extinguishing the vacuum arc. A metal oxide arrester is used to suppress the over-voltage across the VCB.

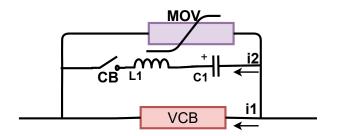


Figure 2.4: General circuit of an ACZ-VCB.

The main advantage of MCBs is low losses and low costs; however, the fault-clearing time is between 30 and 100 ms [76, 91], which is too high for DCMG requirements.

2.3.3 Solid-State Circuit Breakers

This section contains the description of SSCBs, the most recent advances in terms of semiconductors and materials, and also the most recent topology of SSCBs reported in the technical literature.

SSCBs General Description

SSCBs do not have mechanical moving parts to operate in case of electrical faults, since this is performed by semiconductor devices. Compared to MCBs, SSCBs are much faster and feature greater accuracy in controlling their operation. With the rise of power electronics in the 1970s, the SCR thyristor appears as one of the first solid-state switches. With the development and contribution of power control systems between 1980 and 1990, the growth of solid-state switches became remarkable, whose predominant material is silicon (Si), such as SCR[15], IGBT [89], IGCT [6], GTO [39], and CS-MCT [86]. Si devices have a high level of maturity and are commercially available with a wide range of voltages and currents. SSCBs have the following advantages: fast operating times of less than 100 μ s, no arc, no sound, no gas emissions, long service life, and high reliability and applicability [23, 25, 57]. However, SSCBs have the disadvantage of presenting high power losses, and being very expensive and large, due to the need for heat sinks [7]. Another group of SSCBs is the devices proposed since 1989 [3], in which the predominant material is a wide band gap (WBG), such as SiC JFETs SiC ETO, SiC MOSFETs [45], SiC SITs [70], GaN HEMTS, and GaN MOSFETS [74]. WBG semiconductors exhibit superior material properties than silicon ones, which enable the operation of power devices at higher-temperature operation, higher blocking voltage capability, and higher switching frequencies [66, 50]. Although WBG semiconductors offer significant improvement over silicon ones in power efficiency, switching frequency, and operating temperature, their proliferation into the mainstream power electronic market is impeded by high device cost and reliability concerns, and this is mainly because the WBG technology itself is still evolving towards its maturity [76].

SSCBs can be damaged due to overvoltage of the inductive components of the system, hence the importance of reducing this voltage for the safety of the device. To protect the solid-state switch from overvoltage at the moment of opening, additional elements are required, such as resistors, capacitors, diode (RCD) Snubber Circuits, metal oxide varistors (MOV), and freewheeling diodes [88, 46]. In the Ref. [37], the authors described the advantages and disadvantages of different SSCB snubbers: the metal oxide varistor (MOV), single snubber capacitor, dissipative snubber, RC snubber, and RCD snubber. They concluded that RCD snubber is the best option and is able to avoid the oscillation between C and L by using a fast recovery diode to clamp the changing voltage; it is, therefore, a suitable candidate for medium-capacity applications [37]. The protection control, heat cooling system, sensor, and damping system for a SSCB are depicted in Figure 2.5.

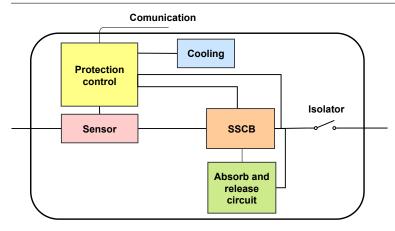


Figure 2.5: Conceptual diagram of a typical SSCB.

One of the main drawbacks of SSCB is the lack of galvanic isolation in the open state. This can be overcome by adding an auxiliary circuit based on two mechanical switches in series with the SSCB [7] (see Figure 2.6). This circuit is opened after the trip of the SSCB, guaranteeing complete isolation between load and supply. Galvanic isolation of SSCBs is a key feature for achieving fault detection, isolation, and DCMG reconfiguration. The mechanical switches that provide physical isolation are as follows: (1) a mechanical switch to handle the high current that appears through the SSCB when the SSCB interrupted the fault current, and (2) a secondary mechanical switch for interrupting the leakage current during isolation [69].

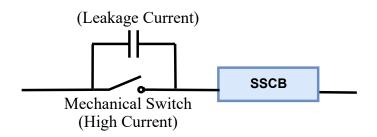


Figure 2.6: Galvanic isolation circuit for SSCBs.

Recent Developments of SSCBs

The following paragraphs show the most recent developments of SSCBs in terms of the type of semiconductors and material used:

In the Ref. [80], the authors compared the switching waveforms of Si GTO and SiC GTO switches. The latter is known as an automatic turn-off device that controls high voltages and large currents. GTO is preferred for DC applications because it has an independent gate for turn-on and turn-off. The results showed Sic GTO times of 2.21 μ s, which are lower than Si GTO times of 10.82 μ s.

In the Ref. [81], a SSCB based on IGBTs was implemented in a DCMG. The designed SSCB was capable of low-end lighting protection applications and tested at 50 V. A 15 A continuous current rating was obtained, and the minimum response time of the SSCB was nearly 290 times faster than that of conventional AC protection methods. The development

of this technology shows promise for the future of integrated power systems; nonetheless, the cost associated with these new technologies remains an obstacle in the growth of commercial DC systems.

In the Ref. [6], a new SSCB was designed based on IGCT technology for an aircraft DCMG. The authors proposed a new IGCT-based SSCB that uses Y-shape coupled inductors that forces the current to zero to isolate short-circuit faults. With this implementation, there is no need to add a snubber or clamp circuit across the IGCT because the Y-shape coupled inductors drive inductive currents to zero before the IGCT commutates off. They obtained a SSCB with an efficiency of 99.94%, and operating time of around 20 μ s.

In the Ref. [88], a suitable IGBT for low-voltage (around 400 V) fault protection of a DCMG was proposed. The simulation results showed that the SSCB acted reliably and the fault current dropped to zero within 15 μ s until the fault was removed from the system and reconnected within 8 μ s, while the rest of the system continued to operate normally. However, the high conduction loss and cost of the semiconductor breakers technology was considered as the main obstacle to their wider use in electrical protection applications.

Si IGBT-based breakers have also been proposed to interrupt fault currents In the Ref. [88]. However, these breakers feature relatively high power losses due to the finite conductivity modulation effect of the IGBT [27]. Besides, the maximum current interruption ability of these breakers are also limited by the saturation current of the IGBT which reduces the short-circuit requirements from 10 to 5 μ s. However, Si IGBT would reduce the on-state losses to increase the channel width-to-length ratio [30].

In the Ref. [90], Si MOSFET, Si CoolMOS, SiC MOSFET, and SiC JFET with the lowest on-resistance Rds (on) for a rated breakdown voltage devices were studied. The SiC junctiongate field effect transistor (JFET) has the best maximum turn-off capability, the maximum current that a switch can interrupt, and the highest peak power density.

In the Ref. [45], a photovoltaic-driven SSCB with latching and current-limiting (LCL) capabilities (SSCB-LCL) was proposed. In case the load current is exceeded, the SSCB-LCL limits the load current during a pre-configured time by the user. If the fault persists, after the pre-configured time has elapsed, the load is disconnected from the input. External commands were also included for controlled load disconnection or restarting the SSCB-LCL. This circuit contains very few components, does not require external supply, and provides a large bandwidth control signal.

In the Ref. [55], the authors proposed a SSCB that detects short-circuit faults by sensing the drain source voltage, in which case it extracts power from the fault condition to turn off and stop a SiC JFET. The authors proposed a new two-terminal for the SSCB that can be placed directly on a circuit branch without requiring any external power supply or additional wiring.

In the Ref. [54], a semiconductor DC circuit breaker using SiC static induction transistor (SiC) SITs was investigated in applications for data centers at 400 V. SiC SITs have extremely low on-state resistance and a very large safe operating area. The experimental results showed that the SiC SIT's fault current decayed to 0 A within 20 μ s.

The authors in the Ref. [74] experimentally demonstrated the feasibility of using 650 V GaN bidirectional devices in SSCB applications. GaN devices outperform silicon MOSFETs with regard to the on-resistance value during operation (Rds) versus the breakdown voltage, allowing a further increase in switching frequency and efficiency, and reduction in physical size. The authors reported a new bidirectional SSCB, which comprises a single 650 V, 200 m Ω

dual-gate, bidirectional, normally-on, GaN-on-Si HEMT as the static switch, and a faststarting isolated DC/DC converter and a diode bridge as the fault detection and protection driver. When a fault occurs, the switch opens, bringing the current to zero in 0.8 μ s.

In the Ref. [91], a discussion on the basic concept and general design methodology of the intelligent tri-mode SSCB (iBreaker) was provided. Commercial LVDC GaN FETs in various SSCB designs that offer m Ω -resistance and passive cooling were presented. The SSCB ibreaker identifies and exploits a distinct pulsewidth modulation (PWM) current-limiting (PWM-CL) state in addition to conventional on and off states in a bidirectional commoninductor buck topology without needing additional semiconductor power devices. The IBreaker can operate in the "on" state for continuous conduction of normal load currents, or in the "off" state to interrupt fault currents. In addition, it can operate in the PWM-CL state with a moderate overcurrent for a short period of time to facilitate intelligent functions, such as soft startup, fault authentication, and fault location. The iBreaker switches from the PWM-CL to the off state if it deems the overcurrent condition to be a true short-circuit fault rather than a startup scenario after a short time-period. The tri-mode iBreaker quickly limits a detected overcurrent to 2–3 times of the rated nominal current within a few microseconds, and conducts a fault authentication process within a preset time window (typically a few milliseconds) while operating at a relatively low overcurrent. This significantly reduces the stress on the wiring and power semiconductor devices, and reduces the current rating and cost of semiconductor switches.

In the Ref. [77], the formation of Ohmic Contacts in SSCBs was presented. Ohmic contacts are necessary since they ensure the flow of signals and power from the semiconductor to the peripherals. However, the arrangement of ohmic contacts in p-type 4 H-SiC is still a highly discussed subject, due to the intrinsic challenge of acquiring a low value of specific contact resistance in p-type WBG semiconductors. Moreover, the shortage of metals that provide a low Schottky barrier to p-type SiC and high ionization energy of the Al dopant renders the arrangement of a tunneling contact to a p-type SiC extremely troublesome.

In the Ref. [65], a 4 H-SiC MOSFETs low-inversion channel mobility was reported. This 4 H-SiC MOSFETs revealed stable behavior when at room temperature, as well as for moderate stress periods. However, with rising temperature (>150 °C) and stress periods, a significant threshold voltage instability was found to occur [33].

In the Ref. [65], it was indicated that CBs based on GaN should ensure much better efficiency with respect to CBs based on SiC because of its higher critical electric field and greater electron mobility. However, GaN also suffers from many manufacturing problems concerning the more advanced SiC technology, such as the insufficiency of high-quality freestanding substrates, which prohibits the advancement of vertical structures in the internal design of transistors [56, 77].

In the Ref. [34], a short cathode metal oxide semiconductor controlled thyristor (CS-MCT) was proposed in a 400 V SSCB, which achieved a 30% reduction in energy loss compared to using a Insulated Gate Bipolar transistor (IGBT). However, this kind of SSCB is only able to interrupt unidirectional fault currents and requires an additional DC source to pre-charge the commutating capacitor, thus increasing the circuit complexity and limiting its applications. In the Ref. [31], it was indicated that thyristors are superior to IGBTs in terms of their rating, cost, drive circuit design, and reliability. Moreover, thyristor-based circuit breakers are a common approach to tackle the conduction losses of solid-state circuit breakers. In fact, thyristors constitute one of the best power electronic types of switches

from the point of view of conduction losses, the rating, cost, symmetric blocking capability, and reliability aspects; however, this breaker needs additional commutating circuits.

Z-Source: The New Generation of SSCBs

Z-source circuit breakers (ZSCBs) constitute one of the most recent lines of research and development of circuit breakers for over-current faults in DCMGs. ZSCBs feature natural switching, automatic disconnection of the fault load, simple control circuit, isolation of the fault source, and inherent coordination capacity. Furthermore, the ZSCBs' impedance fault limits the fault current and can operate in bidirectional mode. The ZSCBs can take the transient current that occurs at the fault and pass it through the ZSCB capacitor so that the semiconductor-controlled rectifier (SCR) is disconnected. Chapter 3 delves into the Z-source and its modifications.

2.3.4 Hybrid Circuit Breakers

This section presents the description of HCBs and their most recent advances in terms of semiconductors.

General Description of HCBs

HCBs are a combination of the best features of MCBs and SSCBs in a single device, overcoming the drawbacks of both devices. HCBs have small conduction losses, very short operation times, long life, high reliability, and do not require special cooling equipment. Additionally, they feature simpler control, and more compact volume [85], resulting in a new direction of research and development of switches for engineering applications. Figure 2.7 illustrates the current path in the different states for HSBs—in normal condition, the current I_1 passes through MCB. When a fault is identified, the MCB starts the opening of its contacts and sends a turn-on signal to the SSCB. The established arc voltage is increased until it exceeds the voltage drop of the SSCB. In this case, the current can be naturally commutated from the MCB to the SSCB. The SSCB continues conducting current I_2 until the MCB is able to block the full voltage. At this point, the SSCB is turned off and the voltage increases quickly because of the circuit inductors. While the voltage reaches its breakdown value, the fault current I_3 commutes to the MOV to clamp voltage and approach the current to zero. Finally, when the fault current is zero, the RCB is opened to isolate the faulty line from the DC grid to protect the MOV from thermal overload [25]. Moreover, a current-limiting reactor (CLR) in series with a residual circuit breaker (RCB) was added to limit the rate of rise of currents and to provide complete galvanic isolation.

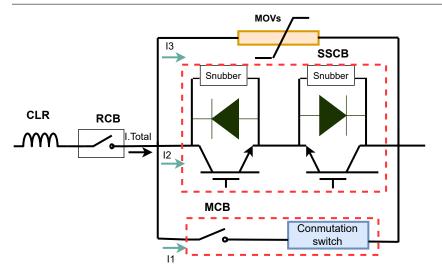


Figure 2.7: Diagram of conventional HCBs [7].

Recent Developments of HCBs

The following paragraphs have the purpose of showing the most recent developments for HCBs in terms of the type of semiconductor and material used:

In the Ref. [18], the authors compared the general characteristics of press pack IGBT and injection-enhanced gate transistor (IEGT) used in HCBs. Basically, the maximum blocking voltage, maximum turn-off current, surge current, di/dt, on-state voltage, drive power, failure mode, and voltage balance for series were compared. The IEGT was more suitable for natural commutation than HCBs when the system fault current was not very high. Comparatively, IGBT and IEGT were more suitable for very high current interruption, and IEGT was the superior selection based on their experiments. The advantage of HCBs is that they have very low on-state losses. Furthermore, the current can be turned off independently from a natural zero crossing. However, HCBs are very expensive and their speed is highly dependent on the mechanical parts of the system [18]. Consequently, a standard mechanical circuit breaker cannot be used because of its lack of speed [49], which represents a limitation for DCMG protection. To improve the speed of HCBs, several fast-acting mechanisms have been proposed to reduce the commutation time of MCBs to SSCB, such as Thomson coil and piezoelectric actuators, which act in hundreds of microseconds. However, in experiments performed with HCBs, the whole process takes between 0.5 and 5.5 ms.

2.4 DC CB Evolution

This section has the purpose of showing the DC CB evolution. DC CBs have been evolving for more that 100 years. For this reason, the time-line is divided after and before the definition of DCMGs. Figure 2.8 corresponds to the evolution of DC CBs before the emergence of DCMGs, while Figure 2.9 illustrates the evolution of DC CBs after the emergence of DCMGs.

Electrical fuses were patented over 100 years ago to operate in DC networks in the late 1890s [84]. The silicon SCR thyristor SCR appeared as a superior alternative to the mercury arc rectifier in the 1950s for application to various AC power electronics devices, since its

18

switching is based on zero crossing of the current. In 1980s, there was a considerable evolution in DC CBs: (a) a DC MCB with LC series resonance to create zero crossing of the fault current and mitigate the arcing problem in switching for HVDC networks was proposed [2]. In fact, the LC series resonance concept served as the basis for the development of the ZSCB for MVDC and LVDC DCMG applications. (b) With the advent of PWM, the development of auto turn-off devices having fast switching and high withstand capability was necessary. Gate Turn-Off (GTO) thyristors meet this requirement and easily withstand high voltages and high currents. The gate turn-off thyristor (GTO) has all the advantages of that of the SCR, and can also be turned off when desired through its gate. Unfortunately, its gate drive current requirements are difficult, making the drive circuit very complex. (c) IGBTs have the best characteristics of MOSFET and BJT transistors with the speed characteristics of high switching speed and high voltage capability, being quite practical in the low- and mediumcurrent ranges. Nonetheless, IGBTs were not suitable for simultaneous high-voltage and high-current operation. (d) Another alternative was the MOS gate thyristors, such as the MOS-controlled thyristor (MCT) and base resistance-controlled thyristor (BRT) for highvoltage applications, due to their single gate drive capabilities and low forward voltage drops. However, as these devices lacked the current saturation feature, they showed much poorer short-circuit SOA characteristics compared to IGBTs [30].

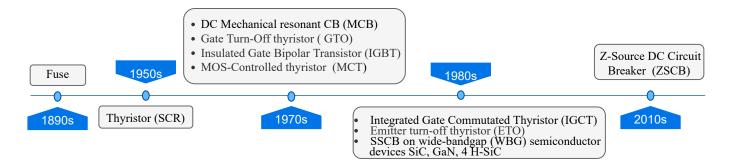


Figure 2.8: Timeline evolution of DC CBs before the definition of DCMGs.

In the 1990s, considerable progress was achieved: (a) IGCT, which has all the advantages of other thyristor-type devices, such as SCR and GTO, was proposed. IGCT features a high voltage, and current and surge current capabilities, which satisfy the high current trend of solid-state switch. The switching speed of IGCT is about six times slower than that of IGBT, but that is not really a problem in switch applications, since IGCT-based SSCB is at least 900 times faster than a typical EMCBs. (b) ETO, a hybrid device of MOS and GTO that combines the advantages of GTO and MOSFET, was proposed. (c) WBG semiconductors exhibit material properties superior to silicon, which allow operation of power devices at higher operating temperature, higher blocking voltage capability, and higher switching frequencies. In the Ref. [30], the authors presented recent applications with SiC, GaN, and 4H-SiC materials, such as SIC ETO, SIC MOSFET, SIC SIT, SIC JFET, and GaN MOSFET. In 2010, a novel alternative for DCMG protections for MVDC and LVDC appeared: the Z-Source DC circuit breaker, ZSCB. This circuit breaker uses a z-source L-C circuit to automatically switch a main path SCR during a fault. Compared to existing DC circuit breakers, the z-source circuit breaker features very fast tripping, easier control,

and the source does not experience a fault current [15]. Figure 2.9 corresponds to a time line after the definition or emergence of DCMGs.

After the definition of DCMGs, DC CBs have evolved quickly, trying to satisfy the DCMG requirements. Figure 2.9 shows the CBs for LVDC and MVDC in chronological order obtained from the literature review that were validated with experiments, prototypes, or simulations in the last 20 years. The participation of the different technologies and topologies proposed as candidates for DCMG protection can be observed. IGBTs [89, 80] (2009, 2011, 2013, 2016, 2019) and IGCTs [6] (2009, 2021), the most widely used SSCBs for MVDC and LVDC DCMG applications today, due to their characteristics and maturity, have been available for more than 20 years. However, in recent years, the number of SSCBs proposed as candidates for DCMG protection has increased. It should be added that ZSCBs [15, 40, 41, 28, 42] (2010, 2011, 2013, 2015, 2016) and derived topologies, such as TZSCBs [91, 82] (2018, 2020, 2021), are under development, which have proven to be strong candidates for DCMG protection of SSCBs. MCTs [86, 87] (2010, 2021, 2021) were out of the market due to their worse short-circuit SOA characteristics. However, CS-MCTs are presented as a candidate for DCMG protection, with very good results. WGB SSCBs are continuously evolving as an alternative to replace Si SSCBs: SiC ETO(2016), SiC MOSFET [33] (2010, 2016), SiC JFECT [45] (2011, 2016, 2020), SiC SIT [70] (2014), and GaN FET [74, 65] (2016, 2019).

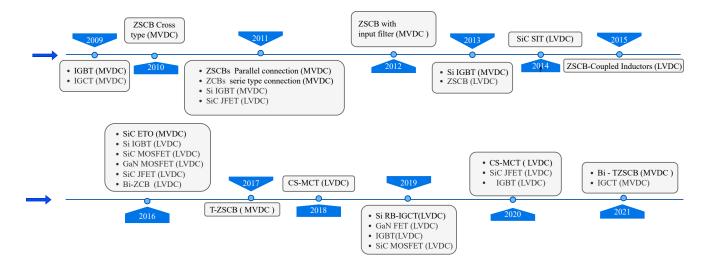


Figure 2.9: Timeline evolution of DC CBs after the definition of DCMGs.

Chapter 3

Z-source topologies and their modifications

3.1 Introduction

3.2 Mono-directional topologies

In monodirectional topologies, the breaker circuit only operates in one direction. Some topologies proposed in the literature use magnetic couplings for commutation and others do not use magnetic couplings. In this section, the topologies that do not use magnetic couplings are discussed first because they are more similar to the classical Z-source and then the topologies that use magnetic couplings.

3.2.1 Topologies without magnetic couplings

In the topologies topologies without magnetic couplings; the fault is supplied through the high frequency circuit in which, the current flowing through the capacitors reverse bias the SCR for commutation.this section presents topologies without load variation and a topology that includes load variations.

Classic Z-source topology

Classical Z-source topology opens an interesting line of research on the subject of overcurrent fault protection in DC microgrids. This topology is also called Cross Z-source topology. Classic Z-source breakers are characterized by natural commutation, fast operation, simple control circuit, fault source isolation, automatic disconnection of fault load and inherent coordination capability [14].

Classic Z-source topology is depicted in Figure 3.1. It is composed of one SCR, two capacitors (C_1) , (C_2) two inductors (L_1) , (L_2) in parallel with diodes (D_1) , (D_2) and resistors (R_1) , (R_2) series array. Assuming that inductors (L_1) and (L_2) , capacitors (C_1) and (C_2) , diodes (D_1) and (D_2) and resistors (R_1) and (R_2) have the same values (L), (C), (D) and (R) respectively. Z-source is between the voltage source (v_s) and load composed of a capacitor (C_L) and a resistor (R_L) . G_f is the conductance used to simulate the fault conductance in the load. The aim of the Z-source breaker is safely disconnect the source when a short

circuit occurs. Classic Z-source breaker has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCR, inductors and load are equal in steady state to i_L . The current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4 which consists of the source, the SCR, inductor L_1 , load R_L and inductor L_2 ; in this state, capacitors C are also charged with the source voltage and they behave as an open circuit see state 1 Figure 3.2. 2) Second state is the transient state or fault occurrence state. When a fault occurs in 6, the fault current is supplied by the capacitors C_1 and C_2 in series and C_L . The series capacitors C and C_L form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitors C_1 and C_2 and SCR following the red line through 7, 6, 9 and 1 in the direction of the source; please see Figure 3.1. High frequency current of the capacitors increases until is equal to the low frequency current through the inductors i_L , then the SCR is reverse biased and commutates off (source is disconnected); please see i_{SCR} in state 2 of Figure 3.2. 3) Third state, after SCR is turned off, two series LC circuits are connected to the fault and load through 9, 2 and 7, 4; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor L_1 matches the voltage across the capacitor C_1 or the voltage across the inductor L_2 matches the voltage across the capacitor C_2 . When the capacitor voltage is reached by the inductor voltage; the voltage at the output becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR becomes negative. Then the SCR is forward biased. For this reason, one of the functions of the control is to deactivate the gate before the inductor and capacitor voltages at resonance reach half the source voltage or activate the SCR with a single pulse. The resonance ends when voltages in the inductor tend to become negative, please see state 3 of Figure 3.2. 4) Fourth state begins when the voltage on the capacitor decays to zero after the resonance has ended. Current from the inductors L_1 and L_2 continues to flow through the diodes and resistors until the current decays to zero, 2, 12, 13 and 4, 10, 11 respectively. The diodes does not allow the inductor current to recharge the capacitor. The use of Z-source technology for medium voltage networks on ships is proposed in [13]. Through simulations, Z-source performance has been validated for medium voltage at 6.000 V DC, demonstrating instantaneous commutation and fault clearance in tens of microseconds. Furthermore, the paper presents methods for sizing Zsource elements. In [14], a laboratory prototype for low voltage at 400V DC was proposed, vielding positive results. The paper also suggests employing Z-source technology for the protection of power converters supplying motors. In [44], tests were conducted with a low voltage prototype at 280-440V DC and a communication architecture was proposed for DC microgrid implementation. in [60] it is proposed to add resistors to the capacitors to mitigate capacitor inrush currents. Simulations are carried out for medium voltage networks at 6.000V DC, obtaining a reduction of the inrush currents with additional resistors.

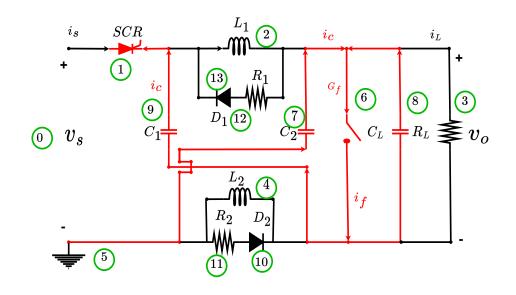


Figure 3.1: Classic Z-source circuit breaker [13]

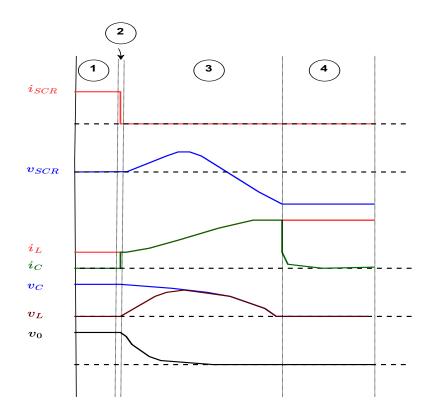


Figure 3.2: Classic Z-source commutation states, adapted from [13]

Parallel Z-source topology

In the parallel Z source topology, LC legs are connected in parallel after the SCR turn off, hence referred to as parallel Z-source. In the parallel Z source topology, the circuit has been

placed in line with the power transmission to provide a common point between the source and the load. Parallel Z-source topology meets the disconnection characteristics of the classic Z-source topology. Parallel Z-source topology is depicted in Figure 3.3. It is composed of one SCR, two capacitors (C_1) , (C_2) two inductors (L_1) , (L_2) in parallel with diodes (D_1) , (D_2) and resistors $(R_1), (R_2)$ series array. Assuming that inductors L_1 and L_2 , capacitors C_1 and C_2 , diodes D_1 and D_2 , and resistors R_1 and R_2 have the same values L, C, D, Rrespectively. Parallel Z-source is between the voltage source (v_s) and load that is composed by a capacitor (C_L) and a resistor (R_L) . G_f is the conductance used for simulating a short circuit in the load, please see Figure 3.3. The aim of this topology is to provide a common ground between the source and the load, preserving the main characteristics of the classic Z-source. Parallel Z-source breaker has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, source v_s delivers energy to the load R_L . The currents of the source, SCR, inductors and load are equal in steady state to i_L current. The current passes through the low-frequency circuit composed by 0, 1, 2, 3, and 4; this circuit basically consists on the source, the SCR, inductors L_1 , L_2 and load; in this state, capacitor C_1 and C_2 are discharged, they behave as an open circuit. 2) Second state is the transient state or fault occurrence state. When a fault occurs in 6, the fault current is supplied by the capacitors C_1 , C_2 and C_L . The series capacitors C_1 , C_2 and C_L form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitors C_1 , C_2 and SCR following the red line through 0, 7, 2, 8, 6, and 9; in reverse direction of the SCR current, please see Figure 3.3. High frequency current of the capacitors increases until is equal to the low frequency current through the inductors i_L , then the SCR is reverse biased and commutates off. The parallel Z-source has the same behavior as the classic Z-source until commutation occurs. 3) Third state corresponds to resonance series, it is composed by the voltage source V_s , two capacitors C_1 , C_2 and two inductors L_1 and L_2 . After SCR is turn off, two series LC circuits are connected to the fault and load through 0,7, 1 and 8, and 3, 8; initiating an LC resonance series. Note that in this topology after the SCR is commutates off, the voltage source is still connected to the resonant circuit. Indeed, the source inductance is not negligible. If the source inductance is large, a series resonance occurs between the capacitors C_1 and the source inductance in the end state. Then, the oscillations in the capacitor voltage grow. A filter design may be used to mitigate this issue [12]. 4) Fourth state begins when current from the inductors i_{L1} and i_{L2} continues to flow through the diodes and resistors until the current decays to zero, 1, 12, 13 and 3, 10, and 11 respectively.

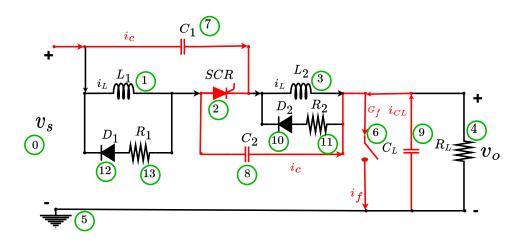


Figure 3.3: Parallel Z-source topology [13]

Series Z-source topology

Series Z-source topology is depicted in Figure 3.4. It is composed of one SCR, two capacitors $(C_1), (C_2)$ two inductors $(L_1), (L_2)$ in parallel with diodes $(D_1), (D_2)$ and resistors $(R_1), (R_2)$ series array. Assuming that inductors (L_1) and (L_2) , capacitors (C_1) and (C_2) , diodes (D_1) and (D_2) , and resistors (R_1) and (R_2) have the same values (L), (C), (D), (R) respectively . Series Z-source is between the voltage source (v_s) and load that is composed by a capacitor (C_L) and a resistor (R_L) . G_f is the conductance used to simulate the fault in the load. The aim of Series Z-source topology is to reduce the source current in the resonant state which is absorbed by the source in the parallel Z-source topology, preserving the main characteristics of the classic Z-source. Series Z-source breaker has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCR, inductors and load are equal in steady state to i_L current. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4; this circuit consists of the source, inductor L_1 , the SCR, inductor L_2 and load. In this state, capacitor C1 are also charged with the source voltage and and capacitor C2is discharged, they behave as an open circuit 2) Second state is the transient state or fault occurrence state. When a fault occurs in 6, the fault current is supplied by capacitors C_1 , C_2 in series and C_L . The series capacitors C_1 , C_2 and C_L form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitor C_1 , SCR and C_2 following the red line through 9, 2, 7,6, and 8; please see Figure 3.4. High frequency current of the capacitors i_c increases until is equal to the low frequency current through the inductors i_L , then the SCR is reverse biased and commutates off. 3) Third state corresponds to resonance series condition. It is composed of the voltage source v_s , two capacitors C_1, C_2 and two inductors L_1 and L_2 . After SCR is turned off, two series LC circuits are connected to the fault and load through 0, 1, 7 and 9, 2; initiating an LC resonance series. Note that in this topology after the SCR is commutates off, the source voltage is still connected to the resonant circuit, nonetheless the capacitor C_1 has been grounded to feed a large part of the resonance currents. Then, the current reflected by the series resonance between the source inductance and Z-source capacitance is considerably reduced [10]. 4) Fourth state begins when current from the inductor continues to flow through the diodes and resistors until the

current decays to zero, 1, 12, 13 and 3, 10, 11. The serial Z-source topology is a solution that effectively addresses several issues present in classic and parallel Z-source topologies. As a result, it has become a fundamental basis for subsequent designs. In the study by Chang [10], the serial Z-source topology was proposed along with two methods for manually tripping the Z-source breaker. These methods involved inducing either an external artificial fault near the output or an internal artificial fault within the Z-source breaker.

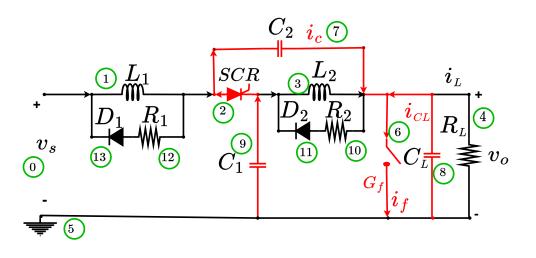


Figure 3.4: Series connected Z-source^[10]

Alternative classical Z-source topology

This topology is is depicted in Figure 3.5. It is composed of two SCRs, three capacitors (C_1) , $(C_2), (C_3),$ Four inductors $(L_1), (L_2), (L_3), (L_4)$ in parallel with diodes $(D_1), (D_2), (D_3), (D_4)$ and resistors $(R_1),(R_2),(R_3)$ (R_4) series array. Assuming that inductors L_1, L_2, L_3 and L_4 , capacitors C_1 , C_2 and C_3 , diodes D_1 , D_2 , D_3 , D_4 and resistors R_1 , R_2 , R_3 , R_4 have the same values L, C, D, R respectively. The circuit breaker is between the voltage source (v_s) and load that is composed by a capacitor (C_L) and a resistor (R_L) . G_f is the conductance used to simulate the fault in the load. The aim of this topology is to improve the fault removal speed of Z-source circuit breaker. This topology maintains the problems that can arise from the lack of a shared point between the source and the load. In addition, this topology uses two SCRs for commutation. This topology has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCRs, inductors and load are equal in steady state to i_L current. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4, 5, 6, and 7; this circuit consists of the source, inductor L_1 , SCR_2 , inductor L_2 load, inductor L_3 , SCR_1 and inductor L_4 In this state, capacitors C_1 are also charged with the source voltage, capacitors C_2 and C_3 are discharged, they behave as an open circuit. 2) Second state is the transient state or fault occurrence state. When a a fault occurs in 10, the fault current is supplied by the capacitors C_1 , C_2 and C_3 in series and C_L . The series capacitors form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitors, SCRs and fault, following the red line through 12, 6, 8, 2, 9, 10, and 11. Note that the current i_c passes through SCR_1 and SCR_2 , which gives two

possibilities of interruption. please see Figure 3.5. High frequency current of the capacitors increases until is equal to the low frequency current through the inductors i_L , then the SCR is reverse biased and commutates off. 3) Third state corresponds to resonance series condition. It is composed of the voltage source v_s , three capacitors C_1 , C_2 , C_3 and Four inductors L_1, L_2, L_3 and L_4 . After SCR is turned off, three series LC circuits are connected to the fault and load through 0, 1, 9; 5, 8, 3 and 7, 12 initiating an LC resonance series. The components involved in series resonance have increased, resulting in higher snubbing resistances compared to the traditional Z-source. Resonance ends when the voltage on the inductors begins to turn negative. 4) Fourth state begins when current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 1, 13, 14: 3, 17, 18; 7, 15, 16 and 5, 19, 20. The energy stored in the inductor is dissipated across the resistor. The following comparison analysis, presented in [35], demonstrates that the fault currents and fault clearing times of this topology are superior to those of the classical. series, and parallel topologies. During the commutation time, this topology exhibits lower fault times and fault current, reduced the fault time by approximately (0.2ms). However, it is important to note that the addition of one SCR in the conduction path will result in increased losses. The results are validated by simulation for 6.000V medium voltage and low voltage prototype.

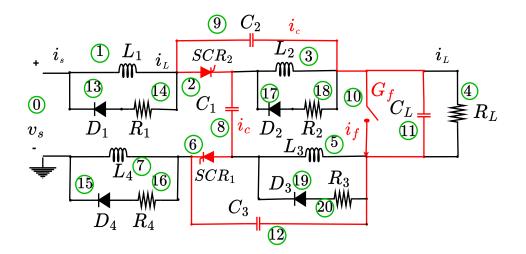


Figure 3.5: Alternative classical Z-source topology [35]

Series Z-source topology with response to load variations

One challenge of the Z-source to withstand load current peaks that are not caused by faults. This is evident in situations such as motor start-up, where currents can surge to 10-15 times their rated current [52], or when loads are being switched within a DC microgrid. Series Z-source topology with response to load variations are depicted in Figure 3.6. It is composed of the SCR, three capacitors (C_1) , (C_2) and (C_3) , two resistor (R_1) , (R_2) , in series with C_1 and C_2 respectively, two inductors (L_1) , (L_2) in parallel with the diodes (D_1) , (D_2) and the resistor (R_3) (R_4) series array. This topology is between the voltage source (v_s) and load composed of a capacitor (C_L) and a resistor (R_L) . G_f is the conductance used to simulate the fault in the load. The aim of this topology is to add to the Z-source series a capacitor C_1

28

to supply sudden load changes or peaks that are not fault overcurrents, avoiding the SCR commuting off. Resistors in series with the capacitors R_1 , R_2 are sized to limit the fault currents. These resistors also serves for fault detection. This topology has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCR, inductors L_1, L_2 and load are equal in steady state to i_L current. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4; this circuit consists of the source, L_1 , the SCR, L_2 and load. In this state, capacitors C_1 and C_2 are also charged with the source voltage and C_3 is discharged, they behave as an open circuit; please see Figure 3.6. 2) Second state is the transient state or fault occurrence state. This topology provides two important high-frequency paths: paths 15, 16, 8 and 4, which supply the abrupt load changes without the SCR commutates to off, which consists of R_1, C_1, C_3 and load C_L, R_L . On the other hand, path 14, 7, 2, 8, 6, 9 commutates the SCR off when a fault occurs in 6, which consisting of R_2, C_2, SCR, C_3, C_L . Since the current from C_1 does not pass through the SCR, the values of R_1 and C_1 can be modified to supply several steps of the steady state current [53].3) Third state corresponds to resonance series condition. It is composed of the voltage source v_s , three capacitors C_1 , C_2 , C_3 and two inductors L_1 , L_2 ; After SCR is turned off, two series LC circuits are connected to the fault and load through 0, 1, 8, 16 and 12, 7, 3 initiating an LC resonance series. 4) Fourth state begins when current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 1, 11, 10 and 3, 12, 13. The energy corresponding to values of the inductor voltage is dissipated in the resistor. This topology was proposed in [53], and it yielded good results even under load current changes up to three times the steady-state value. The system was simulated for medium voltage, and a low-voltage prototype was used for experimental validation. Furthermore, a modified proposal was presented where the resistors R1 and R2 were replaced with inductors in parallel with diodes, vielding similar results.

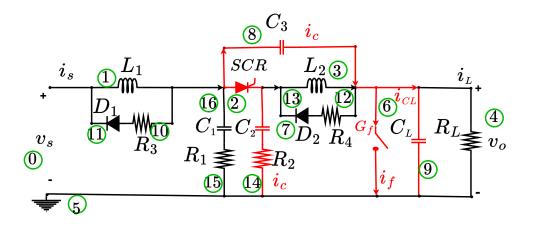


Figure 3.6: Series connected Z-source with response to load variations [53]

3.2.2Topologies with magnetic couplings

Initially, the use of magnetic couplings was proposed for Z-source topologies to reduce the weight and size of the switching circuit. However, it was discovered that magnetic coupling

could be used within the commutation path [79, 63], which allowed for a reduction in the number of capacitors in the topologies. This section describes the behavior of unidirectional topologies with magnetic coupling to reduce the size and weight of the circuit breaker, as well as topologies that use magnetic coupling as a path of fault clearance.

Classic Z-source using magnetic coupling

Classic Z-source using magnetic coupling is depicted in Figure 3.7. It is composed of the SCR, two capacitors (C_1) , (C_2) two coupled inductors (L_{m1}) , (L_{m2}) in parallel with diodes (D_1) , (D_2) and resistors $(R_1), (R_2)$ series array. Assuming that inductors L_1 and L_2 , capacitors C_1 and C_2 , diodes D_1 and D_2 and resistors R_1 and R_2 have the same values L, C, D, Rrespectively. Classic Z-source using magnetic coupling is between the voltage source (v_s) and load composed of a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault conductance in the load. The aim of use coupled inductors on this topology is to reduce the size and weight of the classic Z-source. Coupled inductors use the same number of turns. The current in each inductor is the same. Then the inductors voltages L_{m1} and L_{m2} are equal and the inductance value is halved. This allows the inductor weight to be reduced by 30%. Moreover, the size of the inductor can be reduced by 50%. Classic Z-source using magnetic coupling has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCR, inductors L_{m1} , L_{m2} and load are equal in steady state to (i_L) current. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4 which consists of the source, the SCR, inductor L_{m1} , Load and L_{m2} ; in this state, capacitors C_1 and C_2 are also charged with the source voltage and they behave as an open circuit. 2)Second state is the transient state or fault occurrence state. When a a fault occurs in 6, the fault current is supplied by the capacitors C_1, C_2 in series and C_L . The series capacitors C_1 , C_2 and C_L form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitors C_1 , C_2 and SCR following the red line through 9, 6, 8, and 1 in the direction of the source; please see Figure 3.7. High frequency current of the capacitors increases until is equal to the low frequency current through the inductors i_L), then the SCR is reverse biased and commutates off. 3) Third state, after SCR is turned off, two series LC circuits are connected to the fault and load through 2, 8, and 4, 9; initiating an LC resonance series. 4) Fourth state begins when the voltage on the capacitor decays to zero after the resonance has ended. Current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 2, 7, 8 and 4, 10, 11. The energy corresponding to values of the inductor voltage is dissipated in the resistor [43].

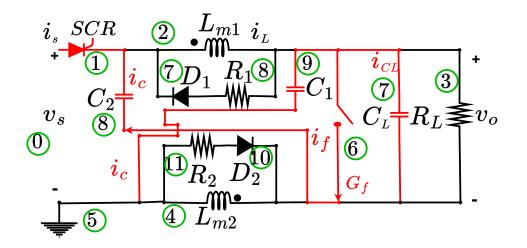


Figure 3.7: Classic Z-source using magnetic coupling [43]

Series Z-source using magnetic coupling

Series connected Z-source using magnetic coupling is depicted in Figure 3.8. It is composed of a SCR, two capacitors (C_1) , (C_2) two coupled inductors $(L_{m1}), (L_{m2})$ in parallel with diodes (D_1) , (D_2) and resistors (R_1) , (R_2) series array. Assuming that inductors L_{m1} and L_{m2} capacitors C_1 and C_2 , diodes D_1 and D_2 and resistors R_1 and R_2 have the same values L_m , C, D, R respectively. Series connected Z-source using magnetic coupling is between the voltage source (v_s) and load that is composed by a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault in the load. The aim of the series-connected Z-source using magnetic coupling topology is to reduce the size and weight of the series Z-source while preserving the main commutation characteristics. Coupled inductors use the same number of turns. The current in each inductor is the same. Then the inductors voltages L_{m1} and L_{m2} are equal and the inductance value is halved and the same reduction in size and volume as the Classic Z-source topology using magnetic coupling is obtained. Series-connected Z-source using magnetic coupling topology has four operating states that are described as follows:) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L . The currents of the source, SCR, inductor and load are equal in steady state to i_L . The current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4; this circuit consists of the source, the SCR, inductors and load. In this state, capacitors C_1 and C_2 are also charged with the source voltage and they behave as an open circuit. 2) Second state is the transient state or fault occurrence state. When a a fault occurs in 6, the fault current is supplied by the capacitors C_1 and C_2 in series and C_L . The series capacitors C_1 and C_2 and C_L form a capacitive voltage divider. Current i_c passes through the high-frequency circuit, formed by the capacitors and SCR following the red line through 17, 2, 8, 5, and 6; please see Figure 3.8. High frequency current of the capacitors increases until is equal to the low frequency current through the inductors i_L , then the SCR is reverse biased and commutates to off. 3) Third state corresponds to resonance series condition. It is composed of the voltage source v_s , two capacitors (C) and two inductors L. After SCR is turned off, two series LC circuits are connected to the fault and load through 0, 1, 8 and 7, 3,

8 initiating an LC resonance series. Note that in this topology after the SCR is commutates off, the source voltage is still connected to the resonant circuit, nonetheless the capacitor C_1 has been grounded to feed a large part of the resonance currents. Then, the current reflected by the series resonance between the source inductance and Z-source capacitances is considerably reduced [10]. 4) Fourth state begins when current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 1, 7, 8 and 3, 9, 10. The energy corresponding to values of the inductor voltage is dissipated in the resistor.

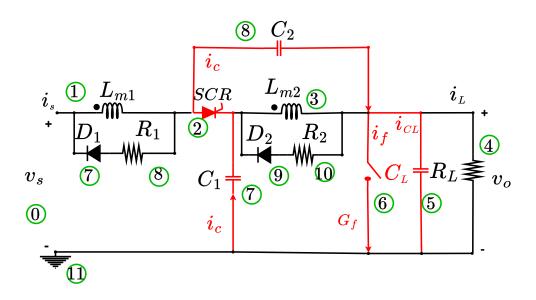


Figure 3.8: Series Z-source using magnetic coupling [43]

Classic connected Z-source using magnetic coupling with reduced capacitance

Classic connected Z-source using magnetic coupling with reduced capacitance is depicted in Figure 3.9. It is composed of the voltage source (v_s) , the SCR, one capacitors (C), two coupled inductors (L_{m1}) , (L_{m2}) in parallel with diodes (D_1) , (D_2) and resistors (R_1) , (R_2) series array. Assuming that diodes D_1 and D_2 and resistors R_1 and R_2 have the same values D, R respectively. Classic connected Z-source using magnetic coupling with reduced is between the voltage source v_s and load composed of a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault conductance in the load. The aim of this topology is to take advantage of the magnetic coupling for fault interruption and reduce the number of capacitors required and inductors with regard to Classic Z-source. In order to achieve this, it was necessary to include the magnetic coupling in the SCR commutation path. Classic Z-source using magnetic coupling topology depicted in Figure 3.9. This topology has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L , C_L and the current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4 which consists of the source v_s , the SCR, coupled inductors L_{m1} , load, L_{m2} and load; in this state capacitor C is charged by the source voltage and behaves as an open circuit 2) Second state is the transient state or fault occurrence state. In this state, the commutation path is 6, 2, 4, 8, and 1 composed of the inductor L_{m1} , inductor L_{m2} , capacitor C and SCR. When a fault occurs in 6 the instantaneous

large current i_{Lm1} flows through L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, voltage in Lm1 undergoes a sudden increase. Voltage on the inductor Lm1 induces a voltage on the inductor L_m2 through mutual inductance and drives current i_{Lm2} equal to i_c through the capacitor C; please see Figure 3.9 in red color. Capacitor current i_c grows and matches the inductor steady-state current i_L and the SCR commutates off [43, 53]. Note that the value of the i_{Lm2} current can be sized for changes in the load by modifying the transformation ratio of the magnetic coupling. 3) Third state, after SCR is turned off, series LC circuits are connected to the fault and load through 2, 8, and 6; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor Lm1 matches the voltage across the capacitor C. The behavior in this state is similar to that of the classical Z-source. The resonance ends when the voltages in the inductor tend to become negative. 4) Fourth state begins when the voltage on the capacitor decays to zero after the resonance has ended. Current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 2, 9, 10 and 4, 11, 12. The energy corresponding to values of the inductor voltage is dissipated in the resistor .The reduction of one of the capacitors implies a reduction of the resonance time. 53.

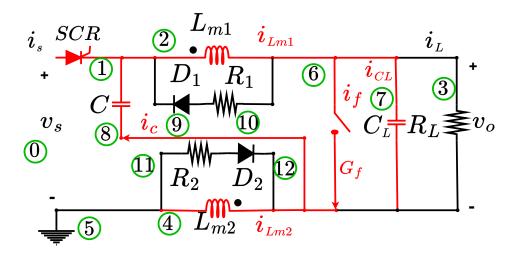


Figure 3.9: Classic connected Z-source using magnetic coupling with reduced capacitance^[53]

T-source topology

This topology was proposed in [53] as Series Z-source connected using magnetic coupling with reduced capacitance and proposed in [83] as T-source topology. This topology is depicted in Figure 3.10 .It is composed of the source (v_s) , a SCR, one capacitors (C), two coupled inductors (L_{m1}) , (L_{m2}) in parallel with diodes (D_1) , (D_2) and resistors (R_1) , (R_2) in series array. Assuming that diodes D_1 and D_2 and resistors R_1 and R_2 have the same values D, R respectively. This topology is between the voltage source (v_s) and load composed of a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault conductance in the load. The aim of this topology is to take advantage of the magnetic coupling for fault interruption and reduce the number of capacitors required and inductors

33

topology is depicted in Figure 3.10. This topology has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L , and the current passes through the low-frequency circuit composed of 0, 1, 2, 3, and 4 which consists of the source v_s , the SCR, inductor L_{m2} , the SCR, inductor L_{m1} and load; in this state, capacitor C is charged with the source voltage and it behave as an open circuit. 2) Second state is the transient state or fault occurrence state. In this state, the commutation path is 6, 3, 1, 7, and 2 composed of the inductor L_{m1} , inductor L_{m2} , capacitor C and the SCR. When a fault occurs in 6, the instantaneous large current i_{Lm1} flows through L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, voltage in Lm1 undergoes a sudden increase. Voltage on the inductor Lm1 changes polarity and induces a voltage on the inductor L_m2 through mutual inductance and drives current i_{Lm2} equal to i_c through the capacitor C; please see Figure 3.10 in red color. The capacitor current i_c grows and matches the inductor steady-state current i_L and the SCR commutates off [43, 53]. i_{Lm2} can be sized for changes in the load by modifying the transformation ratio of the magnetic coupling.3) Third state, after SCR is turned off, series LC circuits are connected to the fault and load through 3 and 7; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductors L_{m1} matches the voltage across the capacitor C. When capacitor voltage is reached by the inductor voltage; the voltage at the output v_0 becomes zero due to the disconnection of the source. The behavior in this state is similar to that of the series Z-source. The resonance ends when the voltages in the inductor tend to become negative. 4) Fourth state begins when the voltage on the capacitor decays to zero after the resonance has ended. Current from the inductor continues to flow through the diodes and resistors until the current decays to zero, 1, 8, 9 and 3, 10, 11. The energy corresponding to values of the inductor voltage is dissipated in the resistor [53].

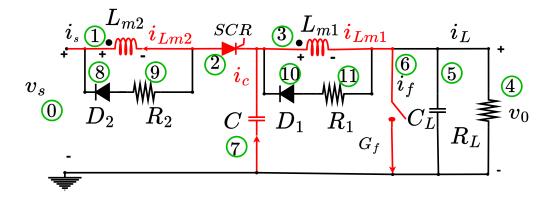


Figure 3.10: T-source topology [53]

τ -source topology

This topology is depicted in Figure 3.11. This topology is referred to as "tau-source" due to the fact that the coupled inductors are configured in the shape of the Greek letter tau. It is composed of the voltage source (v_s) , the SCR, one capacitor (C), two coupled inductors

 $(L_{m1}), (L_{m2})$, one diode (D) and a resistor (R). This topology is between the voltage source v_s and load composed of a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault conductance in the load. The aim of this topology is to take advantage of magnetic coupling for fault interruption and to reduce the number of elements regard to classical, parallel and series z-source topologies while preserving the natural commutation of the SCR please see Figure 3.11. This topology has four operating states that are described as follows: 1)First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L , and the current passes through the low-frequency circuit composed of 0, 1, 2, and 3 which consists of the source v_s , the SCR, coupled inductors L_{m1} , L_{m2} and load; in this state, capacitor C is charged with the source voltage and they behave as an open circuit. 2) Second state is the transient state or fault occurrence state. In this state, the commutation path is 4, 2, 5, 6, 8, and 1 composed of inductor L_{m1} , inductor L_{m2} , capacitor C, and the SCR. When a fault occurs in 6 the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, the voltage v_{Lm1} undergoes a sudden increase. Voltage on the inductor v_{Lm1} induces a voltage on the inductor L_m2 through mutual inductance and drives current i_{Lm2} equal to i_c through the capacitor C; please see Figure 3.11 in red color. The capacitor current i_c grows and matches the inductor steady-state current i_L and the SCR commutates to off [11]. i_{Lm2} can be sized for changes in the load by modifying the transformation ratio of the magnetic coupling. 3) Third state, after turning off the SCR, the series LC circuits are connected to the fault and load through 6, 5, and 2; initiating an LC resonance series when the voltage across the capacitor v_c matches the voltage across v_{Lm2} , which occurs in a given time, generating an increase voltage. The resonance ends when voltages in the inductor tend to become negative 4) The fourth state begins when the voltage on the capacitor starts to decay. It is important to say that the current pulse supplied by the capacitor is transported by the inductor current iL_{m2} . Then the current i_{lm2} decays rapidly to zero as the capacitor current decays [92].

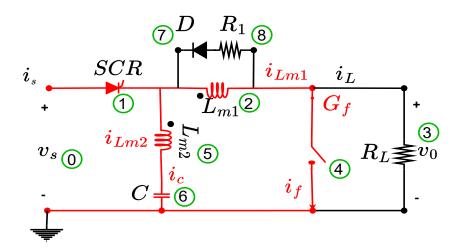


Figure 3.11: τ -source topology[92]

O-Z-source topology

This topology is depicted in Figure 3.12. It is composed of the voltage source (v_s) , the SCR, capacitors (C), two coupled inductors $(L_{m1}), (L_{m2})$ one diode (D) and one resistors (R). This topology is between the voltage source (v_s) and load composed of a capacitor (C_L) and a resistor (R_L) . (G_f) is the conductance used to simulate the fault conductance in the load. The aim of this topology is to preserve the advantages including natural commutation of the SCR, reduced fault current reflection, symmetrical fault current level setting and a common connection between the power supply and the load. It can also be configured for bi-directional operation. please see Figure 3.12. This topology has four operating states that are described as follows: 1) First estate corresponds to steady-state operation, the source v_s delivers energy to the load R_L , and the current passes through the low-frequency circuit composed of 0, 1, 2, and 3 which consists of the source v_s , the SCR, coupled inductors L_{m2} and load; in this state, capacitor C keeps uncharged and it has as an open circuit. 2) Second state is the transient state or fault occurrence state. In this state, the commutation path is 4, 5, 6, 2, and 1, composed of the inductor L_{m1} , the capacitor C, inductor L_{m2} , and the SCR. When a fault occurs in 4 the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, voltage on Lm1 undergoes a sudden increase. Voltage on the inductor Lm1induces a voltage on the inductor L_m^2 through mutual inductance and drives current i_{Lm^2} equal to i_c through the capacitor C; please see Figure 3.12 in red color. The capacitor current i_c grows and matches the inductor steady-state current i_L and the SCR commutates off [93]. i_{Lm2} current can be sized for changes in the load by modifying the transformation ratio of the magnetic coupling. 3) Third state, after turning off the SCR, the series LC circuits are connected to the fault and load through 6, 5, and fault; initiating an LC resonance series when the voltage across the capacitor v_c matches the voltage across v_{Lm1} , which occurs in a given time, generating an increase in voltage. The resonance ends when voltages in the inductor tend to become negative. It is important to add that the inductance participates in the resonance state, which represents a risk for the source. 4) The fourth state begins when the voltage on the capacitor starts to decay. It is important to say that the current pulse supplied by the capacitor is transported by the inductor current iL_{m1} . Then the current i_{lm1} decays rapidly to zero as the capacitor current decays. Energy stored in L_{m2} is dissipated by the resistor.

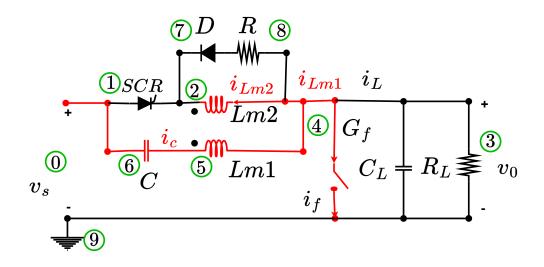


Figure 3.12: O-Z-source topology [93]

3.3 Bi-directional topologies

One of the characteristics of DC microgrids is their greater compatibility with renewable energy sources [62]. In fact, in cases where there are several sources feeding the DC microgrid, the protections must act in a bidirectional way. The following is a description of bidirectional topologies which retain the main commutation characteristics of Z-source topologies in the event of an overcurrent fault.

3.3.1 Topologies without magnetic couplings

Bi-directional topology based on the classic Z-source

Bi-directional topology based on the classic Z-source is depicted in Figure 3.13. It is composed of four capacitors $(C_1), (C_2), (C_3), (C_4)$ four diodes $(D_1), (D_2), (D_3), (D_4)$, two SCRs $(SCR_1), (SCR_2), \text{ four inductors } (L_1), (L_2), (L_3), (L_4) \text{ and four resistors } (R_1), (R_2), (R_3),$ (R_4) . Assuming that inductors inductors L_1, L_2, L_3, L_4 , capacitors C_1, C_2, C_3, C_4 , diodes D_1, D_2, D_3, D_4 , and resistors R_1, R_2, R_3, R_4 have the same values L, C, D, R respectively. Points A or B can be source or load. (G_f) is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows:1) First estate corresponds to steady-state operation, current follows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3 and 4, which consists of the source in A, inductors L_1 , L_2 the SCR_1 and load in B; in this state, capacitors C1, C_2 , C_3 , and C_4 are loaded with the source voltage and they behave as an open circuit. The currents of the source A, SCR_1 , inductors L_1 , L_2 and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current follows in the forward direction B to A. The current passes through the low-frequency circuit composed of 4, 3, 5, 1, and 0, which consists of the source

37

in B, inductors L_1 and L_2 , the SCR_2 , and load in A. The currents of the source B, SCR_2 , inductors L_1 and L_2 and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence in B. When a fault i_f occurs in B, the fault current is supplied by the capacitors C4 and C_2 . Current i_{ca} passes through the high-frequency circuit formed by the capacitors C4, C_2 and SCR_1 which follows the red line through 6, 4, 7, and 2 in the direction to A; please see Figure 3.13. High frequency current of the capacitors C4 and C_2 increases until is equal to the low frequency current through the inductors i_{La} , then the SCR_1 is reverse biased and commutates off. 4) Fourth state is the transient state or fault occurrence in A. When a fault occurs in A, the fault current is supplied by capacitors C1and C_3 . Current i_{cb} passes through the high-frequency circuit formed by capacitors C1 and C_3 , SCR_2 and D_2 following the red line through 0, 8, 9, and 2 in the direction to B; please see Figure 3.13. High frequency current of the capacitors C1 and C_3 increases until is equal to the low frequency current through the inductors i_{Lb} , then the SCR_2 is reverse biased and commutates off. 5) Fifth state: after SCR_1 is turned off by a fault in B, two series LC circuits are connected to the fault and load through 6, 13 and 7, 3; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor v_{L1} matches the voltage across the capacitor v_{C1} . When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_B becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_1 becomes negative. The resonance ends when voltages in the inductor tend to become negative. 6) Sixth state: after SCR_2 is turned off by a fault in A, two series LC circuits are connected to the fault and load through 9, 10 and 8, 1; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor v_{L1} matches the voltage across the capacitor v_{C3} . When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_A becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_2 becomes negative. The resonance ends when voltages in the inductor tend to become negative. 7) Seventh state begins when the voltage on the capacitors C_2 decays to zero after the resonance has ended for load in B. Current from the inductors L_2 and L_4 continues to flow through the diodes D_2 , D_4 and resistors R_2 , R_4 respectively until the current decays to zero, 3, 16, 17 and 13, 14, 15. The energy corresponding to values of the inductor voltage is dissipated in the resistor. 8) Eight state begins when the voltage on the capacitors C_3 decays to zero after the resonance has ended for load in A. Current from the inductors L_1 and L_3 continues to flow through the diodes D_1 , D_3 and resistors R_1 , R_3 respectively until the current decays to zero, 1, 18, 19 and 10, 11, 12. The energy corresponding to negative values of the inductor voltage is dissipated in the resistor. Note that this topology has all the advantages and disadvantages of the classic Z-source topology. However, it can work in both forward and reverse directions [72].

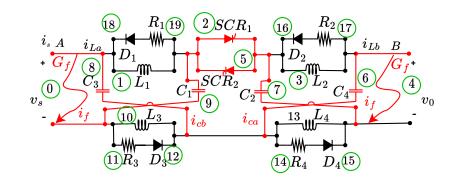


Figure 3.13: Bi-directional topology based on the classic Z-source [72]

Bi-directional topology based on the series Z-source

Bi-directional topology based on the series Z-source is depicted in Figure 3.14. It is composed of two capacitors (C_1) and (C_2) , six diodes (D_1) , (D_2) , (D_3) , (D_4) , (D_5) and (D_6) , one SCR, two inductors (L_1) and (L_2) , two resistors (R_1) and (R_2) . Assuming that inductors inductors L_1 , (L_2) , capacitors C_1 , C_2 , diodes D_1 , D_2 , D_3 , D_4 , D_5 , D_6 and resistors R_1 , R_2 , have the same values L, C, D, R respectively. Points A or B can be source or load. (G_f) is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current follows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4, 5 and 6 which consists of the source in A, the diode D_1 , inductor L_1 , the SCR, inductor L_2 , diode D_2 and load in B; in this state, capacitors C_1 is charged at source voltage and C_2 is discharged they behave as an open circuit. The currents of the source A, inductor L_1 , SCR, inductor L_2 and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current follows in the forward direction B to A. The current passes through the low-frequency circuit composed of 6, 7, 3, 4, 8 and load, which consists of the source in B, D_3 inductors L_1 , the SCR, L_2 , D_4 and load in A. The currents of the source B, L_1 , SCR, L_2 and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence state in B. When a fault occurs in B, the fault current is supplied by the capacitors C_1 and C_2 . Current i_{ca} passes through the high-frequency circuit, formed by the capacitors C1, SCR and C_2 , and D_5 following the red line through 6, 11, 12, and 5 in the direction to B; please see Figure 3.14. High frequency current i_{ca} of the capacitors C_1 and C_2 increases until is equal to the low frequency current through the inductors i_{La} , then the SCR is reverse biased and commutates off. 4) Fourth state is the transient state or fault occurrence state in A. When a fault occurs in A, the fault current is supplied by the capacitors C_1 and C_2 . Current i_{cb} passes through the high-frequency circuit, formed by the capacitors C_1 , the SCR, C_2 and D_4 following the red line through 0, 11, 3, 12, 8, in the direction to A; please see Figure 3.14. High frequency current i_{cb} of the capacitors C_1 and C_3 increases until is equal to the low frequency current through the inductors i_{Lb} , then the SCR is reverse biased and commutates off. Note that the path used by the circuit breaker in the forward or reverse direction is the same, which means it utilizes the same elements for commutation. This allows for a

39

reduction in the number of elements while preserving the bidirectional behavior. 5) Fifth state, after SCR is turned off by a fault in A, two series LC circuits are connected to the fault and load through 2, 12 and 4, 11; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor v_{L2} matches the voltage across the capacitor v_{C1} . When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_B becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR becomes negative. The resonance ends when voltages in the inductor tend to become negative. 6) Sixth state, after SCR is turned off by a fault in B, two series LC circuits are connected to the fault and load through 2, 12 and 4, 11; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor v_{L2} matches the voltage across the capacitor (v_{C1}) . When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_A becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR becomes negative. The resonance ends when voltages in the inductor tend to become negative. 7) Seventh state begins when the voltage on the capacitors decays to zero after the resonance has ended. Current from the inductors L_1 and L_2 continues to flow through the diodes D_5 , D_6 and resistors R_1 , R_2 respectively until the current decays to zero, 2, 13, 5 and 4, 14, 10. The energy corresponding to values of the inductor voltage is dissipated in the resistor. 8) Eighth state begins when the voltage on the capacitors decays to zero after the resonance has ended. Current from the inductors L_3 and L_4 continues to flow through the diodes D_5 , D_6 and resistors R_3 , R_4 respectively until the current decays

to zero, 8, 17, 18 and 6, 19, and 20. The energy corresponding to negative values of the inductor voltage is dissipated in the resistor [67].

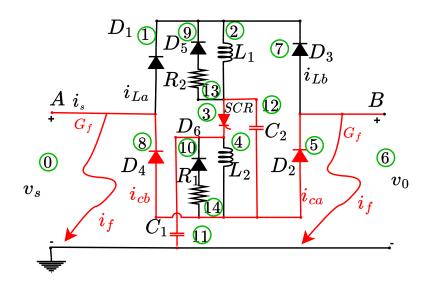


Figure 3.14: Bi-directional topology based on the series Z-source [67]

Bi-directional topology based on the series Z-source

Bi-directional topology based on the series Z-source is depicted in Figure 3.15. This topology requires a control unit with additional elements to refine its behavior after the resonance starts, which are not part of the scope of this study. Therefore, it will only be analyzed up to the series resonance. It is composed of three capacitors $(C_1), (C_2), (C_3)$, two diodes $(D_1), (D_2),$ two SCRs $(SCR_1), (SCR_2),$ two inductors (L_{m1}) and (L_{m2}) . Assuming that inductors inductors L_{m1} and L_{m2} , capacitors C_1, C_2, C_3 , and diodes D_1, D_2 have the same values L, C, D respectively. Points A or B can be source or load. (G_f) is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current follows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4 and 5 which consists of the source in A, inductor L_{m1} , SCR_1 , diode D_2 , inductor L_{m1} load in B; in this state, capacitors C_1 is charged at source voltage, C_2 , C_3 are discharged and behave as an open circuit. The currents of the source A, inductor L_{m2} , SCR_1 , inductor L_{m1} , diode D_2 and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current follows in the forward direction B to A. Current passes through the low-frequency circuit composed of 5, 4, 6, 7, 1 and load, which consists of the source in B, inductor L_{m1} , the SCR_2 , the diode D_1 , inductor L_{m2} , and load in A. The currents of the source B, SCR_2 , inductors L_{m1} and L_{m2} and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence state in B. When a fault occurs in B, the fault current is supplied by capacitors C1 and C₃. The currents of i_{c1} and i_{c3} are equal in transient state to the current i_{ca} passing through the high frequency circuit formed by capacitors C1, the SCR_1 and C_3 , following the red line through 8, 2, 9 and 5 in the direction to B; please see Figure 3.15. Meanwhile C_2 is being charged with from the part of the energy stored in L_{m1} , it subsequently delivers a current pulse in the direction of SCR_1 by following the path 9, 6, 2. High frequency current of i_{ca} increases until is equal to the low frequency current through the inductors i_{La} , then the SCR_1 is reverse biased and commutates off. 4) Fourth state is the transient state or fault occurrence state in A. When a fault occurs in A, the fault current is supplied by capacitors C1 and C₂. Currents of i_{c1} and i_{c2} are equal in transient state to current i_{cb} passing through the high frequency circuit formed by capacitors C1, SCR_2 and C_2 and following the red line through 8, 6, 10 and 0 in the direction to A; please see Figure 3.15. Meanwhile C_3 is being charged with from the part of the energy stored in L_{m2} , it subsequently delivers a current pulse in the direction of SCR_2 by following the path 9, 2, 6. High frequency current of i_{cb} increases until is equal to the low frequency current through the inductors i_{Lb} , then the SCR_2 is reverse biased and commutates off. 5) Fifth state, after SCR_1 is turned off by a fault in A, two series LC circuits are connected to the fault and load through 8, 4, and 5 and 1, 10, 4, 9 composed of C_1 , L_1 and L_{m1} , C_2 , C_3 , L_{m2} initiating a LC series resonance. Series resonance can be observed when the voltage across the inductor v_{Lm1} matches the voltage across the capacitor v_{C1} . the oscillations between L_{m2} , C_3 , C_2 , decay rapidly because they are not connected to the fault. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_B becomes zero due to the disconnection of the source. The resonance ends when voltages in the inductor tend to become negative. 6) Sixth state, after SCR_2 is

turned off by a fault in B, two series LC circuits are connected to the fault and load through 8, 1, and 5 and 1, 10, 4, 9 composed of C_1 , L_{m2} and L_{m1} , C_2 , C_3 , L_{m2} initiating a LC series resonance. Series resonance can be observed when the voltage across the inductor v_{Lm2} matches the voltage across the capacitor v_{C1} . the oscillations between L_{m1} , C_3 , C_2 , decay rapidly because they are not connected to the fault. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_A becomes zero due to the disconnection of the source. The resonance ends when voltages in the inductor tend to become negative [32].

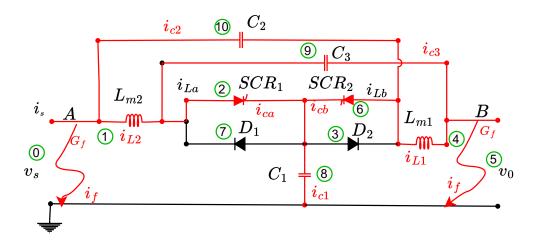


Figure 3.15: Bi-directional topology based on the series Z-source [32]

3.3.2 Topologies with magnetic couplings

This section depict the behavior of bi-directional topologies using magnetic couplings in the commutation path.

Bi-directional topology based on T-source

Bi-directional topology based on T-source is depicted in Figure 3.16. It is composed of one capacitors (C), six diodes (D_1) , (D_2) , (D_3) , (D_4) , (D_5) and (D_6) two SCRs (SCR₁) and (SCR_2) , four coupled inductors (L_{m1}) , (L_{m2}) , (L_{m3}) and (L_{m4}) , four resistors (R_1) , (R_2) , (R_3) and (R_4) . Assuming that inductors L_{m1} , L_{m2} , L_{m3} , L_{m4} , diodes D_1 , D_2 , D_3 , D_4 , D_5 , D_6 , resistors R_1 , R_2 , R_3 , R_4 , have the same values respectively Lm, D, R. Points A or B can be source or load. G_f is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current flows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4 and 5 which consists of the source in A, inductor L_{m2} , SCR_1 , L_{m1} , diode D_5 , and load in B; in this state, capacitor C is charged at source voltage and behave as and open circuit. The currents of the source A, L_{m2} , SCR_1 , L_{m1} , D_4 and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current flows in the forward direction

B to A. The current passes through the low-frequency circuit composed of 5, 6, 7, 8, 9, and 0 which consists of the source in B, inductor L_{m4} , SCR_2 , L_{m3} , D_6 , and load in A. The currents of the source B, L_{m4} , SCR_2 , L_{m3} , D_6 and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence state in B. Current $i_c a$ represents the current of the capacitor C when a fault occurs in B in the transient state. When a fault occurs in B, the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, the voltage on L_{m1} undergoes a sudden increase. Voltage on the inductor L_{m1} induces a voltage on the inductor L_m^2 through mutual inductance and drives current i_{Lm^2} supplied to $i_c a$ through the capacitor C; please see Figure 3.16 in red color. The capacitor current $i_c a$ grows and matches the inductor steady-state current $i_L a$ and the SCR_1 commutates off [72]. 4) Fourth state is the transient state or fault occurrence state in A. Current $i_c b$ represents the current of the capacitor C when a fault occurs in A in the transient state. When a fault occurs in A, the instantaneous large current i_{Lm3} flows through the L_{m3} which is connected to the load. After restoring the steady state, i_{Lm3} has increased slightly. Meanwhile, the voltage in inductor L_{m3} undergoes a sudden increase. Voltage on the inductor L_{m3} induces a voltage on the inductor $L_m 4$ through mutual inductance and drives current i_{Lm4} supplied to $i_c b$ through the capacitor C; please see Figure 3.16 in red color. Capacitor current $i_c b$ grows and matches the inductor steady-state current $i_L b$ and the SCR_2 commutates off. 5) Fifth state begins after SCR_1 is turned off by a fault in A, series LC circuits are connected to the fault and load through 10, 3 and fault; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor Lm1 matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; voltage at the output v_B becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_1 becomes negative. The resonance ends when voltages in the inductor Lm1 tend to become negative. 6) Sixth state begins after SCR_2 is turned off by a fault in B, series LC circuits are connected to the fault and load through 8, 10 and fault; initiating an LC series resonance. Series resonance can be observed when the voltage across the inductor Lm3 matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; voltage at the output v_A becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, voltage across the SCR_2 becomes negative. The resonance ends when voltages in the inductor Lm3 tend to become negative. 7) Seventh state begins when the voltage on the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 , D_2 and resistors R_1 , R_2 respectively until the current decays to zero, 1, 18, 17 and 3, 11, 12. The energy corresponding to values of the inductor voltage is dissipated in the resistor. 8) Eighth state begins when the voltage on the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m3} and L_{m4} continues flowing through diodes D_3 , D_4 and resistors R_3 , R_4 respectively until the current decays to zero, 8, 15, 16 and 6, 13, 14. $\overline{72}$

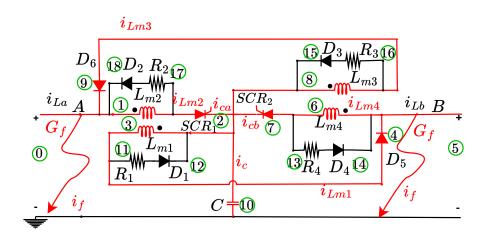


Figure 3.16: Bi-directional topology based on T-source [72].

Bi-directional topology based on T-source

Bi-directional topology based on T-source is depicted in Figure 3.17. It is composed of one capacitor (C), four diodes (D_1) , (D_2) , (D_3) , (D_4) , two SCRs (SCR_1) and (SCR_2) , two coupled inductors (L_{m1}) and (L_{m2}) , and two resistors (R_1) and (R_2) . Assuming that inductors inductors L_{m1} , L_{m2} , diodes D_1 , D_2 , D_3 , D_4 , resistors R_1 , R_2 have the same values respectively Lm, D, R. Points A or B can be source or load. G_f is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current flows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4, and 5 which consists of the source in A, SCR_1 , L_{m2} , L_{m1} , D_3 , and load in B; in this state, capacitor C is charged at source voltage and behave as an open circuit. The currents of the source A, SCR_1 , L_{m2} , L_{m1} , D_3 and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current flows in the forward direction B to A. The current passes through the low-frequency circuit composed of 5, 6, 2, 3, 7, and 0 which consists of the source in B, SCR_2 , L_{m2} , L_{m1} , D_4 , and load in A. The currents of the source B, SCR_2 , L_{m1} , L_{m3} , D_4 and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence state in B. Current $i_c a$ represents the current of the capacitor C when a fault occurs in B in the transient state. When a fault occurs in B, the instantaneous large current i_{Lm1} flows through L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, voltage on L_{m1} undergoes a sudden increase. Voltage in the inductor L_{m1} induces a voltage in the inductor L_{m2} through mutual inductance and drives current i_{Lm_2} supplied to i_{ca} through the capacitor C; please see Figure 3.17 in red color. The capacitor current i_{ca} grows and matches the inductor steady-state current i_{La} and the SCR_1 commutates of i_4) Fourth state is the transient state or fault occurrence state in A. Current i_{cb} represents the current of the capacitor C when a fault occurs in A in the transient state. When a fault occurs in A, the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After

restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, voltage in inductor L_{m1} undergoes a sudden increase. Voltage in the inductor L_{m1} induces a voltage in the inductor L_{m2} through mutual inductance and drives current i_{Lm2} supplied to i_{cb} through the capacitor C; please see Figure 3.17 in red color. The capacitor current i_{cb} grows and matches the inductor steady-state current i_{Lb} and SCR_2 commutates off [87]. 5) Fifth state begins after SCR_1 is turned off by a fault in A, series LC circuits are connected to the fault and load through 8, 3 and fault; initiating an LC series resonance. Series resonance can be observed when voltage across the inductor Lm1 matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_B becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_1 becomes negative. The resonance ends when voltages in inductor L_{m1} tend to become negative. 6) Sixth state begins after SCR_2 is turned off by a fault in B, series LC circuits are connected to the fault and load through 8, 3 and fault; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor L_{m1} matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_A becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_2 becomes negative. The resonance ends when voltages in the inductor L_{m1} tend to become negative. (7) Seventh state begins when the voltage on the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 , D_2 and resistors R_1 , R_2 respectively until the current decays to zero, 2, 9, 10 and 3, 11, 12. The energy corresponding to values of the inductor voltage is dissipated in the resistor. 8) Eighth state begins when the voltage in the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 , D_1

ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 , D_1 and resistors R_1 , R_2 respectively until the current decays to zero, 2, 9, 10 and 3, 11, 12[87].

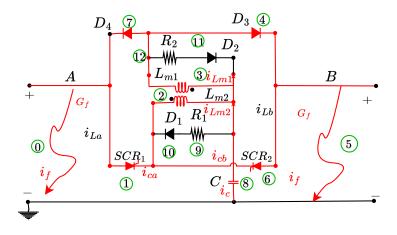


Figure 3.17: Bi-directional topology based on T-source [87]

Bi-directional topology based on T-source

Bi-directional topology based on T-source is depicted in Figure 3.18. It is composed of one capacitor (C), six diodes (D_1) , (D_2) , (D_3) , (D_4) , (D_5) , (D_6) two SCRs (SCR_1) , (SCR_2) , two

inductors L_{m1} , L_{m2} , diodes D_1 , D_2 , D_3 , D_4 , D_5 , D_6 , resistors R_1 , R_2 , R_3 , R_4 have the same values respectively Lm, D, R. Points A or B can be source or load. G_f is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current flows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4 and 5 which consists of the source in A, the SCR_1 , inductors L_{m2} , L_{m1} , diode D_2 , and load in B; in this state, capacitor C is charged at source voltage and behave as an open circuit. The currents of the source A, L_{m2} , SCR_1, L_{m1}, D_2 and load are equal in steady state to (i_{La}) . 2) Second state corresponds to steady-state operation, current follows in the forward direction B to A. The current passes through the low-frequency circuit composed of 5, 6, 3, 2, 7, and 0 which consists of the source in B, inductor L_{m1} , L_{m2} , diode D_1 , and load in A. The currents of the source B, SCR_2 , L_{m1} , L_{m2} , D_1 and load are equal in steady state to i_{Lb} . (3) Third state is the transient state or fault occurrence state in B. Current $i_c a$ represents the current of the capacitor C when a fault occurs in B in the transient state. When a fault occurs in B, the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, the voltage in L_{m1} undergoes a sudden increase. Voltage in inductor L_{m1} induces a voltage in inductor L_m2 through mutual inductance and drives current i_{Lm2} supplied to $i_c a$ through the capacitor C; please see Figure 3.18 in red color. The capacitor current $i_c a$ grows and matches the inductor steady-state current $i_L a$ and the SCR_1 commutates off. 4) Fourth state is the transient state or fault occurrence state in A. Current $i_c b$ represents the current of the capacitor C when a fault occurs in A in the transient state. When a fault occurs in A, the instantaneous large current i_{Lm2} flows through the L_{m2} which is connected to the load. After restoring the steady state, i_{Lm2} has increased slightly. Meanwhile, voltage in inductor L_{m2} undergoes a sudden increase. Voltage in the inductor L_{m2} induces a voltage in the inductor L_m1 through mutual inductance and drives current i_{Lm1} supplied to $i_c b$ through the capacitor C; please see Figure 3.18 in red color. Capacitor current $i_c b$ grows and matches the inductor steady-state current $i_L b$ and the SCR_2 commutates off [78]. 5) Fifth state begins after SCR_1 is turned off by a fault in B, series LC circuits are connected to the fault and load through 8, 3 and fault; initiating an LC series resonance. Series resonance can be observed when the voltage across the inductor Lm1 matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_B becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_1 becomes negative. The resonance ends when voltages in the inductor L_{m1} tend to become negative. 6) Sixth state begins after SCR_2 is turned off by a fault in A, series LC circuits are connected to the fault and load through 8, 2 and fault; initiating an LC resonance series. Series resonance can be observed when the voltage across the inductor L_{m2} matches the voltage across the capacitor C. When the capacitor voltage is reached by the inductor voltage; the voltage at the output v_A becomes zero due to the disconnection of the source. When the resonant voltage of the inductor and capacitor reach half the source voltage, the voltage across the SCR_2 becomes negative. The resonance ends when voltages in inductor L_{m2} tend to become negative. 7) Seventh state begins when

the voltage in the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_3 , D_4 , D_5 , D_6 and resistors R_1 , R_2 , R_3 , R_4 , respectively until the current decays to zero, 2, 9, 10 and 3, 11, and 12, 13, 14, 15, and 16. The energy corresponding to values of the inductor voltage is dissipated in the resistor. 8) Eighth state begins when the voltage in the capacitors decays to zero after the resonance has ended. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_3 , D_4 , D_5 , D_6 and resistors R_1 , R_2 , R_3 , R_4 , respectively until the current decays to zero, 2, 9, 10 and 3, 11, and 12, 13, 14, 15, and 16[78].

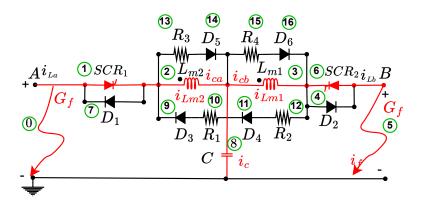


Figure 3.18: Bi-directional topology based on T-source [78]

Bi-directional topology based on T-source

Bi-directional topology based on T-source is depicted in Figure 3.19. It is composed of one capacitor (C), two diodes (D_1) and (D_2) , four SCRs (SCR_1) , (SCR_2) , (SCR_3) , (SCR_4) , two coupled inductors (L_{m1}) , (L_{m2}) , three resistors (R_1) , (R_2) and (R_3) . Assuming that inductors inductors L_{m1} , L_{m2} , diodes D_1 , D_2 , resistors R_1 , R_2 , R_3 have the same values respectively Lm, D, R. Points A or B can be source or load. G_f is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current flows in the forward direction A to B. The current passes through the low-frequency circuit composed of 0, 1, 2, 3 and 4 which consists of the source in A, inductor L_{m2} , the SCR_1 , inductor L_{m1} , and load in B; in this state, capacitor C is charged at source voltage and behave as an open circuit. The currents of the source A, L_{m2} , SCR_1 , L_{m1} and load are equal in steady state to i_{La} . 2) Second state corresponds to steadystate operation, current flows in the forward direction B to A. The current passes through the low-frequency circuit composed of 4, 3, 5, 1, and 0 which consists of the source in B, inductor L_{m1} , SCR_3 , L_{m1} and load in A. The currents of the source B, inductor L_{m1} , SCR_3 , L_{m2} , and load are equal in steady state to i_{Lb} . 3) Third state is the transient state or fault occurrence state in B. Current $i_c a$ represents the current of the capacitor C when a fault occurs in B in the transient state. When a fault occurs in B, the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, the voltage in L_{m1} undergoes a sudden increase.

47

Voltage in inductor L_{m1} induces a voltage in inductor L_m2 through mutual inductance and drives current i_{Lm2} supplied to $i_c a$ through the capacitor C; please see Figure 3.19 in red color. The capacitor current $i_c a$ grows and matches the inductor steady-state current $i_L a$ and the SCR_1 commutates off [71]. 4) Fourth state is the transient state or fault occurrence state in A. Current $i_c b$ represents the current of the capacitor C when a fault occurs in A in the transient state. When a fault occurs in A, the instantaneous large current i_{Lm2} flows through the L_{m2} which is connected to the load. After restoring the steady state, i_{Lm2} has increased slightly. Meanwhile, voltage in inductor L_{m2} undergoes a sudden increase. Voltage in the inductor L_{m2} induces a voltage in the inductor L_m1 through mutual inductance and drives current i_{Lm1} supplied to $i_c b$ through the capacitor C; please see Figure 3.19 in red color. Capacitor current $i_c b$ grows and matches the inductor steady-state current $i_L b$ and the SCR_3 commutates off 5) Fifth state begins after SCR_1 is turned off by a fault in B, series LC circuits are connected to the fault and load through 6, 7, 3 and fault; initiating an LC series resonance. Capacitor C supplies the remaining current to inductor L_{m1} and the capacitor voltage changes polarity to negative. Then SCR_2 commutates off due to the reverse current coming from inductor L_{m1} . 6) Sixth state begins after SCR_3 is turned off by a fault in A, series LC circuits are connected to the fault and load through 6, 8, 1 and fault; initiating an LC series resonance. Capacitor C supplies the remaining current to inductor L_{m2} and the capacitor voltage changes polarity to negative. Then SCR_4 commutates off due to the reverse current coming from inductor L_{m2} . 7) Seventh state begins when the voltage in the capacitors decays to zero after the resonance has ended fault in B. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 and D_2 , and resistors R_1 and R_2 respectively until the current decays to zero, 1, 9, 10 and 3, 11, 12. 8) Seventh state begins when the voltage in the capacitors decays to zero after the resonance has ended fault in A. Current from the inductors L_{m1} and L_{m2} continues flowing through diodes D_1 and D_2 , and resistors R_1 and R_2 respectively until the current decays to zero, 1, 9, 10 and 3, 11,12[71].

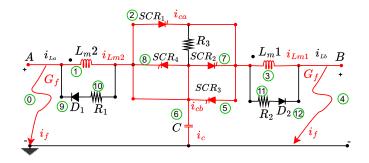


Figure 3.19: Bi-directional topology based on T-source [71]

Bi-directional topology based on T-source

Bi-directional topology based on T-source is depicted in Figure 3.20. It is composed of one capacitor (C), four SCRs (SCR_1) , (SCR_2) , (SCR_3) , (SCR_4) and two coupled inductors $(L_{m1}), (L_{m2})$. Assuming that inductors inductors L_{m1}, L_{m2} have the same values respectively Lm. Points A or B can be source or load. G_f is the conductance used to simulate the fault conductance in A or B. The aim of the Z-source breaker is safely disconnect the source when a short circuit occurs in A or B. The forward direction of the current flow is defined by

activating or deactivating the SCRs with a control circuit. This topology has eight operating states that are described as follows: 1) First estate corresponds to steady-state operation, current flows in the forward direction A to B. SCR_1 and SCR_2 activated. The current passes through the low-frequency circuit composed of 0, 1, 2, 3, 4 and 5 which consists of the source in A, inductor L_{m2} SCRs SCR_1 , SCR_2 , inductor L_{m1} , and load in B; in this state, capacitor C is charged at source voltage and behave as an open circuit. The currents of the source A, L_{m2} , SCR_1 , SCR_2 , L_{m1} and load are equal in steady state to i_{La} . 2) Second state corresponds to steady-state operation, current follows in the forward direction B to A. SCR_3 and SCR_4 activated. The current passes through the low-frequency circuit composed of 5, 4, 6, 7, 1 and 0 which consists of the source in B, L_{m1} , SCR_3 , SCR_4 , L_{m2} and load in A. The currents of the source B, SCR_3 , SCR_4 , L_{m1} , L_{m2} and load are equal in steady state to i_{Lb} .3) Third state is the transient state or fault occurrence state in B. Current i_{ca} represents the current of the capacitor C when a fault occurs in B in the transient state. When a fault occurs in B, the instantaneous large current i_{Lm1} flows through the L_{m1} which is connected to the load. After restoring the steady state, i_{Lm1} has increased slightly. Meanwhile, the voltage in L_{m1} undergoes a sudden increase. Voltage in inductor L_{m1} induces a voltage in inductor L_{m2} through mutual inductance and drives current i_{Lm2} supplied to $i_c a$ through the capacitor C; please see Figure 3.20 in red color. The capacitor current $i_c a$ grows and matches the inductor steady-state current $i_L a$ and the SCR_1 commutates of [71]. 4) Fourth state is the transient state or fault occurrence state in A. Current $i_c b$ represents the current of the capacitor C when a fault occurs in A in the transient state. When a fault occurs in A, the instantaneous large current i_{Lm2} flows through the L_{m2} which is connected to the load. After restoring the steady state, i_{Lm2} has increased slightly. Meanwhile, voltage in inductor L_{m2} undergoes a sudden increase. Voltage in the inductor L_{m2} induces a voltage in the inductor L_{m1} through mutual inductance and drives current i_{Lm1} supplied to $i_c b$ through the capacitor C; please see Figure 3.20 in red color. Capacitor current $i_c b$ grows and matches the inductor steady-state current $i_L b$ and the SCR_2 commutates off . 5) Fifth state begins after SCR_1 is turned off by a fault in B, series LC circuits are connected to the fault and load through 8, 3, 4 and fault; initiating an LC series resonance. Capacitor C supplies the remaining current to inductor L_{m1} and the capacitor voltage changes polarity to negative. Then SCR_2 commutates off due to the reverse current coming from inductor L_{m1} . 6) sixth state begins after SCR_3 is turned off by a fault in A, series LC circuits are connected to the fault and load through 8, 7, 1 and fault; initiating an LC series resonance. Capacitor Csupplies the remaining current to inductor L_{m2} and the capacitor voltage changes polarity to negative. Then SCR_4 commutates off due to the reverse current coming from inductor L_{m2} . 7) Seventh state begins when the voltage in the capacitors decays to zero after the resonance has ended, fault in B. Inductors L_{m1} and L_{m2} remain in operation during the reverse direction of power flow. 8) Inductors L_{m1} and L_{m2} remain in operation during the reverse direction of power flow [71].

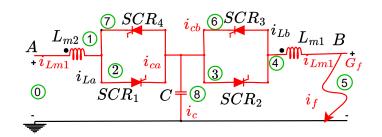


Figure 3.20: Bi-directional topology based on T-source [71]

Chapter 4

Results obtained from the Z-source topologies simulations

4.1 Introduction

In this chapter, the considerations for developing the simulations are explained and the details of the different Z-source topologies simulation are analyzed. The topologies were simulated with OpenModelica's Electrical library. OpenModelica is a complete modeling and simulation tool for complex integrated physical systems. Openmedelica allows modeling complex interactions between systems from different engineering fields, such as electrical circuits, thermodynamics, hydraulics, mechanics, pneumatics and control[26, 22]. It has a very friendly and intuitive interface. Open Modelica has a powerful graphing tool, however the data was exported in csv files and graphed. with the Python package Matplotlib, which offers some additional editing features. The numerical method used was DASSL, since it is an implicit numerical method suggested by the OpenModelica community.

In this chapter, Z-source topologies included in this project were simulated for comparison purposes, the considerations for developing simulations are explained and also some details of different topologies are analyzed. The fault was modeled with a variable resistor controlled by a ramp signal from 0.2 to 0 Ω in 100 µs s[10], the ramp was set to start in 0.2s, that corresponds to sufficient time for the circuit to be stable after start-up; a switch is synchronized to connect the fault to the circuit in 0.2s; a 0.08s pulse through the gate activates the SCR, please see Figure 4.1. Even though topologies that were proposed in technical literature usually have different values for the source voltage, inductors, capacitors, load resistances, damping resistances, and fault resistances. So, the following parameters were used for simulations across all of the topologies: Source voltage $V_s = 6.000V$, source inductor $L_s = 10$ µH., load resistor $R_L = 6\Omega$, capacitors C = 200 µF, parasitic load capacitance $C_L = 1mF$, snubber resistor $R = 0.1\Omega$, inductors L = 2.4 mH, fault resistor $R = 20m\Omega$. Diodes and SCRs were simulated as ideal elements while the internal resistances of the inductors and capacitors is the minimum assigned by OpenModelica. In addition, the coupling coefficient of the topologies with magnetic coupling was assumed as k = 0.

4.2 Mono-directional topologies results

4.2.1 Result Classic Z-source topology

Figure 4.1 shows the implementation of the Classic Z-source topology in OpenModelica, this topology was explained and described in section 3.2.1 and corresponds to Figure 3.1.

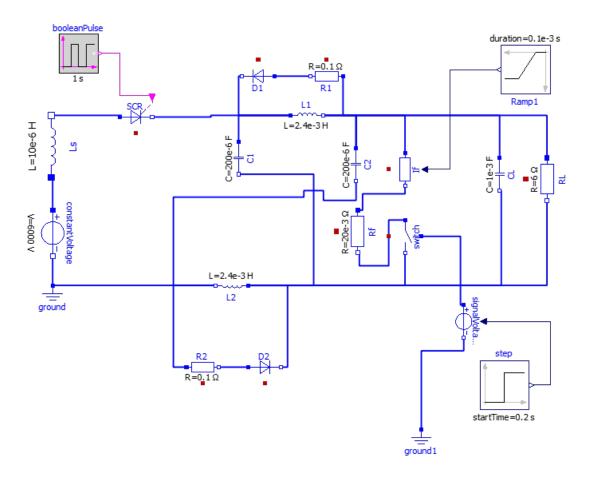


Figure 4.1: OpenModelica simulation of classic Z-source topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_L) of classic Z-source topology, are depicted in Figure 4.2. Figure 4.2 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. Please note that i_f rises to a maximum value and then decreases. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.2 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.2 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. When v_{SCR} crosses zero, the arc generated during switching is mitigated, similar to what happens in AC circuits please see brown line. In addition, the load voltage v_0 behavior is observed.

cleared the load voltage decays to zero, please see blue line.

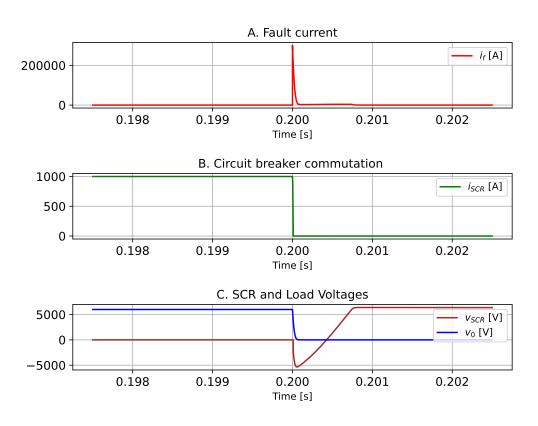


Figure 4.2: Classic Z-source behavior i_f , i_{SCR} , v_{scr} , v_0

Capacitors current(i_c), inductors current (i_L), capacitors voltages (v_C), inductors voltage(v_L), load current (i_{RL}) and source current(i_s) of classic Z-source topology are depicted in Figure 4.3. Figure 4.3 A) corresponds to the moment when the transient current of the capacitor (red line) reaches the steady state, current of the inductor (green line) is observed. In this instant time, the commutation occurs. After disconnection, capacitor current and inductor current are equal because they are connected in series. In Figure 4.3 B), the series resonance lapse is observed. When the inductor voltage (blue line) is equal to the capacitor voltage (brown line), it corresponds to the series resonance time. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero and intend to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues to circulate in the circuit snubber. In Figure 4.3 C), the behavior of the current in the source and the current in the load are depicted. Once fault clearance has occurred, the current in the source (violet line) immediately decays to zero and the current in the load (black line) that also dacays to zero. In effect, classic Z-source topology simultaneously protects the source and the load.

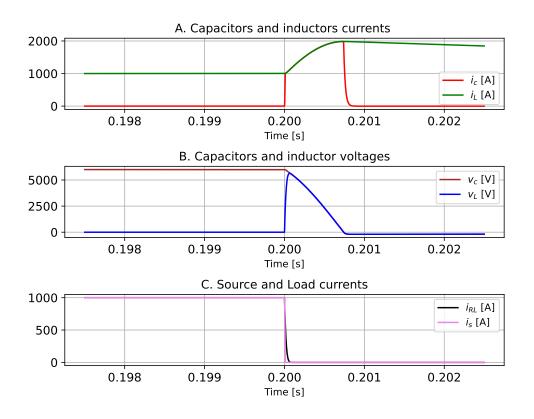


Figure 4.3: Classic Z-source behavior i_c , i_L , v_c , v_L , i_{RL} , i_s

Fault (i_f) and capacitors (i_c) currents of classic Z-source topology are depicted in Figure 4.4. It is observed that the current through the capacitor is only 6% of the fault current. This occurs because the capacitor current does not depend directly on the fault current, but rather on the variation of the voltage in the inductor, please see Figure 4.4.

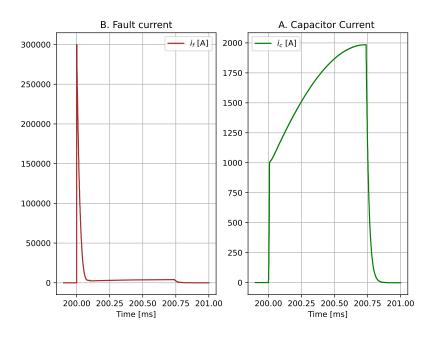


Figure 4.4: Classic Z-source behavior i_f , i_c

4.2.2 Result Parallel Z-source topology

Figure 4.5 shows the implementation of Parallel Z-source topology in OpenModelica, this topology was explained and described in section 3.2.1 and corresponds to Figure 3.3

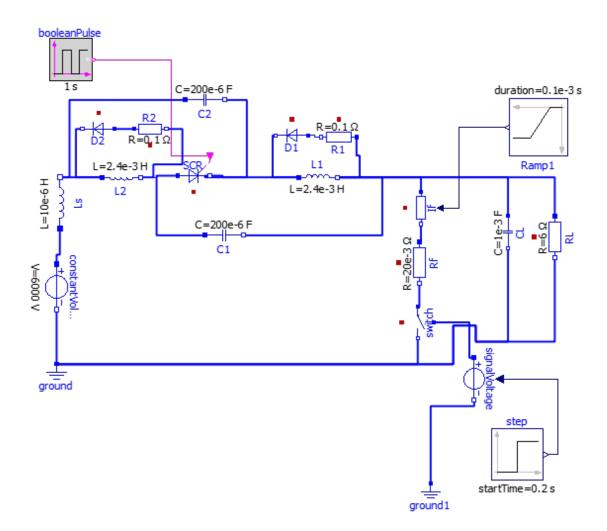


Figure 4.5: OpenModelica simulation of parallel Z-source topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of parallel Z-source topology are depicted in Figure 4.6. Figure 4.6 A) corresponds to the fault current i_f . The fault current of this topology is similar to the fault current of the classical Z-source. Figure 4.6 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases similar to the classic Zsource. Note that in Figure 4.6 C), v_{SCR} voltage crosses zero and then stabilizes; moreover, the v_{SCR} voltage oscillates before stabilizing. These oscillations occur because the capacitor C_1 is connected to the source and the source receives current reflects at the end of the series resonance due to the inductance of the source, please see Figure 4.6. However, the load voltage v_0 decays to zero instantaneously.

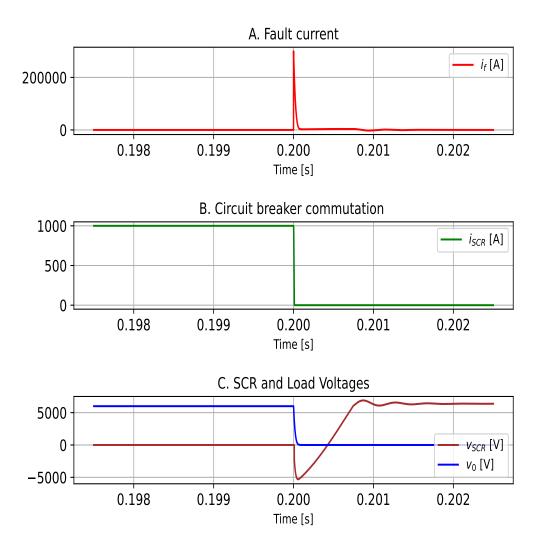


Figure 4.6: Parallel Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitors current (i_c) , inductors current (i_L) , capacitors voltage (v_C) , inductors voltage (v_L) , load current (i_{RL}) , and source current (i_s) of parallel Z-source topology are depicted in Figure 4.7. Figure 4.7 A) corresponds to capacitor current i_C , and inductor current i_L . After the SCR has turned off, the capacitor and inductor have the same current because they are in series. When the voltage across the inductor has dropped to zero, the current in the inductor continues to dissipate in the snubber circuit. Nonetheless, the current in the capacitor continues to oscillate due to the series resonance between capacitor C_1 and the inductance of the source, please see red line .Figure 4.7 B) corresponds to capacitor voltage v_C , inductor voltage v_L . It is observed that the voltage across capacitor C_1 increases and remains at the source voltage due to the connection between the capacitor and the source. The capacitor and inductor voltages only coincide at one point, which corresponds to series resonance. Additionally, the voltage in the inductor decays to zero in a similar manner to the classical Z-source behavior. Figure 4.7 C) corresponds to load current i_{RL} and source current voltage i_s . The current in the load is observed to instantaneously drop

to zero. Nonetheless, the current in the source experiences a significant increase which can be harmful to the source. This current increase is caused by the series resonance of i_s with C_1 and its magnitude depends on the inductance of the source. The design of a filter is necessary to mitigate the problem of reflected current towards the source. Unlike classical Z-source topology, this topology does not fully protect the source, as the source risks being affected by the reflected current at the end of the series resonance.

58

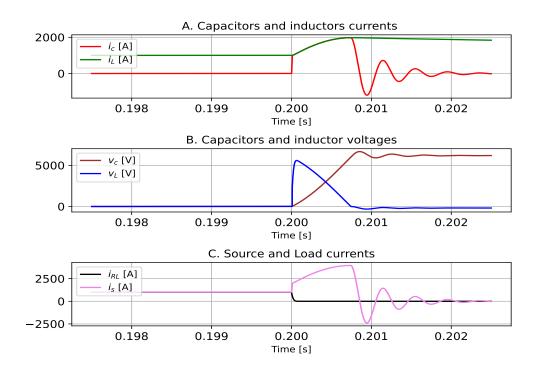


Figure 4.7: Parallel Z-source behavior i_C , i_L , v_C , v_L , i_{RL} , i_s

4.2.3 Result Series Z-source topology

Figure 4.8 shows the implementation of the Parallel Z-source topology in OpenModelica, this topology was explained and described in section 3.2.1 and corresponds to Figure 3.4.

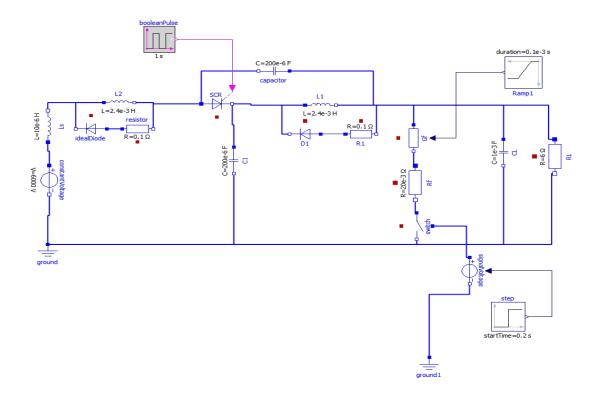


Figure 4.8: OpenModelica simulation of series Z-source topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of series Z-source topology are depicted in Figure 4.9. Figure 4.9 A) corresponds to the fault current i_f . The fault current of this topology is greater to the fault current of the classical Z-source; however, its behavior is similar to the classic Z-source. Figure 4.9 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases similar to the classic Z-source. Note that in Figure 4.9 C, SCR voltage crosses zero and then stabilizes. Note that the SCR voltage oscillates before stabilizing. These oscillations occur because the capacitor C_1 is connected to the source and the source receives current that reflects at the end of the series resonance, please see 4.8. Finally, load voltage v_0 decays to zero instantaneously.

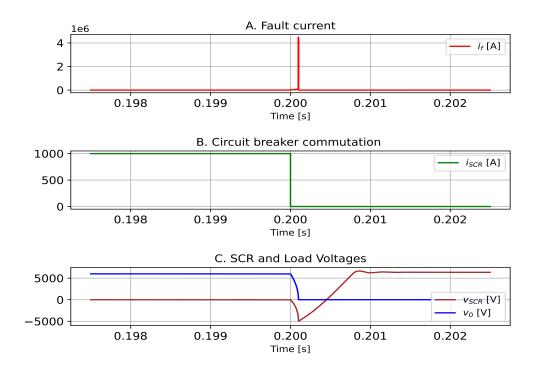


Figure 4.9: Series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) , load current (i_{RL}) , and source current (i_s) of parallel Z-source topology are depicted in Figure 4.10. Figure 4.10 A) corresponds to capacitor current i_C , inductor current i_L . When the transient current of the capacitor i_C reaches the steady state current of the inductor i_L is observed. In this time, the commutation occurs. After disconnection capacitor and inductor currents are equal because they are connected in series. Figure 4.10 B) corresponds to capacitor voltage v_C and inductor voltage v_L . The series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time ocurs. Once the resonance is finished, the voltage across the capacitor decays to zero and the current in the inductor decays to zero intending to become negative. Figure 4.10 C) corresponds to load current i_{RL} and source current voltage i_s . The current in the load is observed to instantaneously drop to zero. However, the current in the source experiences an increase, which can be harmful to the source. This current increasing is caused by the series resonance of i_s with C_1 and its magnitude depends on the inductance of the source. Nonetheless, part of the resonance current is supplied by capacitor C_2 , thus reducing the current reflected back to the source by 33% with respect to the parallel Z-source topology.

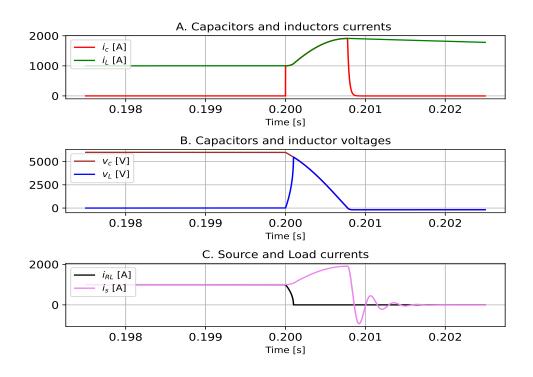


Figure 4.10: Series Z-source behavior i_C , i_L , v_C , v_L , i_{RL} , i_s

4.2.4 Result Alternative Z-source topology

Figure 4.11 shows the implementation of the Alternative Z-source topology in OpenModelica, this topology was explained and described in section 3.2.1 and corresponds to Figure 3.5.

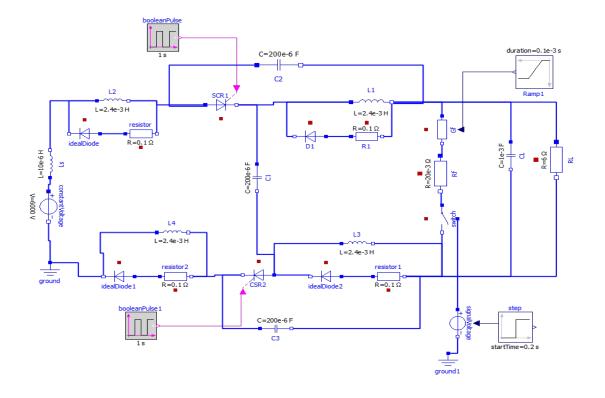


Figure 4.11: OpenModelica simulation of Alternative Z-source topology

Fault current (i_f) , SCR currents (i_{SCR1}) , (i_{SCR2}) , SCR voltages (v_{SCR1}) , (v_{SCR2}) , and load voltage (v_0) of Alternative Z-source topology, are depicted in Figure 4.12. Figure 4.12 A) corresponds to the fault current i_f . The fault current of this topology is greater to the fault current of the classical Z-source. Figure 4.12 B) corresponds to the SCR currents i_{SCR1} and i_{SCR2} . Before fault occurrence, i_{SCR1} and i_{SCR2} have a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR1} rapidly decreases to zero for clearing the fault. SCR_1 commutes off before SCR_2 . Then SCR_2 receives part of the fault current after SCR_1 has commutated off. Nonetheless, commutation process is almost instantaneous and similar to the classic Z-source. Note that in Figure 4.12 C), SCR voltage v_{SCR1} crosses zero and then stabilizes and v_{SCR2} has a low voltage of negative polarity. Note that the SCR voltage oscillates before stabilizing. These oscillations occur because the capacitor C_1 is connected to the source and the source receives current reflects at the end of the series resonance, please see Figure 4.12. Finally, load voltage v_0 decays to zero instantaneously.

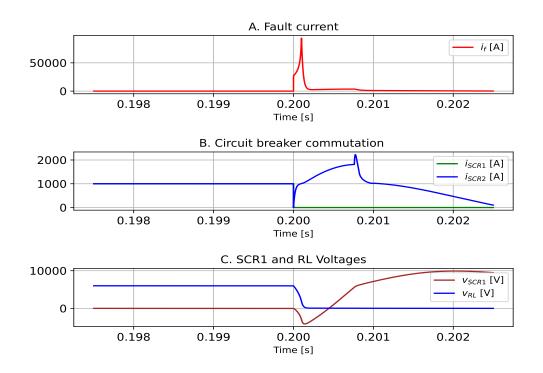


Figure 4.12: Alternative Z-source topology behavior i_f , i_{SCR1} , i_{SCR2} , V_{SCR1} , V_{SCR2} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) , load current (i_{RL}) , and source current (i_s) of parallel Z-source topology are depicted in Figure 4.13. Figure 4.13 A) corresponds to capacitor current i_{C1} , inductor current i_{L1} . After the SCR has turned off, the capacitor and inductor have the same current because they are in series. When the voltage across the inductor has dropped to zero, the current in the inductor continues dissipating in the snubber circuit. However, the current in the capacitor continues to oscillate due to the series resonance between capacitor C_1 and the inductance of the power source, please see red line in Figure 4.13. Figure 4.13 B) corresponds to capacitor voltage v_C , inductor voltage v_L . The series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor C_1 becomes negative and conducts while energy is dissipated in the inductor. The current in the inductor decays to zero. Figure 4.13 C) corresponds to load current i_{RL} and source current voltage i_s . The current in the load is observed to instantaneously drop to zero. However, the current in the source experiences a significant increase, which can be harmful to the source. This current increasing is caused by the series resonance of i_s with C_2 and its magnitude depends on the inductance of the source. It is important to add that the objective of this topology is to increase the fault clearance speed. However, negative voltages across the capacitor can increase the potential difference across the SCR, and too many elements are added in the path of connection between ground and load.

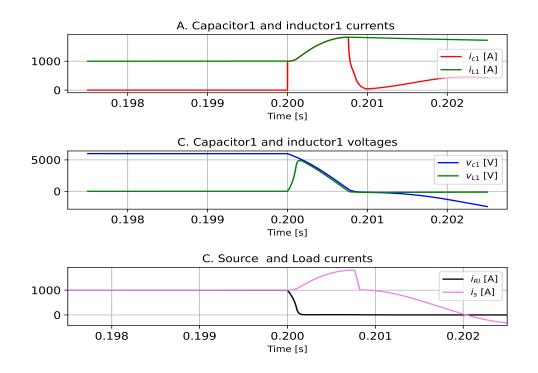


Figure 4.13: Alternative Z-source topology behavior i_{C1} , i_{L1} , v_{C1} , v_{L1} , v_{C1} , i_{Ls}

4.2.5 Result Series connected Z-source with response to load variations topology

Figure 4.14 shows the implementation of Series connected Z-source with response to load variations in OpenModelica, this topology was explained and described in section 3.2.1 and corresponds to Figure 3.6.

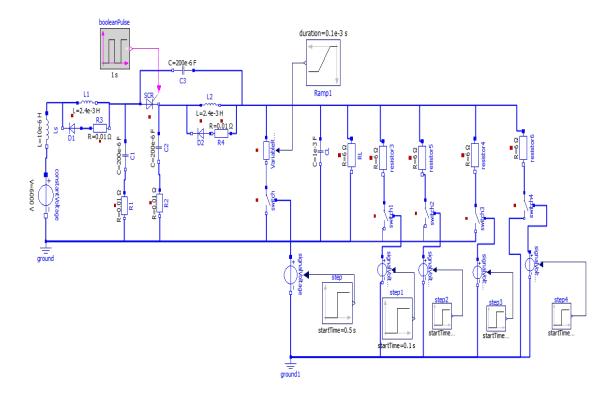


Figure 4.14: OpenModelica Simulation Series connected Z-source with response to load variations

SCR current (i_{SCR}) of Series connected Z-source with response to load variations topology is depicted in Figure 4.15. For this simulation, four loads have been added in parallel with the initial load. Sequentially each load is energized every 0.1s, when 0.5s elapse the fault is entered. A 200 μ f capacitor and a 0.1 Ω resistor were added to supply the non-fault currents requested by the load, please see Figures 4.15 and 4.14. It is observed that the circuit breaker supplies the changes in the load without commutation off. When the fault occurs, it commutes off.

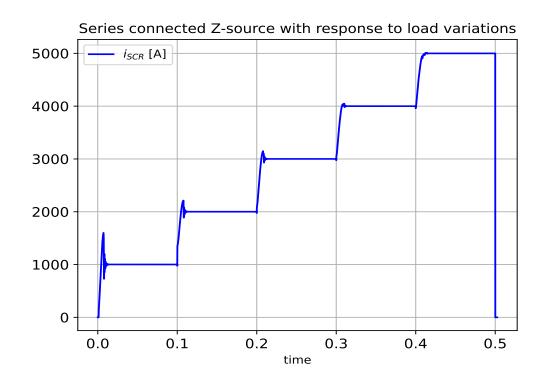


Figure 4.15: Series connected Z-source with response to load variations behavior i_{SCR}

4.2.6 Result Classic Z-source using magnetic coupling topology

Figure 4.16 shows the implementation of the Classic Z-source using magnetic coupling topology in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.7. For this simulation the coupled inductors have 1.2mH which corresponds to half of the inductance used in the classical Z-source. This in order to verify if by using half the inductance of the classical Z-source the performance of the circuit breaker is the same[43]. It is important to add that in this topology, the magnetic couplings are not part of the commutation path.

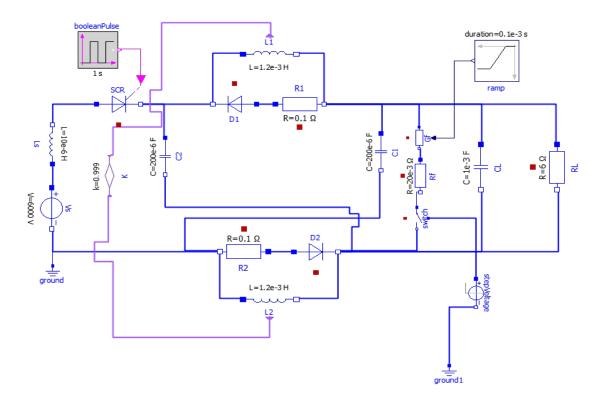


Figure 4.16: OpenModelica Simulation Classic Z-source using magnetic coupling topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_L) of Classic Z-source using magnetic coupling topology are depicted in Figure 4.17. Figure 4.17 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. Please note that i_f rises to a maximum value and then decreases. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.17 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.17 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. When v_{SCR} crosses zero, the arc generated during switching is mitigated, similar to what happens in AC circuits. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared, the load voltage decays to zero, please see blue line.

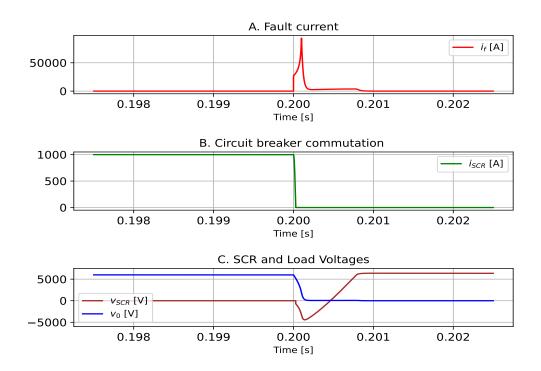


Figure 4.17: OpenModelica Simulation Classic Z-source using magnetic coupling topology behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of Classic Z-source using magnetic coupling topology are depicted in Figure 4.18. Figure 4.18 A) shows the moment when the transient current of the capacitor (red line) reaches the steady state current of the inductor (green line) is observed. In this time, the commutation occurs. After disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.18 B), the series resonance lapse is observed. When the inductor voltage (blue line) is equal to the capacitor voltage (brown line) that corresponds to the series resonance time. Once the resonance is finished, the voltage across the capacitor decays to zero and also inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues to circulate in the circuit snubber. In Figure 4.18 C), the current in the source and the current in the load are depicted. Once fault clearance has occurred, the current in the source (violet line) immediately decays to zero and the current in the load (black line) also decays. In effect, this topology simultaneously protects the source and the load. This topology makes it possible to reduce size and weight by using a coupled inductor for the same purpose as the classic Z-source.

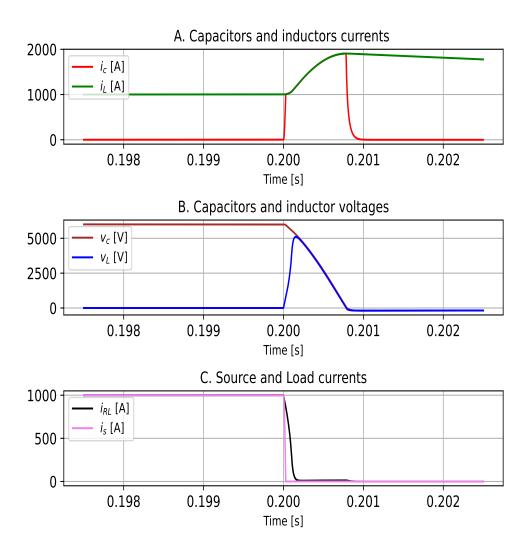


Figure 4.18: Classic Z-source using magnetic coupling topology behavior $i_C,\,i_L,\,v_C,\,v_L$, $i_{RL},\,i_s$

4.2.7 Result Series Z-source using magnetic coupling topology

Figure 4.19 shows the implementation of series Z-source using magnetic coupling topology in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.8. It is important to add that, in this topology, the magnetic couplings are not part of the commutation path.

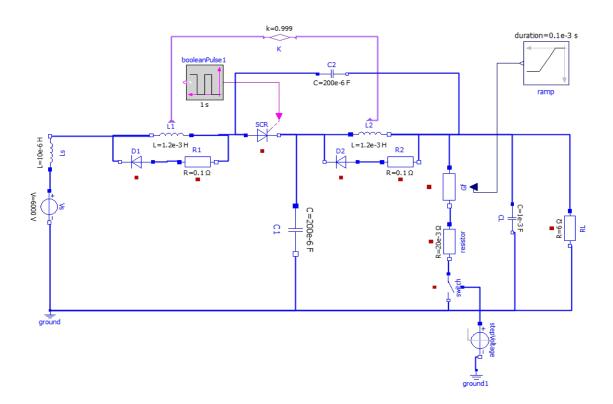


Figure 4.19: OpenModelica simulation of Series Z-source using magnetic coupling topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of series Z-source using magnetic coupling topology are depicted in Figure 4.20. Figure 4.20 A) corresponds to the fault current i_f . The fault current of this topology is similar to the fault current of the classical Z-source. Figure 4.20 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases similar to the classic Z-source. Note that in Figure 4.20 C), v_{SCR} voltage crosses zero and then stabilizes. However, there are oscillations in the SCR voltage due to the capacitor is in series with the source at the end of the resonance stage. The voltage at the load v_0 drops rapidly to zero.

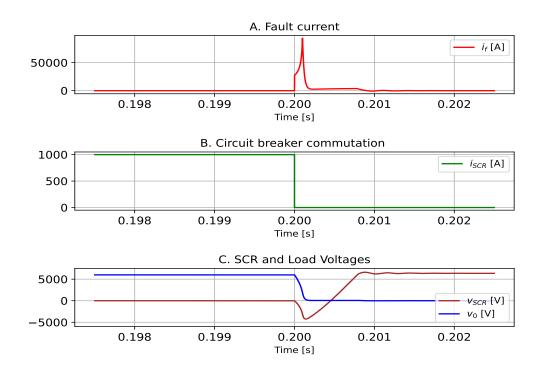


Figure 4.20: Series Z-source using magnetic coupling topology behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) , load current (i_{RL}) , and source current (i_s) of parallel Z-source topology are depicted in Figure 4.21. Figure 4.21 A) corresponds to capacitor current i_C , inductor current i_L . After the SCR has turned off, the capacitor and inductor have the same current because they are in series. When the voltage across the inductor has dropped to zero, the current in the inductor continues dissipating in the snubber circuit. Nonetheless, the current in the capacitor continues to oscillate due to the series resonance between capacitor C_1 and the inductance of the source, please see red line in Figure 4.21. The oscillations described by the current in the capacitor and the current in the inductor at the end of the resonance are considerable compared to the series topology without magnetic coupling. In Figure 4.21B), the series resonance lapse is observed. When the inductor voltage (blue line) is equal to the capacitor voltage (brown line), the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues to circulate in the circuit snubber. In Figure 4.21 C), the behavior of the current in the source i_s and the current in the load i_{RL} are depicted. Once fault clearance has occurred the current in the source (violet line) increases, oscillating and droping to zero. The current in the load (black line) rapidly drops to zero. In effect, this topology simultaneously protects the source and the load. Then it can be concluded that for series topology with magnetic coupling it is necessary to know in advance the source inductance to ensure proper behavior of the circuit breaker.

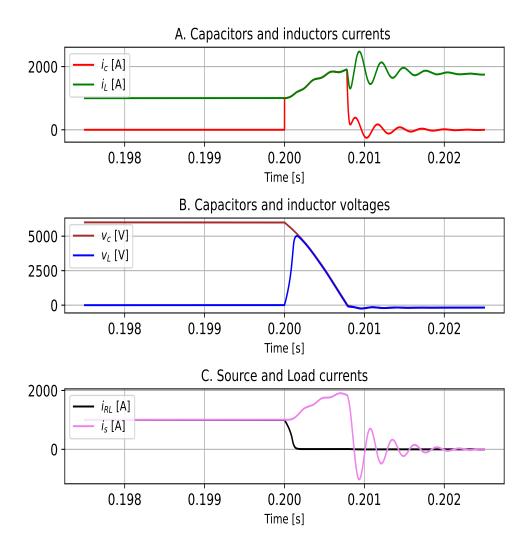
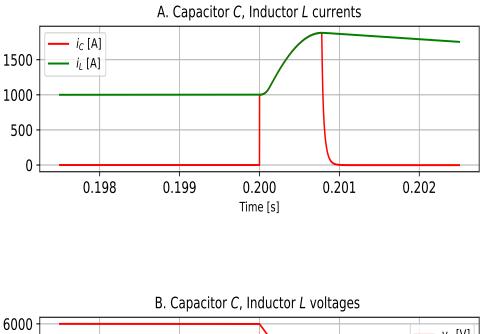


Figure 4.21: Series Z-source using magnetic coupling topology behavior i_C , i_L , v_C , v_L , i_{RL} , i_s

Capacitor current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) of parallel Z-source topology are depicted in Figure 4.22. The aim is to depict the behavior of currents and voltages when the source inductor i_s is not included. Figure 4.22 A) corresponds to capacitor current i_C , inductor current i_L . After the SCR has turned off, the capacitor and inductor have the same current because they are in series. When the voltage across the inductor has dropped to zero, the current in the inductor continues dissipating in the snubber circuit. However, note that no oscillations are observed in the currents. In Figure 4.22 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Please note that no oscillations are observed in the voltages. Indeed, the source inductance is a very important variable in this topology.



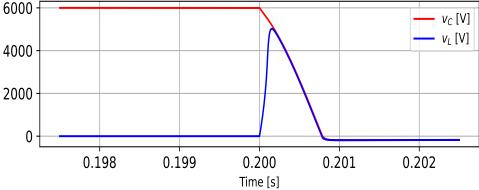


Figure 4.22: Z-source in series with magnetic coupling topology does not include an inductance at the source L_s behavior i_c , i_L , v_c , v_L

4.2.8 Result Classic connected Z-source using magnetic coupling with reduced capacitance

Figure 4.23 shows the implementation of classic connected Z-source using magnetic coupling with reduced capacitance in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.9.

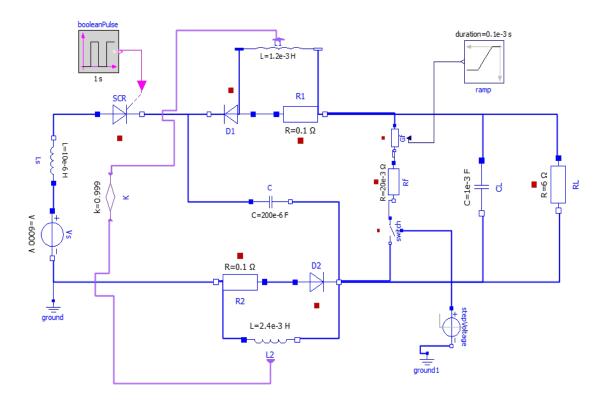


Figure 4.23: OpenModelica simulation of Classic connected Z-source using magnetic coupling with reduced capacitance topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of classic connected Z-source using magnetic coupling with reduced are depicted in Figure 4.24. Figure 4.24 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. Please note that i_f rises to a maximum value and then decreases. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation in the circuit. Figure 4.24 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.24 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared the load voltage decays to zero.

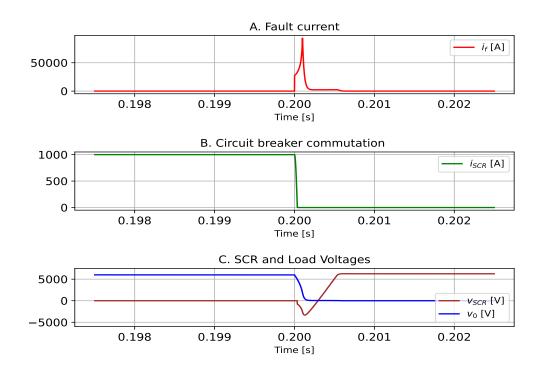


Figure 4.24: Classic connected Z-source using magnetic coupling with reduced capacitance behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductorsvoltage (v_L) , load current (i_{RL}) and source current (i_s) of Classic connected Z-source using magnetic coupling with reduced capacitance topology are depicted in Figure 4.25. It is important to know that the couplings are part of the commutation path in this topology. Figure 4.25 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this time, the commutation occur. After the disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.25 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage also decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues circulating in the circuit snubber. In Figure 4.25 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred, the current in the source immediately decays to zero and the current in the load also decays. Note that the capacitor is in parallel with the source and is charged; furthermore, it does not produce representative oscillations in the commutation process. This topology protects both the source and the load.

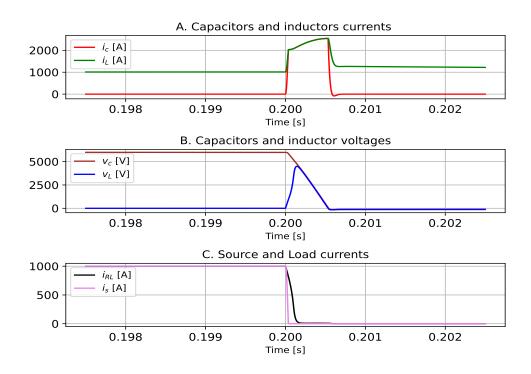


Figure 4.25: Classic connected Z-source using magnetic coupling with reduced capacitance behavior i_c , i_L , v_c , v_L , i_{RL} , i_s

4.2.9 Result T-Source topology

Figure 4.26 shows the implementation of T-Source in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.10.

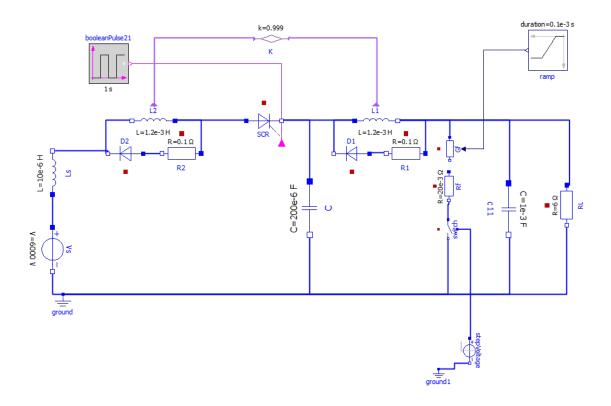


Figure 4.26: OpenModelica Simulation of T-Source topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of T-Source topology are depicted in Figure 4.27. Figure 4.27 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.27 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.27 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior of this topology is similar to the classic Z-source and it protects both the source and the load.

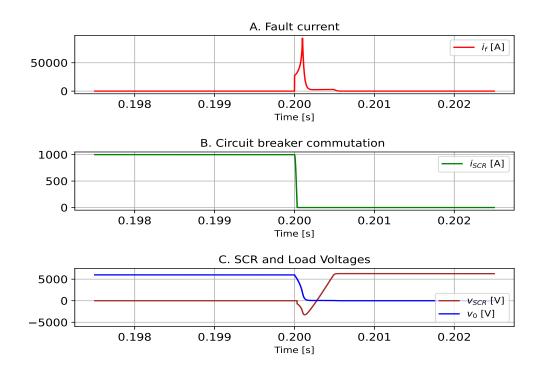


Figure 4.27: T-Source topology behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of T-Source topology are depicted in Figure 4.28. It is important to know that the couplings are part of the commutation path in this topology. Figure 4.28 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this time, the commutation occurs. After the disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.28 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues circulating in the circuit snubber. In Figure 4.28 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred the current in the source immediately decays to zero and the current in the load also decays.

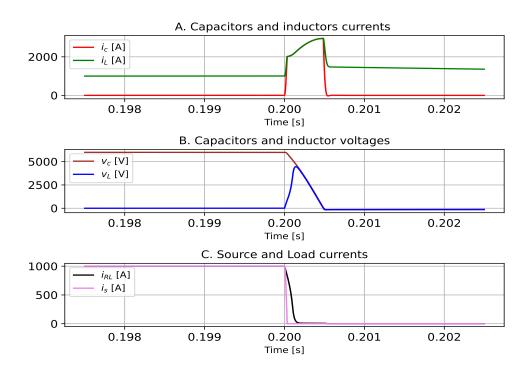


Figure 4.28: T-Source topology behavior i_c , i_L , v_c , v_L , i_{RL} , i_s

4.2.10 Result τ -source topology

Figure 4.29 shows the implementation of τ -source topology in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.11.

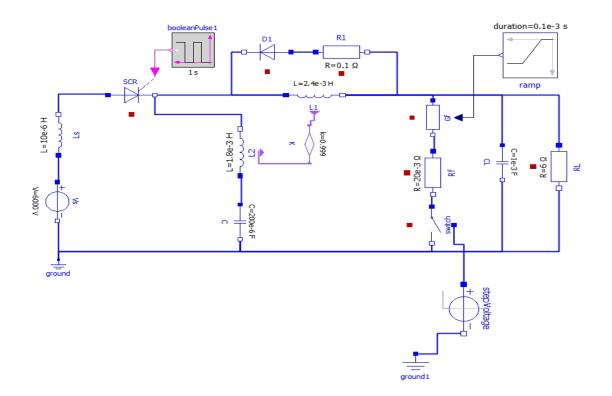


Figure 4.29: OpenModelica simulation of τ -source topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of τ source topology are depicted in Figure 4.30. Figure 4.30 A) corresponds to the fault current i_f . The fault current of this topology is similar to the fault current of the classical Z-source. Figure 4.30 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases similar to the classic Z-source. Note that in Figure 4.30 C) v_{SCR} voltage crosses zero and then stabilizes.

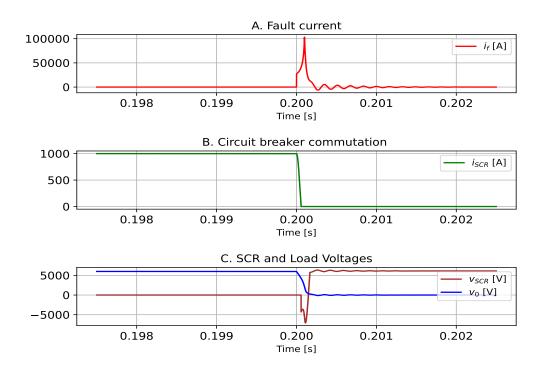


Figure 4.30: τ -Source topology behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of τ -source topology are depicted in Figure 4.31. It is important to know that the couplings are part of the commutation path in this topology. Figure 4.31 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor L_1 is observed. In this time, the commutation occurs. It has been observed that the current induced by inductor L_1 in L_2 is equal to the current flowing through the capacitor C. When capacitor C discharges and its current decays to zero, the current in inductors L_1 and L_2 decays more slowly as the energy dissipates in the snubber. However, it is important to note that, for the given values of inductors and capacitors in the τ -source topology, the current flowing through the capacitor and inductors is much higher than other topologies. To address this issue, it is necessary to increase the value of inductor L_1 so that the current induced by L_1 in L_2 is reduced. In Figure 4.31 B), behavior of v_c , v_L , v_{L1} and v_{L2} is observed. the inductor voltage L_2 has opposite polarity to the inductor voltage L1, which allows a current from capacitor C. When the voltage across the capacitor drops to zero, the voltage across the inductors increases and then also drops to zero. In Figure 4.31 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred, the current in the source immediately decays to zero and the current in the load also decays.

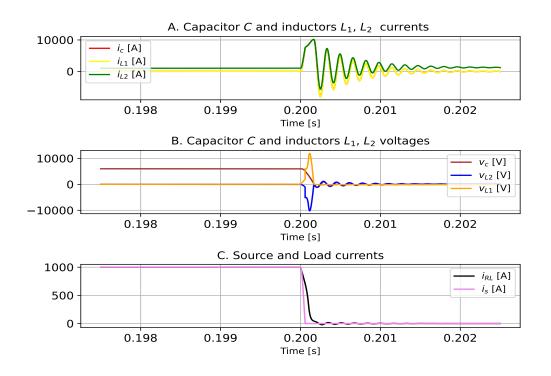


Figure 4.31: τ -source topology behavior i_c , i_{L1} , i_{L2} , v_c , v_L , v_{L1} , v_{L2} , i_{RL} , i_s

COMPARISON OF ELECTRICAL FAULT RESPONSES IN Z-SOURCE CIRCUIT BREAKER TOPOLOGIES FOR D.C. MICROGRID APPLICATIONS.

Capacitor current(i_c), inductor current (i_L), capacitor voltages (v_C), inductor voltage(v_L) of τ -source topology are depicted in Figure 4.32. For this particular case, the inductor values in this topology were adjusted to achieve similar current values through capacitor Cas those in the other topologies. This was done to investigate whether this topology requires additional materials compared to the others for a similar scenario. Specifically, an inductor value of $L_1 = 20mH$ and $L_2 = 4mH$ was chosen, resulting in a comparable current through the capacitor as that observed in the other topologies, as shown in Figure 4.32. Figure 4.32 A) depicts the current behavior similar to Figure 4.31, but with a lower value of capacitor current. Additionally, Figure 4.32 B) depict similar voltage behavior as in Figure 4.31, but with lower voltages. Thus, it is evident that the total inductance of the circuit breaker is a crucial parameter when making comparisons of topologies under equal conditions. The total inductance for this topology is 24mH, in contrast to the other topologies, whose total inductance is around 4.8mH. Then, the *tau*-source topology requires a larger volume and weight of inductors than the other topologies, even though it has fewer elements.

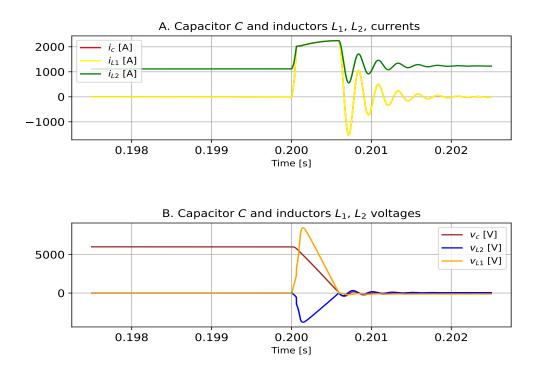


Figure 4.32: τ -Source topology with inductor values optimized for lower i_C behavior i_c , i_{L1} , i_{L2} , v_c , v_L , v_{L1} , v_{L2}

4.2.11 Result O-Zsource topology

Figure 4.33 shows the implementation of τ -source topology in OpenModelica, this topology was explained and described in section 3.2.2 and corresponds to Figure 3.12.

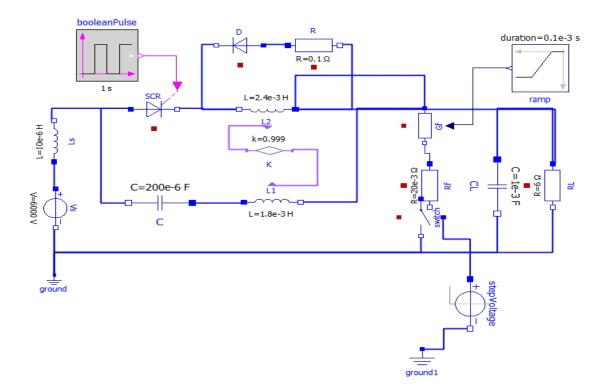


Figure 4.33: OpenModelica simulation of O-Zsource topology

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of O-Zsource topology are depicted in Figure 4.34. Figure 4.34 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.34 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.34 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. The voltage zero crossing in the SCR is very short compared to other topologies, but sufficient for the commutation process. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared, the load voltage decays to zero. The behavior of this topology is similar to the classic Z-source and it protects both the source and the load.



Figure 4.34: O-Zsource topology behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of O-Zsource topology are depicted in Figure 4.35. It is important to know that the couplings are part of the commutation path in this topology. Figure 4.35 A) shows the moment when the transient current of the capacitor reaches the steady state current of the nductor L_2 is observed. In this time, the commutation occurs. It has been observed that the current induced by inductor L_1 in L_2 is equal to the current flowing through the capacitor C. When capacitor C discharges and its current decays to zero, the current in inductors L_1 drops to zero too. The current in inductors L_2 drops more slowly as the energy dissipates in the snubber. In Figure 4.35 B), behavior of v_c and v_{L2} is observed. Notice that the voltage across the capacitor decreases to a negative value. This is because it remains with opposite polarity with respect to the source. In Figure 4.35 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred, the current in the load drops to zero; but due to series resonance between the capacitor and the source capacitance, the source experiences high currents at the end of the commutation. One way to improve the performance of this topology is to have different inductance values, which creates a voltage difference at each end of the capacitor at the start of the commutation process.

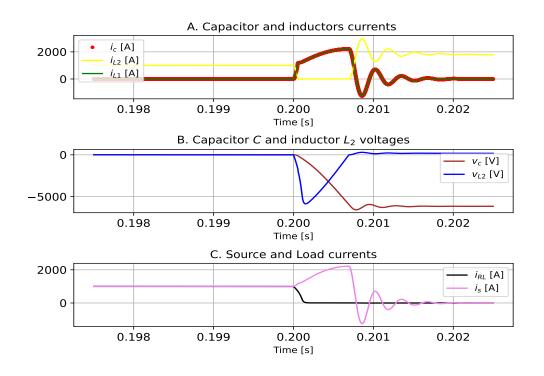


Figure 4.35: O-Z source topology behavior $i_c, i_{L1}, i_{L2}, v_c, v_{L2}, i_{RL}, i_s$

4.3 Results Bi-directional topologies

This section presents the results of the simulations conducted on the bi-directional topologies. The simulations were carried out in only one forward direction, considering all the elements of the topologies. This is because, owing to the symmetry of the circuits breakers, the results are identical in the opposite forward direction.

4.3.1 Result Bi-directional topology based on the classic Z-source

Figure 4.36 shows the implementation of Bi-directional topology based on the classic Z-source in OpenModelica, this topology was explained and described in section 3.3.1 and corresponds to Figure 3.13.

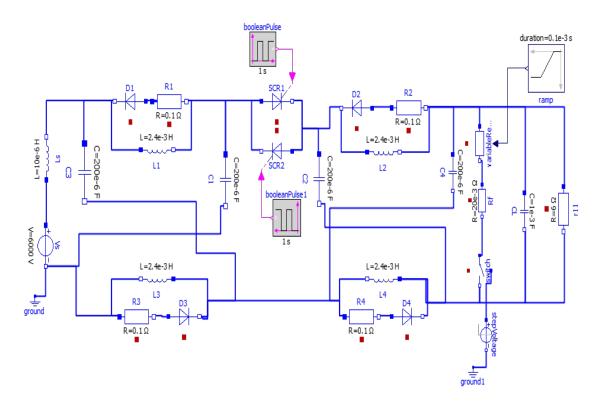


Figure 4.36: OpenModelica simulation of Bi-directional topology based on the classic Z-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bi-directional topology based on the classic Z-source are depicted in Figure 4.37. Figure 4.37 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.37 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage v_0 are depicted in Figure 4.37 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. The voltage zero crossing in the SCR is very short compared to other topologies, but sufficient for the commutation process. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared the load voltage decays to zero.

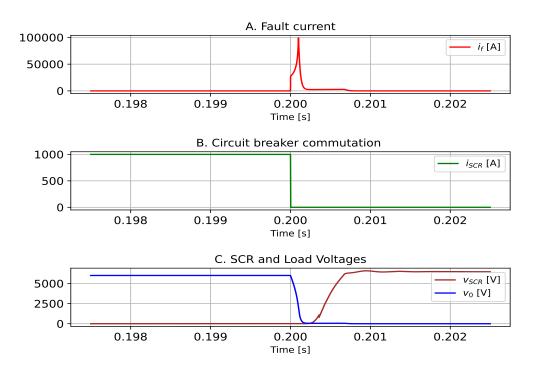


Figure 4.37: Bi-directional topology based on the classic Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitors current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) , load current (i_{RL}) , and source current (i_s) of Bi-directional topology based on the classic Z-source behavior are depicted in Figure 4.38. Figure 4.38 A) corresponds to capacitor current i_C , inductor current i_L . When the transient current of the capacitor i_C reaches the steady state current of the inductor i_L is observed. In this time, the commutation occurs. After the disconnection, capacitor and inductor currents are the same because they are connected in series. Figure 4.38 B) corresponds to capacitors voltage v_C and inductors voltage v_L . The series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero and the current in the inductor decays to zero intending to become negative. Figure 4.38 C) corresponds to load current i_{RL} and source current voltage i_s . The current in the load is observed to instantaneously drop to zero. However, the current in the source experiences a negative increase which can be harmful to the source. This is because capacitors that are not involved in the forward power flow that still plays an active role in the circuit. Hence, during a fault event, these capacitors exchange energy with the source inductance. In other words, the classical Z-source-based bidirectional topology differs from its unidirectional counterpart in the current received by the source due to capacitors that do not participate in the commutation to improve this, limiti tng resistors are required in all capacitors.

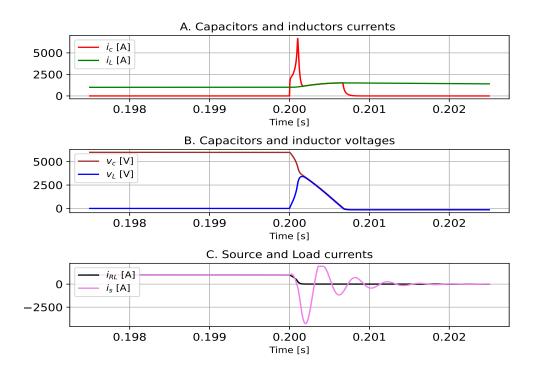


Figure 4.38: Bi-directional topology based on the classic Z-source behavior i_c , i_L , v_c , v_L , i_{RL} , i_s

4.3.2 Result Bi-directional topology based on the series Z-source

Figure 4.39 shows the implementation of Bi-directional topology based on the series Z-source in OpenModelica, this topology was explained and described in section 3.3.1 and corresponds to Figure 3.14.

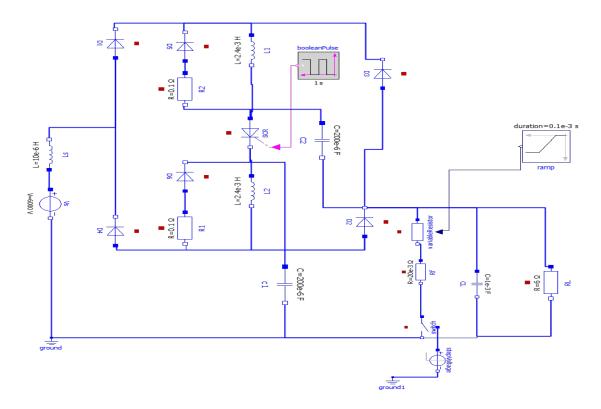


Figure 4.39: OpenModelica simulation of Bi-directional topology based on the series Z-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bidirectional topology based on the series Z-source are depicted in Figure 4.40. Figure 4.40 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.40 B) corresponds to the SCR current i_{SCR} . It should be noted that the current flowing through the SCR is higher than the current in the load due to the currents passing through the blocking diodes D_3 and D_5 , as shown in Figures 4.39 and 4.40. This effect increases the steady-state losses of the SCR and needs to be considered when selecting the SCR size. Furthermore, a higher fault clearance current is required compared to other topologies. Before fault occurrence, i_{RL} has a value of 1.000A which corresponds to the normal operation of the circuit. After fault occurrence i_{SCR} rapidly drops to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage v_0 are depicted in Figure 4.40 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior is observed . Once the fault is cleared the load voltage decays to zero.

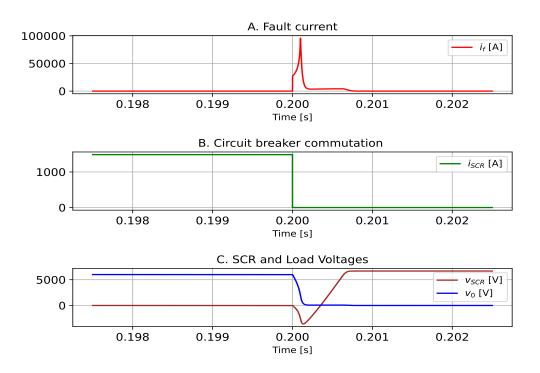


Figure 4.40: Bi-directional topology based on the series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltage (v_C) , inductor voltage (v_L) , load current (i_{RL}) , and source current (i_s) of Bi-directional topology based on the series Z-source behavior are depicted in Figure 4.41. Figure 4.41 A) corresponds to capacitor current i_C , inductor current i_L . When the transient current of the capacitor i_C reaches the steady state current of the inductor i_L is observed. In this time, the commutation occurs. After the disconnection, capacitor and inductor currents are the same because they are connected in series. Figure 4.41 B) corresponds to capacitors voltage v_C and inductors voltage v_L . The series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero and the current in the inductor decays to zero intending to become negative. Figure 4.41 C) corresponds to load current i_{RL} and source current voltage i_s . The current in the load is observed to instantaneously drop to zero. However, the current in the source experiences an increasing which can be harmful to the source. This current increase is caused by the series resonance through C, L_2 and D_4 connected to the fault.

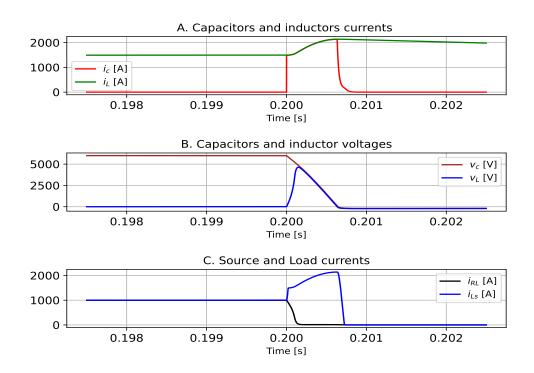


Figure 4.41: Bi-directional topology based on the series Z-source behavior i_c , i_L , v_c , v_L , i_{RL} , i_{Ls}

4.3.3 Result Bi-directional topology based on the series Z-source

Figure 4.42 shows the implementation of Bi-directional topology based on the series Z-source in OpenModelica, this topology was explained and described in section 3.3.1 and corresponds to Figure 3.15. This topology is only analyzed up to the commutation. This is because it requires a complex control system to obtain the stability of the circuit after commutation.

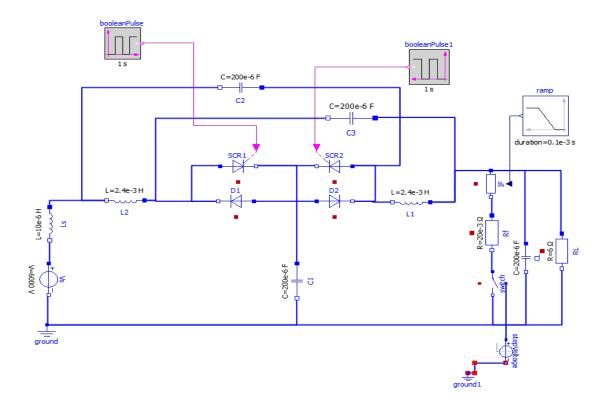


Figure 4.42: OpenModelica simulation of Bi-directional topology based on the series Z-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bidirectional topology based on the series Z-source are depicted in Figure 4.43. Figure 4.43 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.43 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. In Figure 4.43 C), The instability produced in SCR voltage and the load due to the effect of the capacitors and inductances is observed. This topology requires a control system to stabilize the variables.

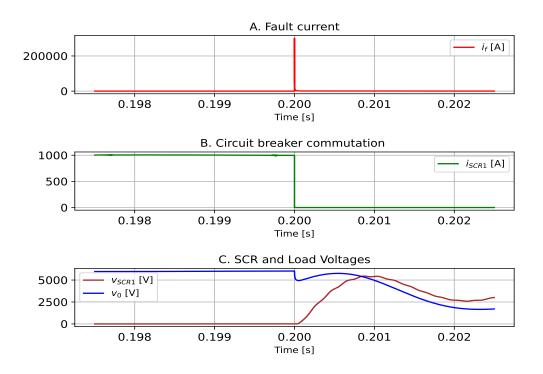


Figure 4.43: Bi-directional topology based on the series Z-source behavior i_f , i_{SCR} , v_{SCR} , v_0

4.3.4 Result Bi-directional topology based on T-source

Figure 4.42 shows the implementation of Bi-directional topology based on T-source in Open-Modelica, this topology was explained and described in section 3.3.2 and corresponds to Figure 3.16.

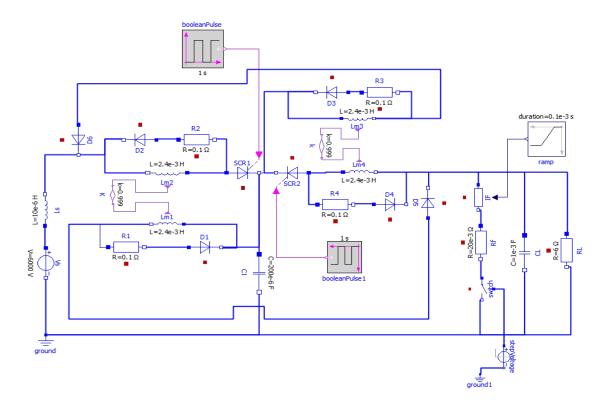


Figure 4.44: OpenModelica simulation of Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bi-directional topology based on T-source are depicted in Figure 4.45. Figure 4.45 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.45 B) corresponds to the SCR current i_{SCR} . It should be noted that the current flowing through the SCR is higher than the current in the load due to the currents passing through the blocking diodes D_6 , as shown in Figures 4.45. This effect increases the steady-state losses of the SCR which needs to be considered when selecting the SCR size. Furthermore, a higher fault clearance current is required compared to other topologies. Before fault occurrence, i_{RL} has a value of 1.000A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly drops to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage v_0 are depicted in Figure 4.45 C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared the load voltage decays to zero.

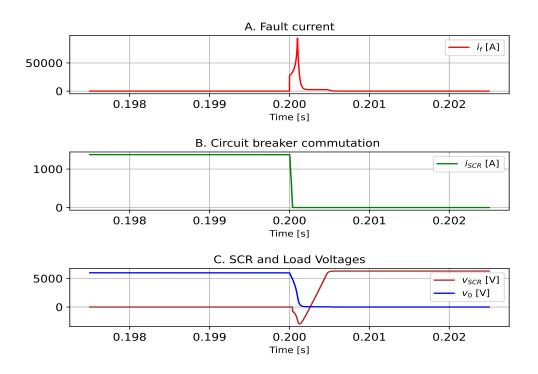


Figure 4.45: Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of Bi-directional topology based on T-source behavior are depicted in Figure 4.46. It is important to know that the couplings are part of the commutation path in this topology. Figure 4.46 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this time, the commutation occurs. After the disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.46 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues to circulate in the circuit snubber. In Figure 4.46 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred the current in the source immediately decays to zero and the current in the load also decays.

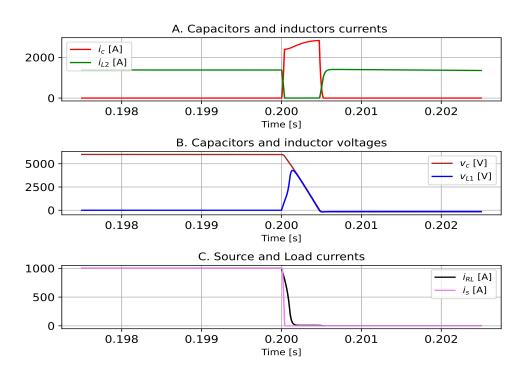


Figure 4.46: Bi-directional topology based on T-source behavior i_c , i_{L2} , v_c , v_{L1} , i_{RL} , i_s

4.3.5 Result Bi-directional topology based on T-source

Figure 4.47 shows the implementation of Bi-directional topology based on T-source in Open-Modelica, this topology was explained and described in section 3.3.2 and corresponds to Figure 3.17.

COMPARISON OF ELECTRICAL FAULT RESPONSES IN Z-SOURCE CIRCUIT BREAKER TOPOLOGIES FOR D.C. MICROGRID APPLICATIONS.

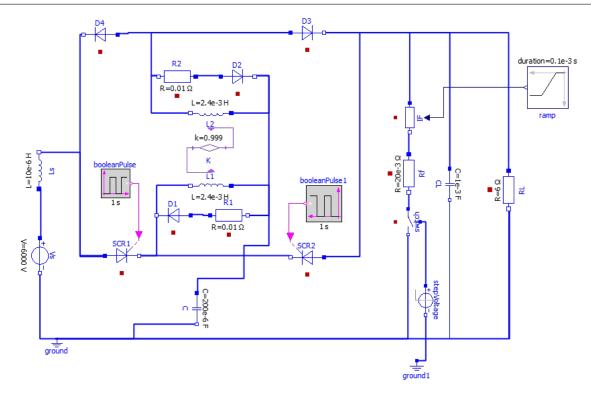


Figure 4.47: OpenModelica simulation of Bi-directional topology based on T-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bidirectional topology based on T-source are depicted in Figure 4.48. Figure 4.48 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.48 B) corresponds to the SCR current i_{SCR} . It should be noted that the current flowing through the SCR is higher than the current in the load due to the currents passing through the blocking diodes D_4 , as shown in Figure 4.48. This effect increases the steady-state losses of the SCR and needs to be considered when selecting the SCR size. Furthermore, a higher fault clearance current is required compared to other topologies. Before fault occurrence, i_{RL} has a value of 1.000A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly drops to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage v_0 are depicted in Figure 4.48 C). A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared, the load voltage decays to zero.

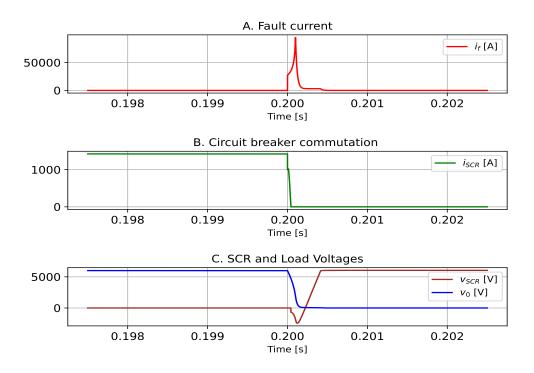


Figure 4.48: Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) , load current (i_{RL}) and source current (i_s) of Bi-directional topology based on T-source behavior are depicted in Figure 4.49. It is important to know that the couplings are part of the commutating path in this topology. Figure 4.49 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this time, the commutation occurs. After the disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.49 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series reso-

nance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues to circulate in the circuit snubber. In Figure 4.49 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred, the current in the source immediately decays to zero and the current in the load also decays.

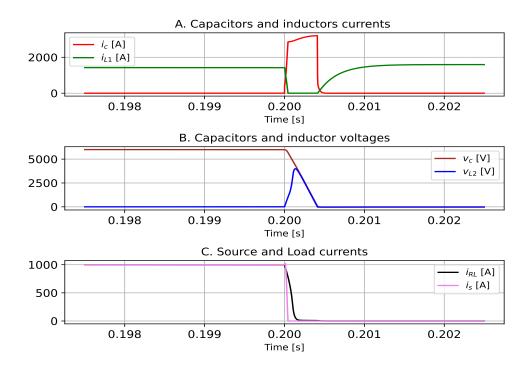


Figure 4.49: Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{RL} , i_s

4.3.6 Result Bi-directional topology based on T-source

Figure 4.50 shows the implementation of Bi-directional topology based on T-source in Open-Modelica, this topology was explained and described in section 3.3.2 and corresponds to Figure 3.18.

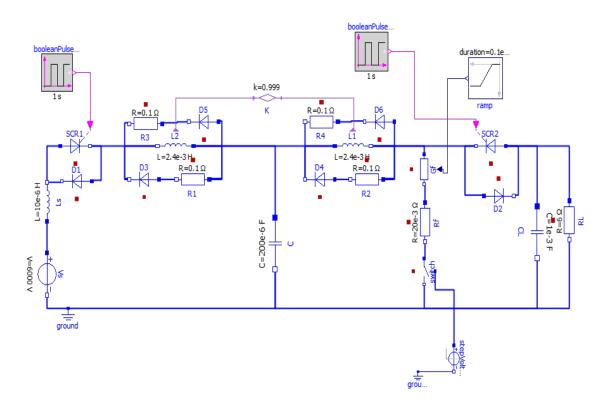


Figure 4.50: OpenModelica simulation Bi-directional topology based on T-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bi-directional topology based on T-source are depicted in Figure 4.51. Figure 4.51 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. This topology presents low fault current compared to the other topologies. Figure 4.51 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure 4.51 C). A zero crossing of v_{SCR} is observed which is very important for SCR protection. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared, the load voltage drops to zero but slower than the other topologies.

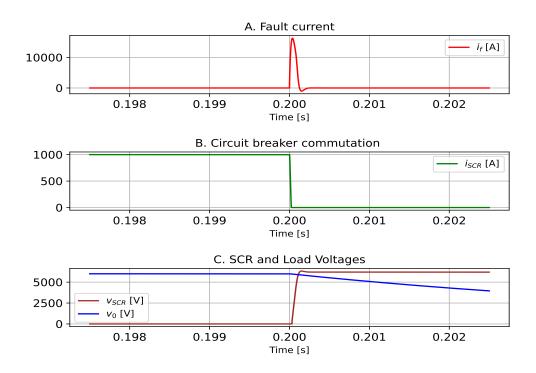


Figure 4.51: Result Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current (i_c) , inductor current (i_L) , capacitor voltages (v_C) , inductor voltage (v_L) of Bi-directional topology based on T-source are depicted in Figure 4.52. In Figure 4.52 A), the behavior of the currents are depicted. The inductor L_1 induces in L_2 a current that is supplied by the capacitor C. In Figure 4.52 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero and intend to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues circulating in the circuit snubber. In Figure 4.52 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred, the current in the source immediately decays to zero; however the current in the load decreases more slowly than in the previous topologies.

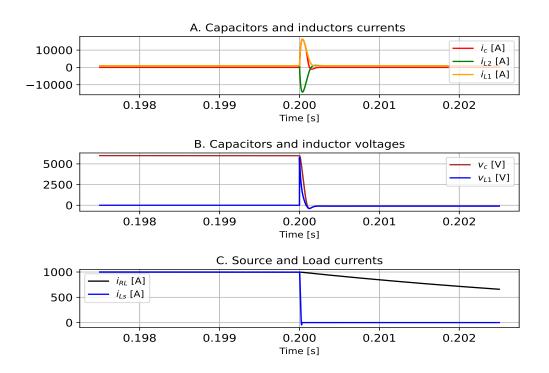


Figure 4.52: Result Bi-directional topology based on T-source behavior i_c , i_{L1} , i_{L2} , v_c , v_{L1} , i_{RL} , i_s

4.3.7 Result simulation of Bi-directional topology based on T-source

Figure 4.53 shows the implementation of Bi-directional topology based on T-source in Open-Modelica, this topology was explained and described in section 3.3.2 and corresponds to Figure 3.19.

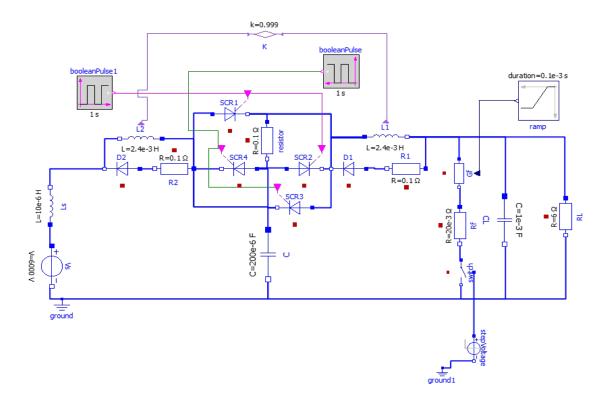


Figure 4.53: Bi-directional topology based on T-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_0) of Bi-directional topology based on T-source are depicted in Figure 4.54. Figure 4.54 A) corresponds to the fault current i_f . fault current of this topology is similar to the fault current of the classical Z-source. Figure 4.54 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases similar to the classic Z-source. Note that in Figure 4.54 C), v_{SCR} voltage crosses zero and then stabilizes.

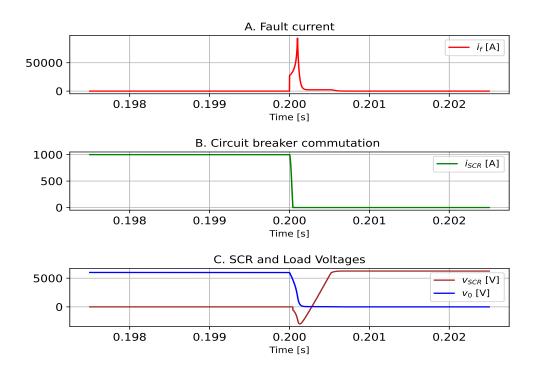


Figure 4.54: Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor current(i_c), inductor current (i_L), capacitor voltages (v_C), inductor voltage(v_L), load current (i_{RL}) and source current (i_s) of Bi-directional topology based on T-source behavior are depicted in Figure 4.55. Figure 4.55 A) shows the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this time, the commutation occur. After the disconnection, capacitor and inductor currents are the same because they are connected in series. In Figure 4.55 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues circulating in the circuit snubber. In Figure 4.55 C), the behavior of the current in the source i_s and the current in the load i_{LS} are depicted. Once fault clearance has occurred the current in the source immediately decays to zero and the current in the load also decays.

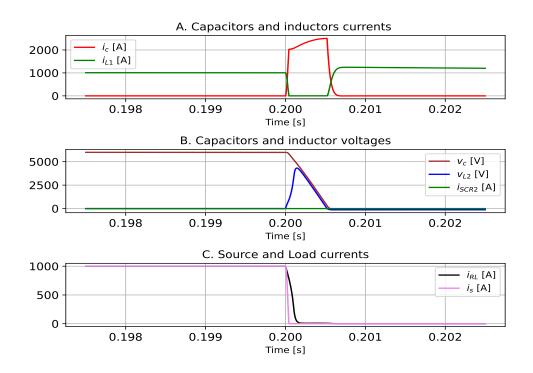


Figure 4.55: Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{SCR2} , i_{RL} , i_s

4.3.8 Result simulation of Bi-directional topology based on T-source

Figure 4.56 shows the implementation of Bi-directional topology based on T-source in Open-Modelica, this topology was explained and described in section 3.3.2 and corresponds to Figure 3.20

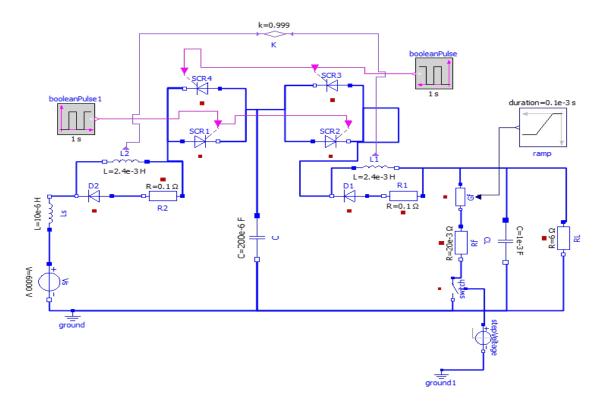


Figure 4.56: OpenModelica simulation of Bi-directional topology based on T-source

Fault current (i_f) , SCR current (i_{SCR}) , SCR voltage (v_{SCR}) and load voltage (v_L) of Bi-directional topology based on T-source are depicted in Figure 4.58. Figure 4.58 A) corresponds to the fault current i_f . Fault occurs in 0.2 s. Please note that i_f rises to a maximum value and then decreases. When the fault current is increasing, fault clearing events occur in the circuit. When the fault current is decreasing, resonance events occur followed by energy dissipation events in the circuit. Figure 4.58 B) corresponds to the SCR current i_{SCR} . Before fault occurrence, i_{SCR} has a value of 1.000 A which corresponds to the normal operation of the circuit. After fault occurrence, i_{SCR} rapidly decreases to zero for clearing the fault. The commutation process is almost instantaneous and occurs when the fault current increases. Voltage in SCR v_{SCR} and load voltage (v_0) are depicted in Figure ?? C. A zero crossing of v_{SCR} is observed which is very important for SCR protection. When v_{SCR} crosses zero, the arc generated during switching is mitigated, similar to what happens in AC circuits. In addition, the load voltage v_0 behavior is observed. Once the fault is cleared the load voltage decays to zero, please see blue line.

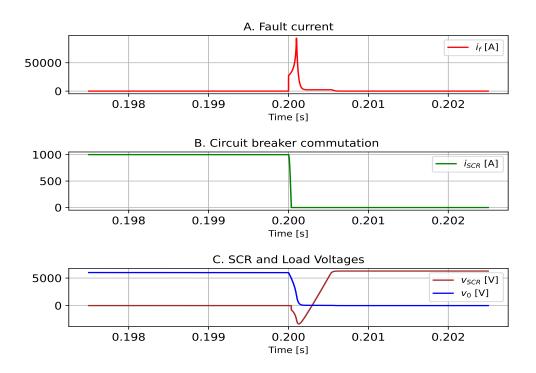


Figure 4.57: Bi-directional topology based on T-source behavior i_f , i_{SCR} , v_{SCR} , v_0

Capacitor currents (i_c) , inductor currents (i_L) , capacitor voltages (v_C) , inductor voltages (v_L) , load current (i_{RL}) , SCR current (i_{SCR2}) and source current (i_s) of Bi-directional topology based on T-source are depicted in Figure 4.58. Figure 4.58 A) corresponds to the moment when the transient current of the capacitor reaches the steady state current of the inductor is observed. In this instant time, the commutation occurs. After the disconnection, capacitor current and inductor current are equal because they are connected in series. In Figure 4.58 B), the series resonance lapse is observed. When the inductor voltage is equal to the capacitor voltage, the series resonance time occurs. Note that when the voltage across the inductor goes negative, a reverse current appears that turns off the SCR_2 please see i_{SCR2} green line. Once the resonance is finished, the voltage across the capacitor decays to zero, inductor voltage decays to zero intending to become negative. Once the resonance is finished, the current across the capacitor decays to zero and the current in the inductor continues circulating in the circuit snubber. In Figure 4.58 C), the behavior of the current in the source and the current in the load are depicted. Once fault clearance has occurred, the current in the source immediately decays to zero and the current in the load drops to zero.

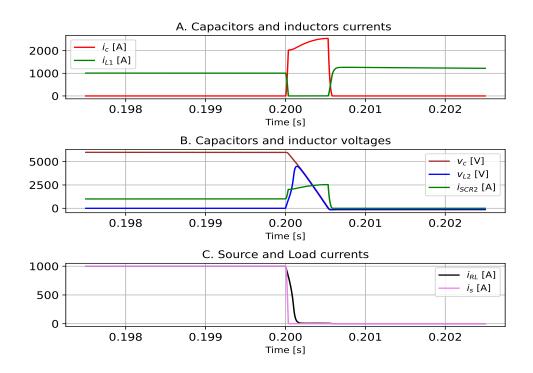


Figure 4.58: Bi-directional topology based on T-source behavior i_c , i_{L1} , v_c , v_{L2} , i_{SCR2} , i_{RL} , i_s

Chapter 5

Comparative analysis, discussion and future challenges

5.1 Introduction

In this chapter, a comparative analysis of results is presented, focusing on the evaluation of various parameters in different Z-source topologies. First, there is a comparative analysis section, then a discussion section, and finally a future challenges section. The abbreviations of these parameters are listed in Table 5.1 for reference and ease of understanding. The comparison data is divided into three tables, with the simulation results for mono-directional topologies presented in Tables 5.2, and 5.3 and the comparative data for bi-directional topologies provided in Table 5.4. This chapter aims to provide a detailed comparison and analysis of the different topologies to now their performance in medium voltage DC microgrids.

5.2 Comparative analysis

Topologies are evaluated based on parameters such as Energization Current (EC), Fault Clearing Time (FCT), Maximum current in the source by series resonance (MRSC), Total Inductance (TI), Galvanic Isolation (GI), Number of Capacitors (NC), Number of Inductors (NI), Number of Diodes (ND), Number of Resistors (NR), Number of SCR (NSCR), Number of SCR in conduction (NSSCR), Number of Couplings (Ncoup), and Load Variation (LV). The description of the parameters are summarized in the Table 5.1.

Description	Abbreviation
Energization Current [A]	EC
Fault Clearing Time $[\mu s]$	FCT
Maximum Resonance Source Current [A]	MRSC
Total Inductance [mH]	TI
Galvanic Isolation	GI
Number of Capacitors	NC
Number of Inductors	NI
Number of Diodes	ND
Number of Resistors	NR
Number of SCR	NSCR
Number of SCR in conduction	NSSCR
Number of Couplings	NCoup
Load Variation	LV

Table 5.1: Table with Descriptions and Abbreviations

Table 5.2 presents the data obtained for the mono-directional topologies represented in Figures 3.1 to 3.7.

Parameter	F3.1	F3.3	F3.4	F3.5	F3.6	F3.7
EC	1675	1691	1581	1468	1600	1670
FCT	12	12	2	2	86	27
MRSC	0	3884	1875	50	0	0
TI	4.8	4.8	4.8	9.6	4.8	2.4
GI	N	N	N	Ν	Ν	Y
NC	2	2	2	3	3	2
NI	2	2	2	4	2	2
ND	2	2	2	4	2	2
NR	2	2	2	4	4	2
NSCR	1	1	1	2	1	1
NSSCR	1	1	1	2	1	1
Ncoup	N	N	N	Ν	Ν	1
LV	N	N	Y	Ν	Ν	Ν

Table 5.2: Comparative table of mono-directional topologies

Table 5.3 presents the data obtained for the mono-directional topologies represented in Figures 3.8 to 3.12.

Parameter	F3.8	F3.9	F3.10	F3.11	F3.12	
EC	1579	1510	1640	1817	1738	
FCT	2	34	32	61	56	
MRSC	1853	0	0	0	2217	
TI	2.4	2.4	4.8	24	4.2	
GI	Y	Y	Y	Y	Y	
NC	2	1	1	1	1	
NI	2	2	2	2	2	
ND	2	2	2	1	1	
NR	2	2	2	1	1	
NSCR	1	1	1	1	1	
NSSCR	1	1	1	1	1	
Ncoup	1	1	1	1	1	
LV	Y	Y	Y	Y	Y	

Table 5.3: Comparative table of mono-directional topologies

Table 5.4 presents the data obtained for the mono-directional topologies represented in Figures 3.13 to 3.20.

Parameter	F3.13	F3.14	F3.15	F3.16	F3.17	F3.18	F3.19	F3.20
EC	1449	1527	4000	1489	1500	1000	1445	1500
FCT	2	3	3	38	42	3	41	34
MRSC	1940	2138	N/A	0	1200	0	0	0
TI	9.6	4.8	4.8	9.6	4.8	4.8	4.8	4.8
GI	N	N	Ν	Y	Y	Y	Y	Y
NC	4	2	3	1	1	1	1	1
NI	4	2	2	4	2	2	2	2
ND	4	6	2	6	4	6	2	0
NR	4	2	0	4	2	4	3	0
NSCR	2	1	2	2	2	2	4	4
NSSCR	1	1	1	1	1	1	1	2
Ncoup	N	N	Ν	2	1	1	1	1
LV	Ν	Ν	Ν	Y	Y	Y	Y	Y

Table 5.4: Comparative table of bi-directional topologies

5.3 Discussion

The most important factors for DC circuit breakers within the context of the selected topologies are as follows. Firstly, rapid fault clearing is crucial due to the sensitivity of power converters to sudden current increases. Tables 5.2, 5.3, and 5.4 that correspond for both unidirectional and bidirectional topologies, it can be observed that all topologies exhibit fast fault clearing times of less than 100μ s. Secondly, mitigating the arc generated during disconnection is a significant concern due to the absence of zero-crossing of DC current. While high switching speeds are beneficial in preventing arc issues, achieving automatic zero-crossing and providing additional safety for the circuit breakers. Indeed, it is evident that all the unidirectional and bidirectional topologies generate a zero-crossing in the SCR voltage, effectively reducing the risk of damage from arc generation during the commutation, which could be observed in the figures depicted in result section. The peak current that occurs when energizing the circuit breaker is important, as this behavior repeats when the circuit breaker is reactivated after switching. According to Tables 5.2 and 5.3 for the unidirectional topology, there is no significant difference among the topologies, as they all exhibit current spikes close to 1.500A. Nonetheless, Table 5.4 shows a significantly lower energization current for the topology in Figure 3.18 compared to the others. It should be noted that reducing the energization peak requires the addition of resistors to the capacitors, which in turn increases losses during the switching state. Some topologies were proposed without including the effects of the source inductance. In the present project, it was confirmed that the source inductance is a variable that should be included in every topology. The series resonance between the source inductance and a capacitor in the circuit breaker can generate currents that can damage the source. For mono-directional topologies, as shown in Tables 5.2 and 5.3, there is an increasing in source current due to resonance that is greater than 50%, these were observed for the topologies represented in Figures 3.3, 3.4, 3.8, and 3.12. These topologies have a discharged capacitor in series with the source that does not make contact with the negative pole of the circuit. In Table 5.4, for bi-directional topologies, similar increasing of source current occurs due to resonance that is greater than $50^{\circ}\%$, these were observed for topologies 3.13 and 3.14. The source inductance varies for each application, and as the inductance increases, the resonant current reflected by the source can also increase. This implies that topologies exhibiting behaviors associated with the source inductance cannot be implemented in general applications, but rather only in applications where the source inductance is known. Another important factor for selecting a circuit breaker for DC microgrids is the inherent heating losses of power electronics solid-state devices. In this project, a comparison was made between mono-directional and bi-directional topologies, taking into account the number of SCRs carrying the steady-state current. The resistors accompanying the capacitors and the resistors in the damping circuits experience heating, but only during transients when commutation occurs. Nonetheless, when analyzing heating losses, the diodes carrying current in steady state are important. The topology shown in Figure 3.11 (τ -source) presents considerable advantages compared to other topologies, as it has fewer components and does not reflect current back to the source. However, despite this topology have a capacitor current similar compared to currents of the other topologies, the total inductance had to be increased by a factor of 5.7. For this reason, the total circuit inductance was included as a comparative factor to observe changes in the amount of material required when comparing

under similar conditions with other topologies. This implies a larger amount of material

116

needs to be carefully examined. The T-source topology also has advantages, as only a part of the circuit remains in resonance when the SCR commutates off. The bidirectional topologies shown in Figures 3.16 and 3.17 exhibit minimal losses due to material reduction. However, the circuit shows a current re-circulation through the SCR, which increases conduction losses. The topology in Figure 3.19 increases the initial costs by using four SCRs in the circuit in exchange which reduces conduction losses, as only one out of the four SCRs conducts the steady-state current. On the other hand, the topology in Figure 3.20 decreases the commutation losses by using SCRs, due to rapidly decreasing the resonance time by adding an additional SCR that opens the final series resonance circuit. However, this topology includes two SCRs that are conducting in steady state, which increases conduction losses. In general, there is a significant advantage observed in topologies that utilize magnetic couplings. The use of couplings allows to reduce the material used in inductors, enable the adjustment of the number of turns to achieve abrupt changes in load current, and provide the possibility of galvanic isolation, as current flow between the part of the circuit in which the circuit breaker is located and the rest of the system can be prevented [47]. It is important to add that one of the characteristics of the Z-source topology is that the switching depends on the failure time, as well as on the speed of the failure. It also depends on the resistance of the failure material. These limitations make the switch circuit unable to operate in all situations. Until now, the circuit breakers operate in controlled environments or in specific circuits.

5.4Future challenges

Research on topologies for Z-source-based circuit breakers is growing, as there is a need to overcome several obstacles to achieve optimal performance. The following are some future challenges:

- In order to simulate the fault currents of the z-source topology and derived topology, studies on DC fault times are required to model the faults with greater accuracy.
- Conducting studies on the behavior of Z-source switch circuits utilizing capacitive grounding meshes is crucial. The utilization of capacitive meshes offers the potential to achieve improved fault-clearing speeds in Z-source topologies and effectively mitigate the time dependency of the system during switching. By exploring these aspects, we can enhance the performance and reliability of Z-source switch circuits.
- Most of the topologies are simulated in laboratories with low voltage elements and it is necessary to do further experiments at medium voltage levels in the presence of real parasitic capacitances.
- Recent research proposes to improve the performance of the Z-source topology and its modifications by integrating solid-state devices with complex control and high conduction losses. Hence the importance of continuing the efforts to obtain the best performance of the circuit breakers, preserving the natural commutation with SCR and only additional passive elements

Chapter 6

Conclusions

- In the development of this project, 19 Z-source topologies and derived topologies that preserve the switching principle of the classical Z-source circuit breaker were selected and compared. The topologies were classified into two categories: Unidirectional and Bidirectional, based on the proposed solutions. Within each group, they were further classified into topologies that utilize magnetic coupling and topologies that do not utilize magnetic coupling.
- The OpenModelica software was utilized for conducting simulations of the different topologies, and the figures were edited using the Matplotlib package of the Python software, resulting in favorable outcomes.
- The behavior of all topologies was analyzed and simulated, resulting in figures that provide an understanding of the different operational stages of the topologies, including steady-state operation, resonance period, and energy dissipation. Furthermore, specific simulation parameters for a medium-voltage DC microgrid were used, which were consistent across all topologies.
- The results were separated for mono-directional and bi-directional topologies, considering as analysis variables: Energization Current, Fault Clearing Time, Maximum current in the source by series resonance, Total Inductance, Galvanic Isolation, Number of Capacitors, Number of Inductors, Number of Diodes, Number of Resistors, Number of SCRs, Number of SCRs in conduction, Number of Couplings, and Load Variation.

It was possible to observe that the Z-sources topologies and their modifications have solved two fundamental problems of direct current switching circuits, such as the problem of rapid fault clearance with few losses and the problem of the arc generated in switching due to the absence of zero crossing direct current. For a DC microgrid, it is expected that the fault clearance does not last longer than 0.1ms and the fault clearance times from the simulations do not exceed 100τ s

• It was possible to observe that the topologies with magnetic couplings have an advantage over their counterparts without couplings, since they allow to optimize the amount of materials, they can be configured for load variations, they can provide galvanic isolation and they are easy to build.

• Z-source topologies have a great limitation in terms of their dependence on the time of the fault current and the fault resistance, since these variables depend on the electrical installation, for which reason it is still necessary to investigate the specific cases of implementation that guarantee the correct behavior of the circuit breakers.

118

• Z-source topologies and their modifications are strong candidates for the predictions of DC microgrids, but further experimentation is still needed to move from prototype developments to implementations in real medium voltage microgrids.

Chapter 7

Abbreviations

The following abbreviations are used in this manuscript:

Alternating Current
Alternating Current Microgrids
Artificial current zero vacuum switch
Artificial Current Zero
Bi-directional
Bipolar junction transistor
Base resistance thyristor
Capacitance
Circuit Breakers
Cathode Metal oxide Semiconductor Controlled Thyristor
Direct Current
Direct Current Microgrids
Distributed Generation
Gallium Nitride
Gate-Turn-off Thyristors
Hybrid Circuit Breakers
High-Electron-Mobility Transistor
Intelligent tri-mode SSCB
Injection-Enhanced Gate Transistor
Silicon Insulated-Gate Bipolar Transistor
Integrated Gate-Commutated Thyristor
Junction-Gate Field Effect Transistor
Inductance
Mechanical Circuit Breakers
Metal-Oxide Semiconductor Field Effect Transistors
Metal Oxide Varistor
Protective Devices
Photovoltaic Panel
Pulse Width Modulation
Reverse Blocking IGCT
Resistor and Capacitor
Resistor, Capacitor and Diode
On-Resistance value during operation
Semiconductor Controlled Rectifier
Silicon
Silicon Carbide
Static Induction Transistors
solid-state Circuit Breaker Latching and Current Limiting
Solid-state Circuit Breakers
T-Z-Source Circuit Breakers
Vacuum CBs
Wide Band Gap
Z-Source Circuit Breakers
Silicon Carbide Substrate, Crystal Structure 4H

Bibliography

- Sijo Augustine, Jimmy Edward Quiroz, Matthew J. Reno, and Sukumar Brahma. Dc microgrid protection: Review and challenges. Technical report, U.S. Department of Energy Office of Scientific and Technical Information, United States, 8 2018.
- [2] B. Bachmann, G. Mauthe, E. Ruoss, H.P. Lips, J. Porter, and J. Vithayathil. Development of a 500kv airblast hvdc circuit breaker. *IEEE Transactions on Power Apparatus* and Systems, PAS-104(9):2460–2466, 1985.
- [3] B.J. Baliga. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters*, 10(10):455–457, 1989.
- [4] Navid Bayati, Hamid Reza Baghaee, Amin Hajizadeh, and Mohsen Soltani. A fuse saving scheme for dc microgrids with high penetration of renewable energy resources. *IEEE Access*, 8:137407–137417, 2020.
- [5] Navid Bayati, Amin Hajizadeh, and Mohsen Soltani. Impact of faults and protection methods on dc microgrids operation. In 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I CPS Europe), pages 1–6, 2018.
- [6] Siavash Beheshtaein and Robert Cuzner. A new y- igct-based dc circuit breaker for nasa n3-x spacecraft. In 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1215–1218, 2021.
- [7] Siavash Beheshtaein, Robert M. Cuzner, Mojtaba Forouzesh, Mehdi Savaghebi, and Josep M. Guerrero. Dc microgrid protection: A comprehensive review. *IEEE Journal* of Emerging and Selected Topics in Power Electronics, pages 1–1, 2019.
- [8] Siavash Beheshtaein, Mehdi Savaghebi, Juan Carlos Vasquez, and Josep M. Guerrero. Protection of ac and dc microgrids: Challenges, solutions and future trends. In *IECON* 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, pages 005253– 005260, 2015.
- [9] Duong Minh Bui, Shi-Lin Chen, Chi-Hua Wu, Keng-Yu Lien, Chen-Ho Huang, and Kuo-Kuang Jen. Review on protection coordination strategies and development of an effective protection coordination system for dc microgrid. In 2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), pages 1–10, 2014.
- [10] Arthur H. Chang, Brian R. Sennett, Al-Thaddeus Avestruz, Steven B. Leeb, and James L. Kirtley. Analysis and design of dc system protection using z-source circuit breaker. *IEEE Transactions on Power Electronics*, 31(2):1036–1049, 2016.

- [11] Keith A. Corzine. A new-coupled-inductor circuit breaker for dc applications. IEEE Transactions on Power Electronics, 32(2):1411–1418, 2017.
- [12] Keith A. Corzine and Robert W. Ashton. A new z-source dc circuit breaker. In 2010 IEEE International Symposium on Industrial Electronics, pages 585–590, 2010.
- [13] Keith A. Corzine and Robert W. Ashton. Structure and analysis of the z-source mvdc breaker. In 2011 IEEE Electric Ship Technologies Symposium, pages 334–338, 2011.
- [14] Keith A. Corzine and Robert W. Ashton. A new z-source dc circuit breaker. IEEE Transactions on Power Electronics, 27(6):2796–2804, 2012.
- [15] Keith A. Corzine and Robert W. Ashton. A new z-source dc circuit breaker. IEEE Transactions on Power Electronics, 27(6):2796–2804, 2012.
- [16] Rob Cuzner, Doug MacFarlin, Don Clinger, Michael Rumney, and Gene Castles. Circuit breaker protection considerations in power converter-fed dc systems. In 2009 IEEE Electric Ship Technologies Symposium, pages 360–367, 2009.
- [17] Robert M. Cuzner and Giri Venkataramanan. The status of dc micro-grid protection. In 2008 IEEE Industry Applications Society Annual Meeting, pages 1–8, 2008.
- [18] Xiaoguang Diao, Fei Liu, Yuan Song, Mengyue Xu Yizhan Zhuang, Wenkun Zhu, and Xiaoming Zha. A new efficient bidirectional t-source circuit breaker for flexible dc distribution networks. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pages 1–1, 2020.
- [19] Daniel R. Doan. Arc flash calculations for exposures to dc systems. *IEEE Transactions on Industry Applications*, 46(6):2299–2302, 2010.
- [20] Tomislav Dragicevic, Juan C. Vasquez, Josep M. Guerrero, and Davor Skrlec. Advanced lvdc electrical power architectures and microgrids: A step toward a new generation of power distribution networks. *IEEE Electrification Magazine*, 2(1):54–65, 2014.
- [21] Tomislav Dragičević, Xiaonan Lu, Juan C. Vasquez, and Josep M. Guerrero. Dc microgrids—part ii: A review of power architectures, applications, and standardization issues. *IEEE Transactions on Power Electronics*, 31(5):3528–3549, 2016.
- [22] Hilding Elmqvist, Sven Erik Mattsson, and Martin Otter. Object-oriented and hybrid modeling in modelica. Journal Européen des systèmes automatisés, 35(4):395–404, 2001.
- [23] Abdullah A. S. Emhemed, Kenny Fong, Steven Fletcher, and Graeme M. Burt. Validation of fast and selective protection scheme for an lvdc distribution network. *IEEE Transactions on Power Delivery*, 32(3):1432–1440, 2017.
- [24] Steven D. A. Fletcher, Patrick J. Norman, Kenny Fong, Stuart J. Galloway, and Graeme M. Burt. High-speed differential protection for smart dc distribution systems. *IEEE Transactions on Smart Grid*, 5(5):2610–2617, 2014.
- [25] Zheng Ganhao. Study on dc circuit breaker. In 2014 Fifth International Conference on Intelligent Systems Design and Engineering Applications, pages 942–945, 2014.

- [26] H Giuliani, C Kral, JV Gragger, and F Pirker. Modelica simulation of electric drives for vehicular applications-the smart drives library. ASIM, Erlangen, 2005.
- [27] Yanxun Guo, Gang Wang, Dehui Zeng, Haifeng Li, and Hong Chao. A thyristor fullbridge-based dc circuit breaker. *IEEE Transactions on Power Electronics*, 35(1):1111– 1123, 2020.
- [28] Venkata Raghavendra I, Satish Naik Banavath, and Sreekanth Thamballa. Modified z-source dc circuit breaker with enhanced performance during commissioning and reclosing. *IEEE Transactions on Power Electronics*, 37(1):910–919, 2022.
- [29] IEEE. Recommended practice for the design of dc power systems for stationary applications. IEEE Std 946-2020 (Revision of IEEE Std 946-2004), pages 1–74, 2020.
- [30] Noriyuki Iwamuro and Thomas Laska. Igbt history, state-of-the-art, and future prospects. *IEEE Transactions on Electron Devices*, 64(3):741–752, 2017.
- [31] Davood Keshavarzi, Ebrahim Farjah, and Teymoor Ghanbari. Hybrid dc circuit breaker and fault current limiter with optional interruption capability. *IEEE Transactions on Power Electronics*, 33(3):2330–2338, 2018.
- [32] Davood Keshavarzi, Teymoor Ghanbari, and Ebrahim Farjah. A z-source-based bidirectional dc circuit breaker with fault current limitation and interruption capabilities. *IEEE Transactions on Power Electronics*, 32(9):6813–6822, 2017.
- [33] Aivars J. Lelis, Ron Green, Daniel B. Habersat, and Mooro El. Basic mechanisms of threshold-voltage instability and implications for reliability testing of sic mosfets. *IEEE Transactions on Electron Devices*, 62(2):316–323, 2015.
- [34] Tao Li and Qiming Cheng. A comparative study of z-source inverter and enhanced topologies. CES Transactions on Electrical Machines and Systems, 2(3):284–288, 2018.
- [35] Tao Li, Yongli Li, and Ningning Liu. A new topological structure of z-source dc circuit breaker. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69:3294–3298, 2022.
- [36] Di Liu, Dimitrios Tzelepis, and Adam Dyśko. Protection of microgrids with high amounts of renewables: Challenges and solutions. In 2019 54th International Universities Power Engineering Conference (UPEC), pages 1–6, 2019.
- [37] Fei Liu, Wenjun Liu, Xiaoming Zha, Hua Yang, and Kun Feng. Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage dc microgrid. *IEEE Transactions on Power Electronics*, 32(4):3007–3021, 2017.
- [38] Laurens Mackay, Nils H. van der Blij, Laura Ramirez-Elizondo, and Pavol Bauer. Toward the universal dc distribution system. *Electric Power Components and Systems*, 45(10):1032–1042, 2017.

- [39] H. Alan Mantooth, Osama Saadeh, Erik Johnson, Juan C. Balda, Simon S. Ang, Alexander B. Lostetter, and Roberto M. Schupbach. Solid-state fault current limiters: Silicon versus silicon carbide. In 2008 IEEE Power and Energy Society General Meeting -Conversion and Delivery of Electrical Energy in the 21st Century, pages 1–5, 2008.
- [40] Atif Maqsood and Keith Corzine. Z-source dc circuit breakers with coupled inductors. In 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pages 1905–1909, 2015.
- [41] Atif Maqsood and Keith Corzine. Application of a new coupled-inductor based dc circuit breaker. In 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), pages 1390–1393, 2017.
- [42] Atif Maqsood, Lu Li, and Keith A. Corzine. Low-voltage dc testbed design for a zsource breaker based protection scheme. In 2016 Clemson University Power Systems Conference (PSC), pages 1–6, 2016.
- [43] Atif Maqsood2015 and Keith Corzine. Z-source dc circuit breakers with coupled inductors. In 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pages 1905–1909, 2015.
- [44] Atif Maqsood20161, Allan Overstreet, and Keith A. Corzine. Modified z-source dc circuit breaker topologies. *IEEE Transactions on Power Electronics*, 31(10):7394–7403, 2016.
- [45] David Marroqui, Ausias Garrigos, Jose M. Blanes, and Roberto Gutierrez. Photovoltaicdriven sic mosfet circuit breaker with latching and current limiting capability. *Energies*, 12(23), 2019.
- [46] Witness A. Martin, Cheng Deng, Dimas Fiddiansyah, and Juan Carlos Balda. Investigation of low-voltage solid-state dc breaker configurations for dc microgrid applications. In 2016 IEEE International Telecommunications Energy Conference (INTELEC), pages 1–6, 2016.
- [47] Stephen Mazich. Galvanic isolation.
- [48] A. Meghwani, S. C. Srivastava, and S. Chakrabarti. A non-unit protection scheme for dc microgrid based on local measurements. *IEEE Transactions on Power Delivery*, 32(1):172–181, 2017.
- [49] C. Meyer, M. Kowal, and R.W. De Doncker. Circuit breaker concepts for future highpower dc-applications. In *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, volume 2, pages 860–866 Vol. 2, 2005.
- [50] José Millán, Philippe Godignon, Xavier Perpiñà, Amador Pérez-Tomás, and José Rebollo. A survey of wide bandgap power semiconductor devices. *IEEE Transactions on Power Electronics*, 29(5):2155–2163, 2014.
- [51] Julia Niewind, Nasser G.A. Hemdan, Christoph Klosinski, Dirk Bösche, Michael Kurrat, Frank Gerdinand, Johann Meisner, and Stephan Passon. Operation and protection of 380v dc distribution systems. In 2017 IEEE Manchester PowerTech, pages 1–6, 2017.

- [52] Henry W Ott. *Electromagnetic compatibility engineering*. John Wiley & Sons, 2011.
- [53] Allan Overstreet, Atif Maqsood, and Keith Corzine. Modified z-source dc circuit breaker topologies. In 2014 Clemson University Power Systems Conference, pages 1–6. IEEE, 2014.
- [54] Karthik Palaniappan, Willy Sedano, Mark Vygoder, Nicholas Hoeft, Robert Cuzner, and Z. John Shen. Short-circuit fault discrimination using sic jfet-based self-powered solid-state circuit breakers in a residential dc community microgrid. *IEEE Transactions* on Industry Applications, 56(4):3466–3476, 2020.
- [55] Jae-Do Park and Jared Candelaria. Fault detection and isolation in low-voltage dc-bus microgrid system. *IEEE Transactions on Power Delivery*, 28(2):779–787, 2013.
- [56] Tanya Paskova, Drew A. Hanser, and Keith R. Evans. Gan substrates for iii-nitride devices. Proceedings of the IEEE, 98(7):1324–1338, 2010.
- [57] X. Pei, O. Cwikowski, D. S. Vilchis-Rodriguez, M. Barnes, A. C. Smith, and R. Shuttleworth. A review of technologies for mvdc circuit breakers. In *IECON 2016 - 42nd* Annual Conference of the *IEEE Industrial Electronics Society*, pages 3799–3805, 2016.
- [58] Chang Peng and Alex Q. Huang. A protection scheme against dc faults vsc based dc systems with bus capacitors. In 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, pages 3423–3428, 2014.
- [59] Bayron Perea-Mena, Jaime A Valencia-Velasquez, Jesús M López-Lezama, Juan B Cano-Quintero, and Nicolás Muñoz-Galeano. Circuit breakers in low-and mediumvoltage dc microgrids for protection against short-circuit electrical faults: Evolution and future challenges. *Applied Sciences*, 12(1):15, 2021.
- [60] P. Prempraneerach, M. G. Angle, J. L. Kirtley, G. E. Karniadakis, and C. Chryssostomidis. Optimization of a z-source dc circuit breaker. In 2013 IEEE Electric Ship Technologies Symposium (ESTS), pages 480–486, 2013.
- [61] Pavel Purgat, Samad Shah, Nils van der Blij, Zian Qin, and Pavol Bauer. Design criteria of solid-state circuit breaker for low-voltage microgrids. *IET Power Electronics*, 14(7), 2021.
- [62] Pavel Purgat, Samad Shah, Nils van der Blij, Zian Qin, and Pavol Bauer. Design criteria of solid-state circuit breaker for low-voltage microgrids. *IET Power Electronics*, 14(7):1284–1299, 2021.
- [63] Wei Qian, Fang Zheng Peng, and Honnyong Cha. Trans-z-source inverters. In The 2010 International Power Electronics Conference - ECCE ASIA -, pages 1874–1881, 2010.
- [64] Simon Ravyts, Giel Van den Broeck, Leonie Hallemans, Mauricio Dalla Vecchia, and Johan Driesen. Fuse-based short-circuit protection of converter controlled low-voltage dc grids. *IEEE Transactions on Power Electronics*, 35(11):11694–11706, 2020.

- [65] Fabrizio Roccaforte, Patrick Fiorenza, Giuseppe 1 error8 warnings Greco, Raffaella Lo Nigro, Filippo Giannazzo, Ferdinando Iucolano, and Mario Saggio. Emerging trends in wide band gap semiconductors (sic and gan) technology for power devices. *Microelectronic Engineering*, 187-188:66–77, 2018.
- [66] Rostan Rodrigues, Yu Du, Antonello Antoniazzi, and Pietro Cairoli. A review of solidstate circuit breakers. *IEEE Transactions on Power Electronics*, 36(1):364–377, 2021.
- [67] Daniel Joseph Ryan, Hugh Duffy Torresan, and Behrooz Bahrani. A bidirectional series z-source circuit breaker. *IEEE Transactions on Power Electronics*, 33(9):7609–7621, 2018.
- [68] D. Salomonsson and A. Sannino. Load modelling for steady-state and transient analysis of low-voltage dc systems. *IET Electric Power Applications*, 1:690–696(6), September 2007.
- [69] Daniel Salomonsson, Lennart Soder, and Ambra Sannino. Protection of low-voltage dc microgrids. *IEEE Transactions on Power Delivery*, 24(3):1045–1053, 2009.
- [70] Yukihiko Sato, Yasunori Tanaka, Akiyoshi Fukui, Mikio Yamasaki, and Hiromichi Ohashi. Sic-sit circuit breakers with controllable interruption voltage for 400-v dc distribution systems. *IEEE Transactions on Power Electronics*, 29(5):2597–2605, 2014.
- [71] Swati Savaliya and Baylon G. Fernandes. Performance evaluation of a modified bidirectional z-source breaker. *IEEE Transactions on Industrial Electronics*, 68:7137–7145, 2020.
- [72] Swati Savaliya, Sumeet Singh, and B. G. Fernandes. Protection of dc system using bi-directional z-source circuit breaker. In *IECON 2016 - 42nd Annual Conference of* the *IEEE Industrial Electronics Society*, pages 4217–4222, 2016.
- [73] Adil Ayub Sheikh, Sarvesh A. Wakode, Rohit R. Deshmukh, Makarand S. Ballal, Hiralal M. Suryawanshi, Mahesh K. Mishra, and Shrawan Kumar. A brief review on dc microgrid protection. In 2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC), pages 1–6, 2020.
- [74] Z. John Shen, Zhenyu Miao, Aref M. Roshandeh, Peter Moens, Herbert Devleeschouwer, Ali Salih, Balaji Padmanabhan, and Woochul Jeon. First experimental demonstration of solid state circuit breaker (sscb) using 650v gan-based monolithic bidirectional switch. In 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), pages 79–82, 2016.
- [75] Z. John Shen, Zhenyu Miao, and Aref Moradkhani Roshandeh. Solid state circuit breakers for dc micrgrids: Current status and future trends. In 2015 IEEE First International Conference on DC Microgrids (ICDCM), pages 228–233, 2015.
- [76] Z. John Shen, Gourab Sabui, Zhenyu Miao, and Zhikang Shuai. Wide-bandgap solidstate circuit breakers for dc power systems: Device and circuit considerations. *IEEE Transactions on Electron Devices*, 62(2):294–300, 2015.

- [77] Sadhana Singh, Tarun Chaudhary, and Gargi Khanna. Recent advancements in wide band semiconductors (sic and gan) technology for future devices. *Silicon*, 2021.
- [78] Weizhang Song, Ning An, and Youyun Wang. A novel bidirectional t-source dc circuit breaker for dc microgrids. In 2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA), pages 1540–1545, 2019.
- [79] Ryszard Strzelecki, Wieslaw Bury, Marek Adamowicz, and Natalia Strzelecka. New alternative passive networks to improve the range output voltage regulation of the pwm inverters. In 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, pages 857–863. IEEE, 2009.
- [80] Hiroshi Sujod, Muhamad Zahim y Sakata. Simulación de conmutación de si-gto, sic-gto y power mosfet. In 2006 IEEE International Power and Energy Conference.
- [81] Leslie Tracy and Praveen Kumar Sekhar. Design and testing of a low voltage solid-state circuit breaker for a dc distribution system. *Energies*, 13(2), 2020.
- [82] Yufeng Wang, Weilin Li, Xuanlyu Wu, Renyou Xie, Zhiyong Zhang, and Heng Wang. A novel solid-state circuit breaker for dc microgrid system. In 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC), pages 1–6, 2018.
- [83] Yufeng Wang, Weilin Li, Xuanlyu Wu, Renyou Xie, Zhiyong Zhang, and Heng Wang. A novel solid-state circuit breaker for dc microgrid system. In 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), pages 1–6. IEEE, 2018.
- [84] Arthur Wright and P Gordon Newbery. *Electric fuses*, volume 49. IET, 2004.
- [85] Xiaorui Xu, Wanjun Chen, Chao Liu, Ruize Sun, Zhaoji Li, and Bo Zhang. An efficient and reliable solid-state circuit breaker based on mixture device. *IEEE Transactions on Power Electronics*, PP:1–1, 03 2021.
- [86] Xiaorui Xu, Wanjun Chen, Hong Tao, Qi Zhou, Zhaoji Li, and Bo Zhang. Design and experimental verification of an efficient sscb based on cs-mct. *IEEE Transactions on Power Electronics*, 35(11):11682–11693, 2020.
- [87] Yachao Yang, Chun Huang, Zhenxing Zhao, Qianming Xu, and Yaqun Jiang. A new bidirectional dc circuit breaker with fault decision-making capability for dc microgrid. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(3):2476–2488, 2021.
- [88] Mohammad Aman Yaqobi, Hidehito Matayoshi, Mir Sayed Shah Danish, Mohammed Elsayed Lotfy, Abdul Motin Howlader, and Senjyu Tomonobu. Low-voltage solid-state dc breaker for fault protection applications in isolated dc microgrid cluster. *Applied Sciences*, 9(4), 2019.

- [89] Fengyan Zhang, Chao Meng, Yun Yang, Chunpeng Sun, Chengcheng Ji, Ying Chen, Wen Wei, Hemei Qiu, and Gang Yang. Advantages and challenges of dc microgrid for commercial building a case study from xiamen university dc microgrid. In 2015 IEEE First International Conference on DC Microgrids (ICDCM), pages 355–358, 2015.
- [90] Liqi Zhang, Kai Tan, Xiaoqing Song, and Alex Q. Huang. Comparative study on the turn-off capability of multiple si and sic power devices. In 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), pages 295–299, 2017.
- [91] Yuanfeng Zhou, Risha Na, Yanjun Feng, and Zheng John Shen. Gan-based tri-mode intelligent solid-state circuit breakers for low-voltage dc power networks. *IEEE Transactions on Power Electronics*, 36(6):6596–6607, 2021.
- [92] Zhongzheng Zhou, Jianguo Jiang, Shu Ye, Cong Liu, and Dan Zhang. A t-source circuit breaker for dc microgrid protection. *IEEE Transactions on Industrial Electronics*, 68(3):2310–2320, 2020.
- [93] Zhongzheng Zhou, Jiayan Jiang, Shu Ye, Dirui Yang, and Jianguo Jiang. Novel bidirectional o-z-source circuit breaker for dc microgrid protection. *IEEE Transactions on Power Electronics*, 36(2):1602–1613, 2021.