Development of a Smart Energy Meter for Power Grids

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Abstract

Smart cities implement information and communication technologies (ICTs), IoTs devices, sustainable projects, among others, to enhance quality of life, proficiency and efficiency. Power grids can incorporate these qualities to a transform into a smart grid. In this context, smart meters play a crucial role by submitting information of the grid in real-time to a management center and helping the utilities to take decisions. In this thesis it is described the development of a smart meter, from the analysis of the requirements, the design of the different systems, components acquisition, the design of the PCB, firmware structure, up the connection to a database. It is a prototype project that proposes to solve problems such as fraud (stealth), grid failures, energy distribution inefficiency, etc. while offering scalability, proficiency and flexibility of use to the utilities. Its application context is the city of Medellín, Antioquia, and is involved in a master project of the Universidad de Antioquia.

Keywords: Smart City, Smart Grid, Smart Meter, Database, ESP32, PCB, Conditioning System, Communication Interface.

I. INTRODUCTION

Utility companies provide services regarding electricity transmission, management and distribution. Basically, they consist traditionally of power lines, electrical stations and consumers. The management is mainly executed manually and the support for faults on the line is detected by reports made by the customers. There is no efficient way to know how properly it is distributed and consumed. Thus, modern approaches are looking for solutions to achieve end-to-end communication between the customers and the utilities. Here, as it is stated in [1], "Smart grid concept promises a reliable and efficient supply of electricity. It recognizes the growing importance of Information and Communication Technologies (ICTs). By incorporating ICT in the existing electrical network, it will transform into the smart or intelligent grid". In this way, smart meters play an important role, not only for measuring, but for delivering quality power. The metering option benefits utility companies by decreasing the required capacity. Also, it benefits customers by providing reduced demand and usage rates during off-peak times, which gives customers a chance to reduce their utility bill. Smart meters are powerful measurement devices that have digital display, capabilities of recording how much power is consumed and when, and transmitting this information automatically to a meter data management system (MDMS) for further processing and storage [3]. This means that automated metering infrastructures (AMIs) are required to assemble all the entities. [2] states "An AMI is minimally made up of smart meters, data concentrators, meter data management system (MDMS), and bidirectional communication networks". Fig. 1 shows an example of an AMI.

In order to provide reliable and protected information, smart meters include a combination of hardware, software, and calibration systems; metrology, security, and communication are the core elements of smart meters. Besides, they might be ways to upgrade their firmware (embedded code) in order to make these devices profitable for future applications. The main

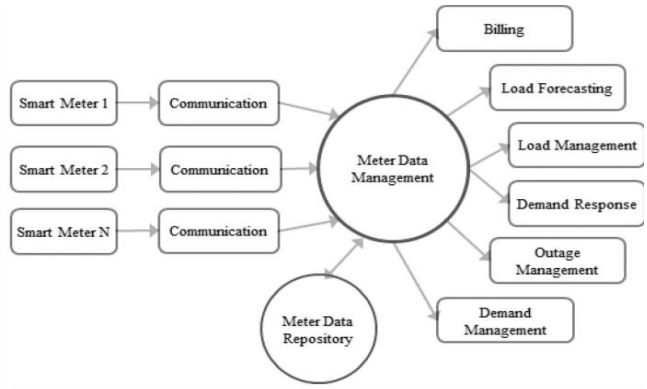

Fig. 1. Example of an automated metering infrastructure, aka, AMI.

energy measurements are RMS current and voltage, active and reactive power, power factor and frequency.

There are some limitations to handle with before setting up the AMI. One of them is the intercommunication speed. 5th generation communication technology is amazingly fast, provides great service in crowd, super real time and reliable connections, though is not possible to find such powerful feature at every city [1]. This is an important consideration to foresee possible update rates and maximum number of simultaneous requests that the AMI could stand. Another limitation to evaluate is the topologies about smart meters and loads. One requires one smart meter per load, which is prohibitively expensive; another, one smart meter for many loads, by applying multiplexing. This is more efficient, but may require faster processing units and more hardware to multiplex; another is to use non-invasive load disaggregation (NILD), which is again one meter for many loads but no multiplexing units. The main idea is to use the measured aggregate load consumption to extract the individual loads consumption. Recent experimental testing conducted by the Electrical Power Research Institute (EPRI) pointed out the lack of accuracy of this technology [2].

Other properties added to the smart grid by implementing smart meters are to reduce losses due to fraud and the possibility to incorporate renewable energies [3].

Now, the purpose of the project is to develop a smart meter with enough resources to operate in different scenarios. The scope of application is within the domestic and industrial environment of Colombia, specifically the city of Medellín-Antioquia, which is right now (2023) facing the 4th industrial revolution: IoT. According to the *Alcaldía de Medellín*, the *Valle de Aburrá* is looking for innovative projects, technologies and civil methodologies that allows them to reach sustainable projects, renewable energies, improvement in transportation, application of IoT devices, open data for the use of people, etc. I.e., it is leading to become smart cities. The city of Medellín is betting for the ICTs to collect data, share it in credible and transparent sources and, hereby, enhance the quality of life [4]. The 4th generation of communication technologies is dominant: 4G/4.5G.

Also, the master project associated to is *Integración y gestión inteligente de las fuentes de energía renovable para propiciar la sostenibilidad energética*, which main goal is to include renewable sources of energy in intelligent/smart ways.

This master project sets the requirements for our project, described in section IV), part 'A'.

This project is a bachelor's degree to obtain the title of electronic engineering at the Universidad de Antioquia, Medellín-Antioquia. The general idea is "develop an analog and digital system capable to sample voltage and current on direct current (DC) or alternate current (AC) signals on monophasic and triphasic 60Hz power lines, measure several energy variables using digital signal processing (DSP) algorithms, have different communication interfaces, such as Bluetooth, WIFI, LORAWAN and Ethernet, and reports to a database the data recorded". With all this, a prototype is created for a very general smart meter. The use of DSP is a powerful feature for companies to keep the product profitable by just changing the algorithms to make new measurement. For this, it is expected to use a processing unit easy to program, otherwise it might be time and cost consuming to reprogram and train new personal. By using DSP, the smart meter is capable to be integrated in any topology, like the NILD type. On the other hand, it is expected to design a general model for DC, monophasic and triphasic system, with the intention to decrease the cost of the final product as much as possible, doing it more accessible to the pocket of clients. The use of different communication technologies let the system to work out in more environments. In any case, the report to a database or a MDMS is indispensable, so an internet connection is mandatory.

Our project does not consider security, firmware updating, fraud or failure report. It is not integrated into any AMI or MDMS, just connected to a database, but all benefits stated are possible to be implemented. The calibration is performed manually. Note that this bachelor's degree does not consider the programming of any DSP algorithm, just a system capable to execute them.

In this thesis the reader will find the different requirements for every stage of development, the analytical procedures, the selected components, the printed circuit board (PCB) considerations, the approach to send to the database, results and analysis. The price of the final product is compared with some commercial domestic and industrial products. The main sample projects studied to design the system were: commercial product "S31 & S31 Lite Wi-Fi Smart Plug US Type" by Sonoff [5] and the "Reference Design to Measure AC Voltage and Current in Protection Relay with Delta-Sigma Chip Diagnostics" by Texas Instruments [6].

II. OBJECTIVES

A. General

Development of analog and digital system capable to sample voltage and current on DC or AC signals on monophasic and triphasic 60Hz power lines. The system must be capable to measure several energy variables using DSP algorithms, have different communication interfaces, such as Bluetooth, WIFI, LORAWAN and Ethernet; It should report to a database the data recorded. The system must be easily reprogrammable and should operate for domestic or industrial environments.

B. Specific:

- Select and purchase of the components
- Develop the analog conditioning system for voltage and current measurement.
- The system should operate in domestic or industrial environments, and for monophasic or triphasic systems.
- Develop the digital system with the following capabilities or interfaces: DSP, WIFI, Bluetooth, LORAWAN, Ethernet.
- Design the PCB of the whole system.
- Write the firmware to control the digital system and send data to the database.
- Choose a data platform to connect to a database.

III. Concepts

A. Analog technical specifications

This project demands to read a lot of Datasheets. The first specification to check at any datasheet are: absolute ratings, recommended ratings, input ranges. **Absolute ratings** are important to be sure how much protection is necessary for our components. Surpassing these ratings means full damage, excessive degradation or malfunction of the components, or something worst. **Recommended rating** are the values at which the component behaves as it is expected to be. **Input ranges** guarantee adequate functionality and are the references of how one component is meant to be connected to other. This means, when choosing the components, they must respect the rating or signal levels, otherwise there might be damages or undesired behavior.

Also, it is notable that **noise** is one of the biggest problems for electronic systems, and designs should/must be though regarding attenuations, corrections or immunity against it. There are some relevant specifications that indicate how much noise or distortion affects a signal when it passes through an **integrated circuit (IC)**, such as: CMRR, PSRR, bandwidth and TDH.

CMRR (common-mode rejection ratio) means how well an IC rejects common-mode signals. It is presented on single-ended and differential inputs. The formula is:

$$V_{CM} = \frac{V_+ + V_-}{2} 10^{-\frac{CMRR}{20}}, \qquad (1)$$

Where V_+ = positive or single-ended input, V_- = Negative input or ground, V_{CM} = common-mode voltage. Sometimes is directly related to single-ended input range specification. This voltage is added to the input as $V_{total} = V_{CM} + V_{input}$.

Similar to CMRR, **PSRR** (power supply rejection ratio) means how well the IC or system rejects noise that is added when the supply sources of the IC changes its magnitude. The supplied component needs to have high PSRR if the voltage regulator, converter or supply source doesn't have good load and/or line regulation. It is calculated with the following formula:

$$PSRR = 20 \log\left(\frac{\Delta V_o}{\Delta V_s}\right) dB, \qquad (2)$$

Where ΔV_s = difference of 2 supply voltages,

ΔV_o = difference at the output for the 2 supply voltages.

If V_{s1} gives an output of V_{o1}, and V_{s2} gives an output of V_{o2}, then:

$$\Delta V_s = V_{s2} - V_{s1}, \qquad (3)$$

$$\Delta V_o = V_{o2} - V_{o1}, \qquad (4)$$

The PSRR is frequency dependable.

Bandwidth and the frequency response play a dirty role, as well. It is known that all system is a filter: it takes a signal and changes its properties. The way the harmonics of signal are affected by a system is called **THD**. On the other hand, the **bandwidth** is the frequency at which the voltage magnitude is reduced -3dB, unless otherwise stated. Attenuation to the signal's spectrum happens if significant frequencies are near or beyond the bandwidth frequency. The **slew-rate** of a systems depends on its bandwidth, so having less bandwidth means that only slower signals can properly pass through.

However, it's not only the components that are noise, but the signals itself could be, introducing noise along its way. This is why **filtering** is important: Rejecting or attenuating noise. Filtering is indispensable to work with ADCs, since this avoids aliasing. In this context it is called "**anti-aliasing**" filtering.

B. Firmware

Firmware is the code embedded into a microcontroller (MCU). Of course, there are many paradigms of programming to write the code. The paradigms of **operative system (OS)** and **object orientated programming (OOP)** are chosen for this project.

FreeRTOS is an open-source and supported OS in many computer architectures. OS allows the programmer to define **tasks** as individual sections of code and the OS is in charge of managing the execution of them. The programmer just needs to set some rules (queues, semaphores, muxes, priorities) to control the execution flow.

OOP is the ability of the code to declare entities or objects as classes. For example, a car could be a **class** and its properties like the wheels, windows, steering wheel, etc. are its **attributes**. Some functionalities such as "take the left", "accelerate", "reduce speed", etc. are called **methods**. This type of programming explicitly shows the relationship between other objects (classes) in a very readable and understandable way, besides produces reusable code. It is chosen for its productivity, unlike **structural programming**, like the **C programming language**, in which the clarity and sense of the code is only defined by the combination and structure of the different flow controls, variables and functions.

C and C++ are the preferred programming languages for programming embedded system. **C++** is and OOP language, so is selected for this project.

Aside from productivity, reuse and readability, efficient coding is important, as well. Efficiency can be performed by hardware or software. E.g., using OS is less efficient since resources are needed to administrate the OS itself. **Direct Memory Access (DMA)** is a hardware-solution that writes and reads to/from memory without the microprocessor intervention, which results in more performance.

Another way to acquire more performance is by using **multiprocessing** or **parallel programming**. Some MCU are embedded with 2 or more processor (cores). In this case, if using OS, it distributes the tasks between the cores depending on their load.

C. PCB process design

The design of the **PCB** is as important as the design of the analog/digital system because of signal integrity. The first step is to have a general idea of what the system is about and how it could be interconnected. After this, it is necessary to look for a **PCB manufacturer**, see its capabilities and decide if they suffice the needs. If the budget is little, the system requirements should be redesign. Next, prior to locating the components, it is good to define the **Design PCB Rules** that will govern the **PCB placement**. They are directly related with the PCB manufacturer capabilities and the signals behavior. For example, working with a low-frequency system is not the same as a high-frequency one. Clearance, differential pairs, impedance profiles, power planes are some relevant rules to have in mind. The **layer stack** should also be created. Components are placed on the **top and bottom layer**, whereas power planes and some special signal could be stacked on the inner layers. **Power and ground planes** are important for signal return. At **low frequency** the return is spread out in a wide pattern, whilst **high frequency** follows the trace path. There are some technics that helps signal integrity, like: isolating sectors, placing component tightly, avoiding cross talking (interference between 2 traces) by increasing their separating distant, sending a bunch of high frequency signals over an internal **signal layer** to guarantee reading times and more. Finally, the files can be delivered to the manufacturer. Additionally, if available and purchased, the **assembly process** places and welds the components on the physical PCB.

D. Data platforms

Data platforms offer services to deploy applications by using the ICTs. Some of them work over private networks or servers and others use the internet. They are an integrated set of technologies that collectively meets an organization's end-to-end data needs. Some examples are: Snap4City, AWS, Firebase. Firebase, in few words, is a database with a lot of APIs to connect to it, which make it very attractive for fast deployment. Snap4city is something bigger, that includes dashboards and IoT agents, and is powered by FIREWARE, a powerful open-source technology for smart solutions. AWS is one of the biggest cloud computing platforms that offers database storage, dashboards, APIs to interconnect, IoT solutions, cloud computing (for machine learning analysis, e.g.), among others. For prototyping, such as our project, Firebase is an excellent option to start up.

IV. METHODOLOGY

A. Requirements:

The master project states the following requirements:

1) Functional properties:

TABLE 1. Functional requirements

Functional Characteristics	Description
Meter Type	DC/Monophasic/triphasic Meter
Measurements	Voltage, current and power DC/AC
Maximum Voltage DC/AC	250V / 240VAC
Maximum Current DC	250A / 50A / 50A
Submitted Information	V, I, power, harmonics
User Interface	Mobile Application connected by Bluetooth
Sample (sampling) Rate	10KHz (for scalability issues)
Report Rate	1 minute (or less; depending on the data platform)
Number of Harmonics	50 minimum
Precision	1%
Voltage sensing method	Voltage Divider
Current sensing method	Non-invasive Reading (Hall effect)
Status indicator	Green Color = Good, Red Color = Something Wrong
Power consumption	To define

2) Non-Functional properties:

2. Non-functional requirements.

Non-Functional Characteristics	Description
Supply	100V-210A source. Solar panels / 120VAC-60Hz power line
Communication	WIFI, Bluetooth, LORAWAN, Ethernet
Data Content (payload)	Voltage, Power, Current, Harmonics
Protection Code	• IP65
Type of Material for Wrapping	• Plastic

The idea is to design a system capable to adapt to the 3 types demanded: DC, Monophasic and Triphasic. I.e., to reduce prices. For the same purpose, it could be optimal to supply the system with AC or DC sources, which does it more versatile.

According to this, the research is the next step to take.

B. Sample Projects = Research

This is a very important stage to learn about some potential designs, problems and suggestion.

The different results found shown that an isolated system is very useful against damage and noise, as long as it is possible to be built. Also, all these systems are distributed like 3 major sub systems: conditioning, processing and reporting. **The conditioning system** is mainly analog and is in charge of reducing the level of current and voltage to proper levels for the measuring devices. Some designs prefer to use ICs to measure, whilst others **analog-to-digital converters (ADCs)**, like the design by Texas Instruments [6]. Using IC could lead to cheap and compact designs, but limits the capabilities of the system, whereas using ADCs offers more flexibility in terms of what measurements to do or not, due to DSP algorithms. This, of course, require more circuitry and complexity, that is translated in money and research time. **The Processing system** is mainly digital and is, like it says, in charge to process any data. Finally, there is a **communication or reporting system**, that is any interface or module that allows to share data to some external entity, like a database, platform or other devices sharing the same protocol and technology of communication.

Between the many results, 2 designs are very tempting: first is a commercial domestic monophasic smart meter "*S31 & S31 Lite Wi-Fi Smart Plug US Type*" by Sonoff, submitted by the advisor of the project, that has WIFI capabilities and reports common energy variables to a database owned by the seller. This device uses an esp8266 and one embedded IC to calculate power, voltage, current and frequency. The IC is the CSE7766. The circuitry is very simple to understand but is not what we request. The design has very close interaction with the power line, that leads to noisy systems and higher probability of damage from transients at the high voltage side. Other drawback is that the measurement fully depends on the IC, widely limiting the range of operation. Even though, one of its components contributed greatly to the final design: The **ESP8266**. By him is decided to use the **ESP32**, a later version and upgraded version, adding one core else, higher clock speed, Bluetooth and WIFI connectivity; The former only has WIFI. So, the ESP8266 is a good option, but thinking in scalability and flexibility is better to find a more powerful option. And, as it can be seen, just by selecting the ESP32 some of the requirements are already checked. It even has TCP/IP drivers for Ethernet devices. The schematic diagram of Sonoff's product can be found at the appendixes.

Now, with this, the processing system is somehow defined, but what about the conditioning system? Well, an ADC is required if scalability and flexibility are desired. So, a design with such device is the second relevant option: a "*Reference Design to Measure AC Voltage and Current in Protection Relay with Delta-Sigma Chip Diagnostics*" by Texas instrument[5]. This design and article are perfect for understanding a conditioning system with metering skills. The structure of our conditioning system is based upon this one. Their system adds redundancy (2 ADC) to provide protection. While one makes the calculations the other is monitoring the power line. This feature is not included in our design due to complexity, money and size of final PCB. The components connections diagram is included at the appendixes.

C. Hardware

With the research done, it's time to establish some extra features or requirements the different stages to come up should

have. The design will have the following stages: Components selection, analog, digital and PCB design, firmware development and database connectivity.

1) Analog system:

The voltage conditioning system is design to implement at least 3 IC: isolated amplifier, gain amplifier and ADC.

The current conditioning system incorporates: gain amplifier and ADC. The current sensor is external.

The system is very soft with the bandwidth and slew-rate requirements, since signals are very-low frequency. Most electronic components found have bandwidths greater than 50 kHz, i.e., very much higher than the frequency where the system operates: up to 10 kHz (see TABLE 1).

To get the demanded precision of 1% on the reading is necessary to reduce the noise and deviation from the expected value of some components (a resistor with a tolerance < 1%, e.g.).

The analog system should work properly in industrial noise, so a high signal-to-noise ratio is requested. It is hard to define a threshold when the voltage level depends on the components acquired, but the idea is to find component with high input voltage and they should compile with the input voltage range the ADC recommends. This means that the design should be done **back to front** and recursively until all requirements are met. The selected ADC (described in V) part a)), accepts differential input voltages up to 3.1V, and single-ended are rail-to-rail (full supply range). Hence, components with single-ended Input Range (Single-Ended or Differential) ≥ 3V are preferable, as long as their differential pair output (if present) is ≤ 3V.

Another way to reduce noise is by isolating sectors of the system. The high-power side, that is where the measurements are sensed, is noisier due to the level of the signals. This noise comes from the induced magnetic fields: the higher the current the stronger the magnetic fields when current changes. This would not be a problem for a DC current with a stable never changing magnitude, but in an AC system the current is always changing. Besides, there exists the probability to present high voltage or current transients (fast peaks) strong enough to damage the entire meter. This is the reason why we sense the current in a non-invasive measure using hall effect. The voltage measurement is done by using a voltage divider, but the reading is past over the low-power side using an isolated operation amplifier.

Also, to reduce induced noise, it is recommended to apply differential pairs. This consideration is made specially for cross-talking on the low-power side. Components with differential input and output are preferable.

Also, the path the signal takes introduces parasite voltages and errors due to lack of quality on the value expected of some components. PSRR, CMRR and tolerance of passive components are factors to consider. Passive components such as resistor, capacitor and inductor specify a tolerance value, which means how accurate their value is. E.g., If a resistor has a commercial value of 100 ohms and a 5% tolerance, it means its real value could oscillate between 95 and 105 ohms. So, a tolerance of < 1% is preferred when a result depends on the precision, like the voltage divider for sensing the voltage. Here, the 1% comes from the requirements of the project.

The CMRR is a parasite input voltage that depends on the magnitude of the input voltages. Suppose a differential pair has voltages V+ = 4V and V- = 1V, ΔV = 3V (recommended differential input voltage for the ADC), using (1) the CMRR is:

$$V_{CM} = \frac{4V + 1V}{2} 10^{-\frac{CMRR}{20}} = 2.5 \cdot 10^{-\frac{CMRR}{20}}, \qquad (5)$$

Here, the parasite V_{CM} depends on the value of the CMRR. The acceptable CMRR value is derived from the resolution of the ADC and the precision demanded.

Let 3V to be equivalent to 240VAC as the ADC input. If the precision demanded by the projects is focused as **"1% precision for 10 VDC measurements"**, then if the real voltage is 10 VDC, the maximum equivalent acceptable value sampled by the ADC is 10.1 VDC, which in the range of the ADC is

$$\mathrm{x} = 3\mathrm{V} \cdot 10.1 \frac{\mathrm{VDC}}{240\ \mathrm{VAC}} = 89.272\ \mathrm{mV}, \qquad (6)$$

For 10 VDC the equivalent value is 88.388 mV.

The difference of these two values is the tolerance to accomplish the 1% precision:

$$\text{Accumulated Tolerance} = (89.272 - 88.388)\mathrm{mV}$$

$$\text{Accumulated Tolerance} = 884\ \mathrm{uV}, \qquad (7)$$

This leads to the next conclusion: if the accumulated noise is bigger than 884uV, then 1% precision is lost.

Consider that the 3 expected ICs of the conditioning voltage system add an equivalent noise. Then,

$$\text{System Tolerance} = \frac{\text{Accumulated Tolerance}}{3} = \mathbf{295\ uV}, \qquad (8)$$

The ADC should have a resolution less than this value to recognize the measurements within the allowed precision. The resolution of and ADC is defined as:

$$LSB = \frac{(Vref - Vmin)}{2^n}, \qquad (9)$$

Where n = number of bits, Vref = is the voltage reference of the ADC and Vmin = minimum value measurable by the ADC.

For n = 16, Vref = 3V and Vmin = 0, LSB = 45.776 uV;

n = 14, LSB = 183uV; n = 12, LSB = 732 mV.

Thus, following the analysis, an ADC with n = 16 or 14 is enough to accomplish the 1% because

$$\mathrm{n} = 16, \mathrm{LSB} = 45.776\ \mathrm{uV} < 295\ \mathrm{uV}, \qquad (10)$$

$$\mathrm{n} = 14, \mathrm{LSB} = 183\ \mathrm{uV} < 295\ \mathrm{uV}, \qquad (11)$$

An ADC with n = 15 would work as well (91.552 uV), but is not common to find this type.

However, ADCs have a specification called linearity, that means how noisy are the conversions. This is an extra consideration when selecting an ADC for an expected precision. For example, let the linearity be ±1LSB, then for n = 14

$$1LSB + 1LSB_{error} = 366\ uV > 295uV, \qquad (12)$$

And for n = 16

$$1LSB + 1LSB_{error} = 91.552\,uV < 295uV, \qquad (13)$$

Where, n = 14 does not suffice the condition to keep a precision of 1%, yet **n = 16 does it**.

The V_{CM} should not be greater that this magnitude either. So,

$$V_{CM} = 2.5 \cdot 10^{-\frac{CMRR}{20}} < 295uV$$

$$\rightarrow \frac{295uV}{2.5} > 10^{-\frac{CMRR}{20}} \rightarrow \log\left(\frac{295uV}{2.5}\right) > -\frac{CMRR}{20}$$

$$\rightarrow \log\left(\frac{2.5}{295uV}\right) \cdot 20 < CMRR$$

$$CMRR > 78.56\,dB, \qquad (14)$$

It is important to consider that the V_{CM} is not the only source of noise, so to have some freedom let's say that the preferable CMRR is

$$CMRR \geq 80\,dB, \qquad (15)$$

For the PSRR, let a supply voltage of 5V to change 10% at some time. Discard the frequency. For the same voltages for a differential pair as in the previous analysis, if a change of maximum 1% is demanded for a 4V signal, then:

$$PSRR = 20 \cdot \log\left(\frac{4.04 - 4}{5.5 - 5}\right) = -22\,dB, \qquad (16)$$

So, a $PSRR < -22\,dB$ is preferable.

Note that some datasheet represents the CMRR and PSRR value as positive or negative.

Another interesting feature is the THD. This specification is not critical for our design since the frequencies to analyze are relatively low. In the component's selection stage, most of the components had THD ≤ 0.5%.

The ADC is required to have simultaneous readings and sampling rate enough to recover at least 50 harmonics. With simultaneous sampling is guaranteed that all measurements will belong to the same time. This is not very critical for our conditions, since the signal's fundamental frequency is 60 Hz, so a little phase shift of microseconds would not make the big difference. In spite of the fact, the issue is scalability, if faster signals are foreseen to be measured for future purposes. Without this condition, an ADC with multiplexing could be enough, are more common and cheaper.

The minimum sampling rate should suffice the Nyquist theorem:

$$F_s \geq 2 * B, \qquad (17)$$

Where Fs = sampling rate and B = bandwidth of the signal.

for 50 harmonics for a signal with fundamental frequency of 60 Hz:

$$B = 50 * 60 = 3000\,Hz, \qquad (18)$$

And adding one more harmonic to be less strict

$$B = 51 * 60 = 3060\,Hz, \qquad (19)$$

And by (17)

$$Fs \geq 6120\,Hz, \qquad (20)$$

So, the minimum sampling rate for the ADC must be 6.12 ksps. Besides, the requirements state the sampling rate should be 10 kHz, for flexibility and scalability purposes. This means that an ADC with at least 10 kHz of sampling rate is expected.

The ADC must include at least 2 channels for the monophasic and DC system, and 6 channels for the triphasic system. Every pair of channels is for 1 voltage and 1 current sampling.

In the other hand, the supplies sources such as LDOs and converters should fulfill some requirements. First, an accuracy of at least ±1% and a current of 800 mA is desired. It should be clear that one thing is the PSRR and other the proper supply for of a component. If the supply goes beyond or below the recommended supply ratings, the component could malfunction even if the PSRR is high (> 70 dB). The 1% for accuracy is very important for the voltage references, like the one the ADC needs. For an LDO it could be a little higher, but was left at this value to guarantee longer lifespan. The 800mA comes from the fact that supply sources hold bigger stress when supplying a current close to their output limit. If the available current is big compared to what is consumed, then the requirements for load and line regulation could be softer. The system that consumes more current is the digital and, based on summing their supply current, it's not even closed to this value. See component list in appendixes for more information about current supply.

Also, With the same idea of extending the lifespan of the supply source, the line and load regulation are expected to be <= 1%, but is not a strict condition.

Being so, a summary of the preferable technical specifications is shown at TABLE 3.

TABLE 3. technical Specification for analog system.

Type	Specification	Condition
Devices	PSRR	>= 22 dB
	CMRR	>= 80
	THD	< 0.5%
	ADC sampling	Simultaneous sampling sampling rate ≥ 6.12ksps (Enough for 50 harmonics), sampling rate ≥ 10 kHz for scalability and flexibility, 2 channels for DC and monophasic, 6 channels for triphasic
	Input range	(Single-Ended or Differential) ≥ 3V
	Cross-talking	Fully Differential
	Tolerance	1%
	Isolation	Isolated conditioning system
Supplies	Line regulation	<= 1%
	Load Regulation	<= 1%
	Supply accuracy	±1%
	Supply Output Current	800

2) Digital system:

For the digital system, the following consideration were taken account:

a. Processing unit: The processing unit should be affordable, have relatively high clock speed, be multicore and peripherals to communicate easily with outer components. This is very much a microcontroller with good processing capabilities and multiparadigm. Some microcontroller can change the default distribution of its GPIO assignment for their peripherals, doing the design of a PCB easier.

b. Communication Interface: The requirements stated 4 interfaces: WIFI, Bluetooth, LORAWAN, Ethernet. The idea is to design a smart meter with several communication interfaces, all-in-one, to be versatile to many application environments. The interfaces should be affordable, easy to use and well documented, so new programmers could change or update the firmware easily. This is productivity and proficiency for the utilities. Also, as a prototype version, it is not suggested to purchase very expensive modules.

The exception to the rule was the LORAWAN module because there was already a module used in other projects at the *Universidad de Antioquia* (where our project belongs to), whence it was selected as well.

c. ADC: Besides the features mentioned before, the ADC should connect to the processing unit somehow. Some ADC are very straight forward: enable the channels and it sends the samples in a predefined (not configurable) way. Other are programmable and they need to be configured according to what is needed. Some are SAR, some delta-signa type. The delta-signa type was preferred for its oversampling rate (OSR) capabilities, that is better for noise suppression, at the cost of less sampling rate, in most cases. Some embeds in filtering and programmable gain amplifiers (PGAs). The idea is to find an ADC easy to configure, delta-sigma type, with embedded filtering. The embedded filtering is very practical because PCB space is saved in exchange by not placing an outer filter. The communication interface must be UART, I2C or SPI.

2) Components Selection:

With the analog analysis ready and the goal of what to search for the digital system, the component selection should not be hard… Well, that what could be said. This process is very tedious and needs a recursive process. Per every component found all the calculations should be done over and over again. The hardest is to find a proper ADC, because is the heart of the system. It's even harder when the budget, lifecycle and stock are important. Most of the components in the design of Texas Instruments [6] are either discontinued or very expensive, whereby there's no way to "copy" the work. Many providers were listed to found the components, but at the end most of the them were bought at Digi-Key Electronics, Headquartered in Thief River Falls, Minnesota, USA and I+D Electronica, a local provider. A full list of the components is included at the appendixes.

The different supply sources must have enough output current for each bunch of components they power. The total sum of all supply currents should be less and not closed to the maximum output current.

Small components such as resistors or capacitors won't have dimensions smaller than the 0805-package size, to be easy to handle and weld on.

3) PCB:

Altium Designer was the software to design the schematic and PCB. It offers functionalities to make very basic design to very complex systems, with checking and automatic features that simplifies the design.

a. Schematics: The schematic is captured as hierarchical. Some parameters are added in the sheets, such as net classes, differential pair nets and special net names.

It happens that not all components or ICs have libraries or are incomplete; a component needs a least 2 things: 1 schematic design and 1 footprint, and a 3D model is optional. So, for those lacking, the process to create them is as follows:

- Create from Scratch:

1. Create the schematic model manually, using the wizards or a combination of both
2. Create the footprint model manually, using the wizards or a combination of both
3. Create the 3D model. For this, any 3D model editor is ok, as long as the extension of the file of the model saved is supported by Altium, like the .step file. When creating the footprint, the wizard can generate the 3D model for some common component packages. Also, Altium designer offer some basic objects to do it.

- Create component using existing models:

The procedure used is:

1. Use Altium library loader (download and install if needed) to find the model (if available). Save the Altium Schematic Library (.SchLib) in another folder. Use "Library Importer" (from File menu) and upload the model saved. Assign a category and save despite of the warning. The component has been added. Now, look for the component and edit it. The component editor panel opens. Change the name to the exact component name found at any distributor or manufacturer. Select the desired component from the drop-down list. Next, select the parameter to add to the component and then press ok. Save the component.
2. Clone one component that matches the schematic, footprint and 3D model of the new component. Remove the parameter and part choices options. In the name enter the name of the new component and select one option from the drop-down list. The parameters and part choices are uploaded. If the component does not appear in the search engine try using another component name of the same family or reference, and change any attribute as needed.
3. Use a combination of 1) and 2) to create, modify or enhance.

b. PCB: **PCBCart** was chosen to be the manufacturer. Its PCB capabilities for basic (cheaper) designs are within the characteristics of the final PCB of the system.

Most capacitors were placed near their respective supply pin. This are bulk or coupling capacitor.

Power planes were used to help the signal return, supply stability and to avoid interference. For the monophasic/DC design, only 2 layers were stacked. Most of the surface of both layers is used as a plane. The top layer is mainly trace for signals and power plane, and the bottom layer is mainly ground. For the triphasic design, due to its complexity and signals (traces) distribution, 4 layers were stacked. Outer layers are for tracing and placement.t The top layer is specially used for tracing, the inner layer closer to this one is a ground plane, and the left layer is the power plane. Putting the ground layer close to the main tracing layer helps more efficiently for signal return.

The differential pairs were traced together with a minimum clearance of 0.2mm, while keeping a clearance of at least 1mm from different differential pairs, to avoid cross-talking.

D. Software

1) *MCU:* The ESP32 is an excellent option for this project. A detailed exposition of some features is shown at Fig. 9. It is supported by the Arduino IDE or the Espressif IDF (officially supported by the Developers), is well-documented and very popular.

2) *Data Platform:* To make things easy, the first version of this project would connect to any database just to be sure all requirements are accomplished. A second version could be a data platform with advanced graphic properties, like dashboards and real-time updating. Snap4City is a valid option for this. Firebase also offers some dashboards.

The selected data platform was Firebase. Firebase is managed by Google and allows fast deployment of prototyping application. It could be used for more than prototyping with a paid plan. It has 2 popular databases: Firestore Database and Real-time Database. The former is a free plan based on how many operations are made daily. For writing and deleting 20 thousand and for reading 50 thousand are no cost. Besides, each item of data has a maximum size of 1MB. The total size of the database can't be larger than 1GB and the maximum bandwidth of 10GB (total amount of data moved through the cloud). The latter is a cloud-hosted database. Data is stored as JSON and synchronized in real-time to every connected client. The no cost plan is 1GB stored, 10GB download and 100 maximum simultaneous connections. Between this two, Firestore was chosen. Firestore is an enhanced version of Real-time Database. The SDKs (APIs) are enhanced, the display of information is better and the queries could be more complex.

V. DESIGN

A. Hardware

1) Analog system:

a. Voltage: The voltage conditioning system was design with 4 main sectors: voltage divider, Isolated fully differential operational amplifier (OP AMP), fully differential PGA and ADC. The block diagram is shown at Fig. 4.

Note the differential pair along the whole path.

- Voltage Divider

The voltage divider is a set of resistors with a precision of 0.1%.

$$R1 = 1\ M\ ohms, \qquad R2 = \ 10.2\ k\ ohms, \qquad (11)$$

- Isolated Fully Differential Op Amp.

The isolated fully differential op amp is the **AMC1350DWVR**. Some of its features are shown at TABLE 4:

Thanks to its input impedance is possible to connect the voltage divider directly. For lower values, an operational amplifier configured as follower might be mandatory.

The specification "Operating common-mode input voltage" means that both inputs shouldn't have magnitudes greater that 4V simultaneously; The sum of both inputs divided by 2 should outcome at most 4V, if normal behavior is expected.

This IC has high input voltage and high common-mode input voltage, which gives a lot of freedom to play with the input signal magnitudes. One of the most important features is that it is fully differential. In fact, was the only one with such property and high voltage. Others can manage differential pair signals but with voltages up to 250mV, specially designed for measuring current on motor. Reducing the input voltage to such a level means that SNR will be smaller, thus the noise will be a harder problem to deal with.

A typical implementation is shown on Fig. 2:

b. Current: The current sensor is an effect hall sensor **L37S300S05M**. Some of its specifications are shown at TABLE 5.

The linear error ± 0.5% is within the required precision of 1%.

The Sensed current is recovered by using the output voltage and the voltage reference.

The Bandwidth is much greater that the bandwidth of the signal to sample 50 harmonics (> 6120 Hz).

This device and the ADC are the most expensive ones. This current sensor fulfills of the requirements. The only drawback is that the voltage measurement span is a little low: 0.625 V when I = 300A. for I = 250A (maximum current given the requirements), V = 0.52 V. However, the path of the current conditioning system is shorter and has fewer intermediate components, meaning less noise is added.

It is good that the sensor can endure higher currents that the maximum current demanded for the system, i.e., in the situation of power transients the sensor wouldn't be damage.

c. Fully Differential PGA: The selected PGA is the MAX9939. It is a general-purpose, differential-input programmable-gain amplifier. The communication interface is SPI. Among the many suitable PGAs, this one was the only one affordable and with differential input-output. The Drawback is that the first incremental gain is 10V/V, whence the signal can only be amplified when is already at a very low magnitude. If the system is design to withstand 240VAC signals, then the first

incremental gain can only be applied when the voltages go below 240VAC / 10 = 24 VAC ≡ 33.941 VDC. For these low voltages is that the 1% precision was evaluated to measure 10VDC.

TABLE 4. AMC1350 Technical Specification

AMC1350DWVR	
Specification	**Description**
Input voltage Range	Rail-to-Rail ±5V
Input Impedance	1.25 MHz
Gain High-to-Low side	0.4V
High-side power-supply	[3, 5.5] V, typical = 5V
Low-side power-supply	[3, 5.5] V, typical = 3.3V
Specified linear full-scale voltage (VIN = VINP – VINN)	[-5, 5] V
Operating common-mode input voltage	[-4, 4] V
Maximum-rated isolation working voltage	1.5 KVAC 2.12 VDC
CMRR	-72 dB
PSRR	PSRR vs VDD1, DC →-67 dB PSRR vs VDD1, DC →-80dB
THD	-87 dB
Biased output voltage	VCC/2

TABLE 5. L37S300S05M technical specifications

L37S300S05M	
Specification	**Description**
Insulation Voltage	3.3kV
Insulation Withstand Voltage	6 kV
Insulation Resistance	1 M Ohms at DC 500V
Primary nominal current	[-300, 300] A
Primary Maximum Current	±900 A
Supply Voltage (VCC)	[4.75, 5.25] V
Output Voltage	Vref + 0.625 V ± 0.015 V, at 300A
Reference Voltage (output) (Vref)	[2.475, 2.515] V
Linear error (nominal current)	± 0.5%
Frequency bandwidth	50 kHz

This component can deal with negative voltage signals, when powered just by a positive supply. This is not our case, but this is very useful in every way: money, space, precision, by discarding a negative voltage supply.

Because this was the only and best option, regarding the preferable features stated at section IV) part c), the design was compromised with this PGA.

Some of its specifications are included at TABLE 6.

TABLE 6. MAX9939 technical specifications

MAX9939	
Specification	**Description**
Supply voltage	[2.9, 5.5] V
Input Common-Mode Range	[-Vcc/2, Vcc – 2.2V]
Gains	[0.2, 1, 10, 20, 30, 40, 60, 80, 119, and 157] V
Communication interface	SPI
CMRR	-60 dB
THD	89 dB
Gain Error	Typ: 0.05%, Max: 0.38%
Output voltage range	Rail-to-Rail
Biased output voltage	VCC/2

d. ADC: The winner to become the ADC is: the ADS1778 (8 channels) for the triphasic system and the ADS1174 (4 channels) for the monophasic/DC system. This family of ADCs is very powerful and fulfill all the requirements. It just needed to be energized and to enable some channels to start sending data. There is no need to do extra configurations. The sampling rate is based on the clock speed and the digital state of some pins. It is embedded with an excellent digital filter, which its passband (0.1dB) covers up the signal bandwidth (FS/2) and the stop band (100dB) appears just right after, as long as sampling rate is FS = 2B. The sampling rate is up 52ksps and is a delta-sigma ADC.

The trade-off is that in order to be easily configurable, more GPIOs of the microcontroller should be expended. However, even some complex ADC that are command-programable (through the communication interface) expend some GPIO for extra configuration, so at the end the difference is not significant.

One drawback is that requires many external supplies to operate and the distribution of the pins seems to be not the best.

Some technical specifications are shown at TABLE 7.

Note the high CMRR. This helps to complement the low CMRRs of the other components.

Fig. 3 shows a block diagram of the ADC.

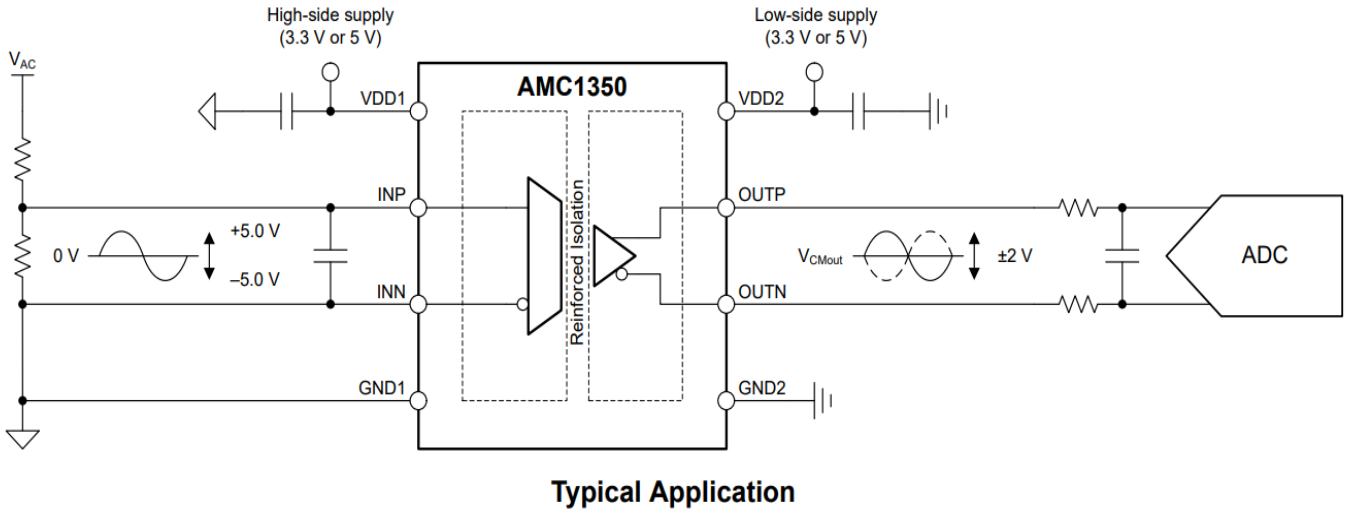

Fig. 2. Typical Application of AMC1350

TABLE 7. ADS1178/ADS1174 technical specifications

ADS1178/ADS1174	
Specifications	**Description**
Sampling rate	Up to 52ksps
THD	-105dB
SNR	97 dB
CMRR	100dB
Stop Band Attenuation	100dB
Interface	SPI
Linearity	1 LSB
Resolution	16 Bits
Analog supply	5V
I/O Supply	1.8V to 3.3V
Digital Core Supply	1.8V
Type	delta-sigma
Channels	4: ADS1174, 8: ADS1178
Voltage Reference (Vref)	[0.5, 3.1] V
Differential input Voltage	[-Vref, Vref]
Absolute input voltage	Rail-to-Rail
Common-mode input voltage	2.5V

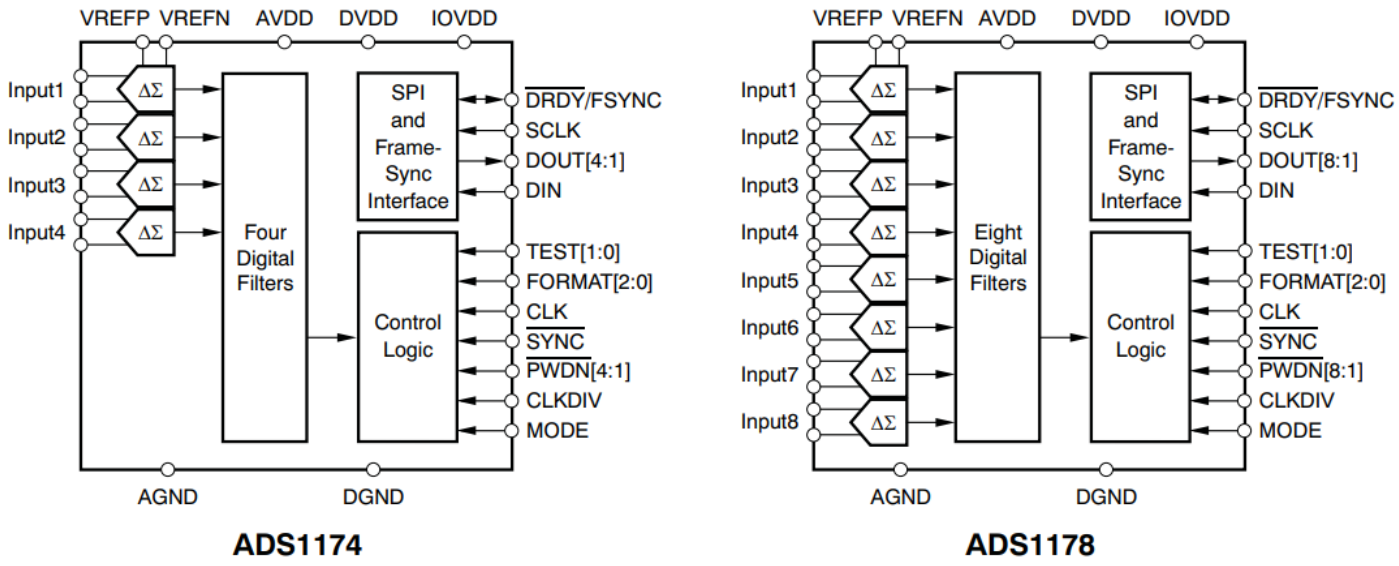

Fig. 3. ADS1178/ADS1174 block diagram.

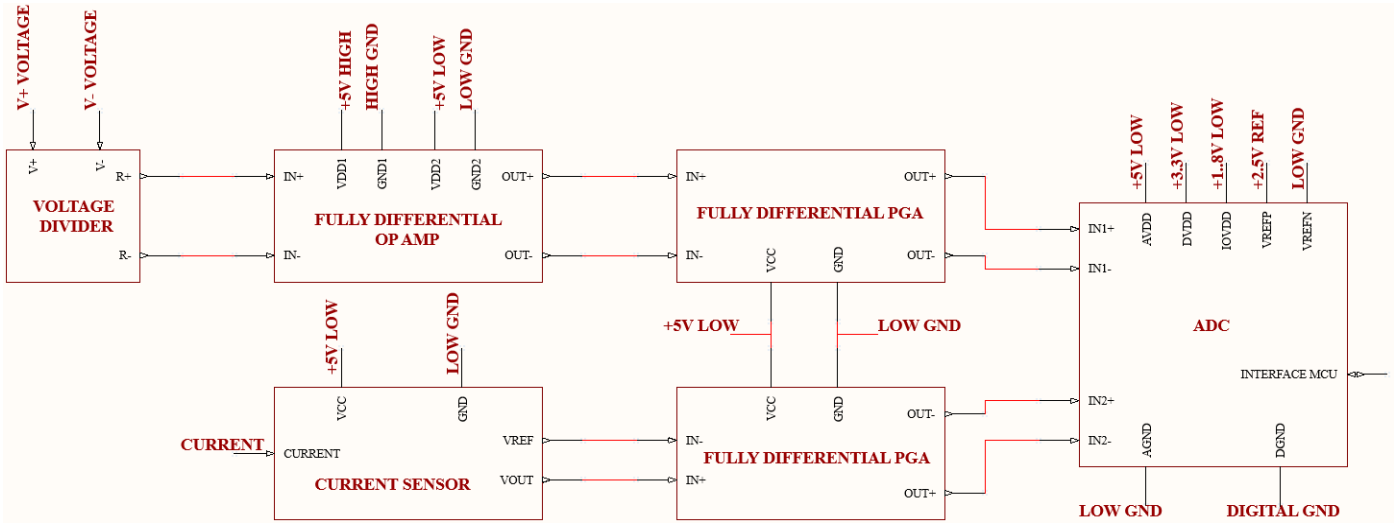

Fig. 4. Block diagram of the analog system

e. Analytical process: The block diagram of the system is displayed at Fig. 4:

1. Voltage: The system should be evaluated with the extreme values. In this case, 240VAC (339.411 Vrms) is the maximum voltage the system resists.

For the set of resistors, let the inputs be V+ = 240VAC, V- = 0V.

The voltage at the divider is

$$R_+ = 240VAC \cdot \frac{R2}{R1 + R2}, \qquad (21)$$

Then, by substituting (11)

$$R_+ = 240\ [VAC] \cdot \frac{10.2\ k\ [ohms]}{(1\ M + \ 10.2\ k)[ohms]}$$
$$= 339.411\ [V] \cdot \frac{51}{5051} = 3.427\ V, \qquad (22)$$

The AMC1350 gain is 0.4, and the output voltage is biased VCC/2. whereby, if VIN+ = 3.427 V, VIN- = 0V

$$VOUT_+ \ = \ 3.1854\ V = 2.5\ V + \ 0.6854V = 2.5V + 0.2 \cdot 3.427$$

$$VOUT\_ \ = \ 1.8146\ V = 2.5\ V - 0.2 \cdot 3.427\ V$$

$$\Delta VOUT = 1.3708\ V = \ 0.4 \cdot \ 3.427\ V, \qquad (23)$$

From this point, the signal is differential.

Now, the input voltage to the PGA is:

$$\Delta VIN = 1.3708\ V$$

And due to the PGA has a biased output voltage equal to VCC/2, for a gain = 1 V/V

$$VOUT_+ = 3.8708\,V = 2.5\,V + 1.3708\,V$$

$$VOUT_- = 1.1292\,V = 2.5\,V - 1.3708\,V$$

$$\Delta VOUT = 2.7416\,V, \qquad (24)$$

Next, the ADC has a differential input voltage of [-Vref, Vref]. The Voltage reference was set to 3V, so

$$|\Delta VIN| \leq 3V, \qquad (25)$$

The current input to the system is

$$\Delta VIN = 2.7416\,V, \qquad (26)$$

That is within the limits. It is suggested to conserve a span from the limit, because noise and parasite signal voltage is added along the signal path.

Here, it is checked that the analog conditioning system works properly under the recommended technical specifications of every component.

2. Current: The current sensor has a nominal current of 300A, at which

$$Vout \approx 2.5 + 0.625, \qquad (27)$$

However, the maximum current held by the system is 250A.

The equivalent voltage magnitude for this current is:

$$V_{250A} = 2.5 + 250\,A \cdot \frac{0.625\,V}{300\,A} = 2.5 + 0.52 = 3.02$$

And

$$V_{-250A} = 2.5 - 250\,A \cdot \frac{0.625\,V}{300\,A} = 2.5 - 0.52 = 1.98\,V$$

Also, let the Vref of the Current sensor to be 2.5V

Then,

$$\Delta Vout = 0.52\,V, \qquad (28)$$

For the PGA input,

$$\Delta VIN = 0.52\,V$$

its output

$$VOUT_+ = 3.02\,V = 2.5\,V + 0.52\,V$$

$$VOUT_- = 1.98\,V = 2.5\,V - 0.52\,V$$

$$\Delta VOUT = 1.04\,V, \qquad (29)$$

So, the ADC input is

$$\Delta VIN = 1.04\,V, \qquad (30)$$

and, this again, it's within the input range of the ADC.

Note that the there is significant difference between the input voltage coming from each system. Also, the voltage can have a maximum amplitude and the current a minimum at the same time, which would be problematic if both PGAs of both systems have the same gain configuration. To solve this problem, each system has its own gain. Although, if one current PGA has a gain of 10V/V then all the others current PGAs will have it as well, but the voltage PGAs can be configured with a gain of 1V/V or any other available gain. If one current/voltage is low on one phase and in another one is high, the PGA is configured according to the larger one.

A summary of the previous analysis is indicated on TABLE 8:

f. Supplies: All the supplies of the system satisfied the preferable features. They can be found in the list of components in the appendixes.

The LS10-13B09R3 is the main supply source of the system. It's an AC-DC or DC-DC converter, which allows the system to be powered by AC or DC sources, that is a requirement of the project. It's a 9VDC-1.1A supply source, 85 ~ 305 VAC, 100 ~ 430 VDC Input.

The 1S4AE_0505S3UP is the isolated DC-DC converter that provides the power on the high-power side. It has Output of 5V 200mA, 4.5V - 5.5V Input. The accuracy is 1% for a current supply less than 100mA at the high-power side, for the triphasic system. This converter is powered by an LDO of 5V.

The list of components in the appendixes includes a column that specifies the current supply of each component.

2) Digital system

The selected digital components and its main features are shown at TABLE 9:

It was already stated that the ESP32 was selected as the processing unit. It really simplifies the development of IoT applications due to its SDK and embedded modules. The 2 cores are for multiparadigm programming and with a frequency clock up to 240MHz it's possible to implement DSP, compared to other MCUs that run on speed up to 80MHz or less. Two communication interfaces are embedded, whence simplifying the PCB design and the reducing the cost of the system. Also, the PCB design is easier by using the GPIO matrix property with which is possible to reassign the peripherals inputs/outputs to most GPIOs. Besides, many projects might find better to use the Arduino IDE (a widely popular and supported IDE) than the Espressif IDF that gives more control over low-level features, which is supported by the developer of the MCU. Anyway, both options are available and both are good.

The embedded Bluetooth module is configured as a serial interface. Very much like a wireless UART: commands are received and decoded. However, it is possible to make much more complicated configurations, like a Bluetooth server. The Espressif idf includes example about how to configure it in many ways. The example to configure it as a serial is "Bluetooth\bt_spp_acceptor".

TABLE 8. Summary of the analytic process of the signal path.

Type	Recommended Input Voltage	Actual Input Voltage	Output Voltage
Voltage:			
Voltage Divider	240VAC Max	240VAC Max	3.427 VAC SE
Isolated Amplifier	[-5, 5] V single-ended	3.427 VAC SE	1.3708 VAC DV → 0.6854 VAC SE
PGA	[-2.5, 2.8V] single-ended	1.3708 VAC DV → 0.6854 VAC SE	With Gain = 1: 2.7416 VAC DV → 2.5 ± 1.3708 VDC SE
Current:			
Current Sensor	[-300, 300] A	[-250, 250] A	2.5 ± 0.52 VDC SE 2.5V ≡ 0A; 3.02 V ≡ 250A
PGA	[-2.5, 2.8V] single-ended	[2.24, 2.76] VCM	With Gain 1: 2.5 ± 0.52 VDC SE on DP → 1.04 VAC DV
Any:			
ADC	[-2.8, 2.8] V DV Rail-To-Rail SE upon analog supply	Voltage: 2.7416 VAC DV → 2.5 ± 1.3708 VDC SE Current: 1.04 VAC DV →2.5 ± 0.52 VDC SE on DP	Digital Stream

*SE = single ended, DV = Differential Voltage, VCM = Voltage Common Mode, DP = Differential Pair

TABLE 9. Digital components

ESP32-Wroom-32D	LORAWAN: E78-915LN22S	Ethernet Interface: ENC28J60
2 Cores	**Already used at the master project**	**Cheap and Popular**
Up to 240 MHz system clock	**Price – Quality**	**Supported on many IDEs**
RF Modules: RF, Bluetooth, WIFI HTTP, TCP/IP, MQTT Support	**Easy to Use: AT Commands**	**SPI interface**
PCB antenna	**UART Interface**	
GPIO Matrix		
Well Documented		
Arduino IDE or Espressif IDF		

The WIFI module is not implement because is not possible to use both WIFI or Bluetooth simultaneously, as a consequence of having only 1 RF module of 2.4GHz. Nonetheless, this issue is solved with the Ethernet module. Whatever done on WIFI can be done on Ethernet. In fact, they are only communication technologies (physical layers) to reach internet. The entity in charge of connecting to the internet is the protocol used: HTTP, TCP, MQTT, etc. Now, if WIFI is request to be implemented, it can replace all functionalities of the Bluetooth and Ethernet Modules. It was just stated its similarity with Ethernet, and Bluetooth can be replaced by implementing a server and Webpage. The Webpage will interact with the user as if it were the mobile application. Hereby, if WIFI or Ethernet is selected it depends on the available technology to connect to.

Finally, the use of the LORAWAN module is very straightforward by sending AT commands with the payload. The data is sent to the data platform *The Things Network* to visualize the content. The only extra element is any LORAWAN gateway to connect to internet.

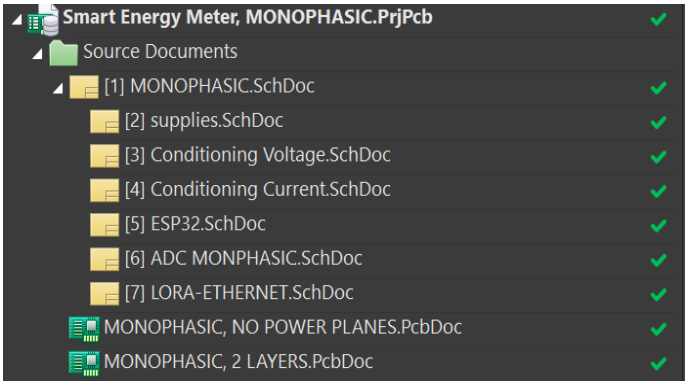

Fig. 4. Project Hierarchy of the monophasic system

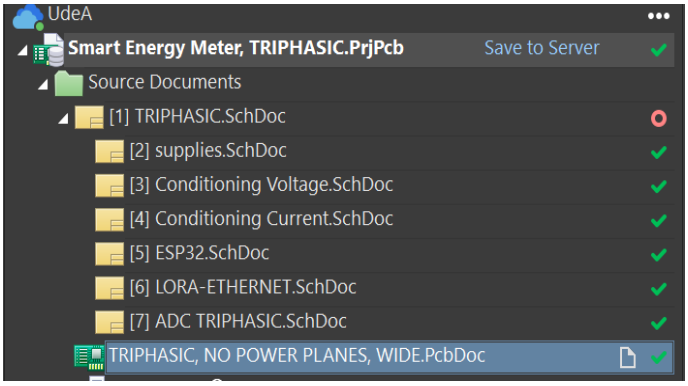

Fig. 5. Project Hierarchy of the triphasic system

B. PCB:

1) Schematics:

a) Hierarchy: The hierarchy of the project is shown at figures 4 and 5:

The schematic of each system hierarchy is displayed at the results section, Figures 11 and 12.

Note that no DC system was design because it is the same as the monophasic. Also, the triphasic system has the same hierarchy, except for the ADC and the ESP32 GPIO pin assignment. This leads to a reusable design for reducing production costs.

b) Parameter: The full set of parameters of the system are shown at TABLE 10. They are specials nets, differential pairs or net classes.

Here, it is remarkable to speak about the PWR, SOURCE, INTERACE and ADC_DIFF net classes. The PWR and SOURCE net classes transmits the whole power throughout the whole PCB. Their traces should be thicker, so they do not heat excessively. INTERACE net class contains fast digital signals (some in the order of MHz), hence they are traced with a clearance of 0.75mm, to avoid cross talking. The ADC_DIFF net class contain the differential pairs connected to the ADC, which should be traced with a narrow clearance in the pair itself to enhance noise immunity, but separated (a larger clearance than at least 4 times the trace width) from other differentials pairs.

No impedance profile is added.

c. Design of libraries: Most of the components included the necessary libraries: schematic, footprint and 3D model. For those that did not include schematic or footprint, these were made manually or with the help of the wizard. For the 3D models that were lacking and not found by neither "Altium library loader" nor the footprint wizard, OpenSCAD was employed with the aim of FreeCAD to convert the files to .step file extension. The specific component within this category were: ESP32, E78-915LN22S (LORAWAN module), ENC28J60 (Ethernet module) and the LS10-13B09R3 (Main System power source).

2) PCB:

a) *Layout and layer stack:* 2 layers are stacked for the monophasic system. 4 for the triphasic. Most of the top layer of the monophasic PCB is power, Fig. 6, and most of the bottom is ground, Fig. 7. The triphasic PCB has its own layer for power and ground; Fig. 8 and 9 shows their layout. Note that several supply voltages and grounds are distributed, in accordance with the function of the area: digital, analog, high power, main power source.

b) Purchase: Ones the PCB is ready is time to send the required file to the manufacturer. The manufacturer PCBCart asked for the Gerber and Drill files, which are the most common. But, have in mind, there are other formats.

No assembly process was purchased.

For full detail of the system schematics can be found at the appendixes. Additionally, the whole project can be found at: https://github.com/Juan13x/Smart_Meter_PCB_UdeA_Bachelor

C. Software:

The software was written with the C++ programming language and OOP. The MCU has DMA capabilities and OS support with FreeRTOS, so these were exploited.

TABLE 10. Parameters (nets) for the PDB design

Nets	Description
ADC	ADC pins
ADC_DIFF	ADC differential Pairs
CURR	Current Sensor pins
DIFF_PGA	Differential Pairs of the PGAs
ETHERNET	Ethernet pins
HIGH_POWER	Power and Ground high-power side
INTERFACE	Interface nets (SPI, UART, clocks)
net_2mm	Some nets to be 2mm width
PGAC	PGA current pins
PGAV	PGA voltage pins
SOURCE	Nets to power the Main supply source
PWR	Nets that transmit the power (5V, 3.3V, etc)
LOW_POWER	Power and Ground low-power side

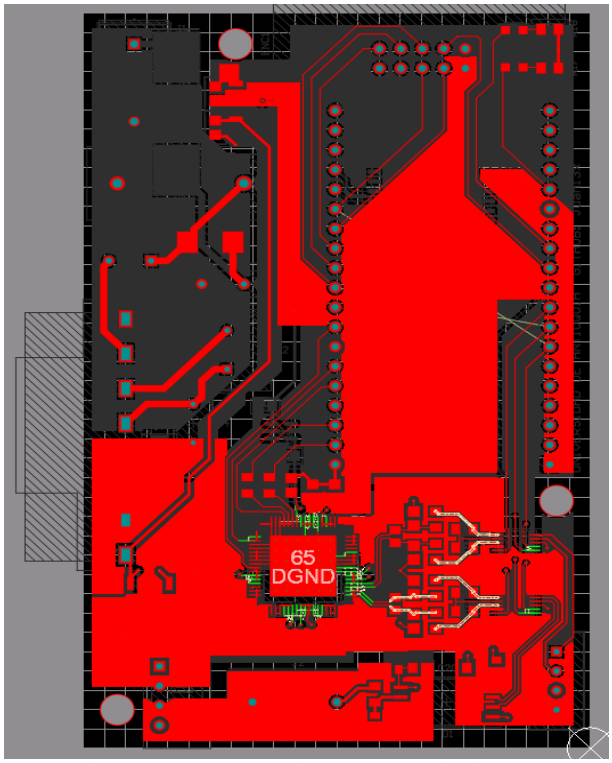

Fig. 6. Top Layer, Ground Layout, Monophasic PCB

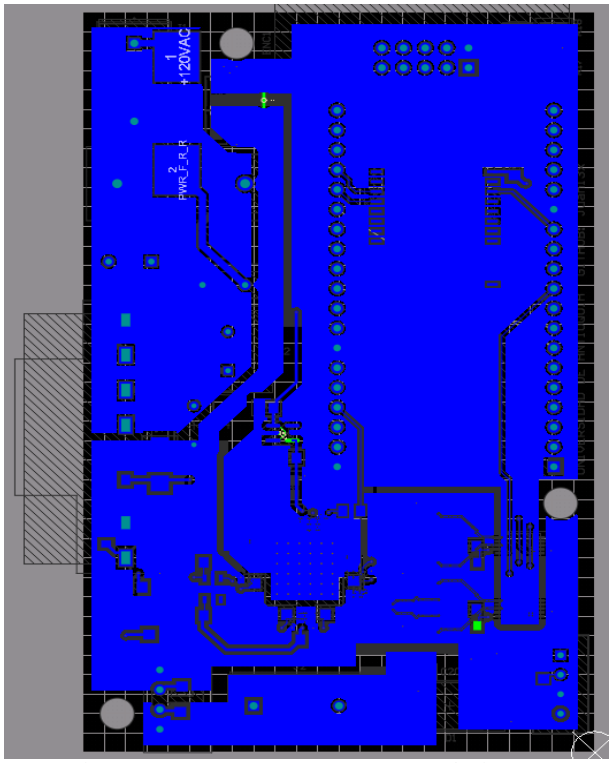

Fig. 7. Bottom Layer, Power Layout, Monophasic PCB

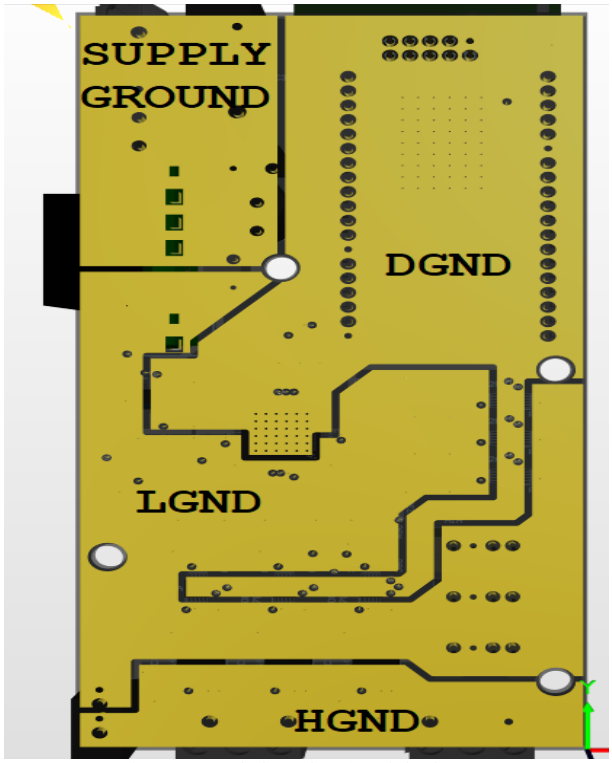

Fig. 8. Ground plane (layer), Triphasic PCB

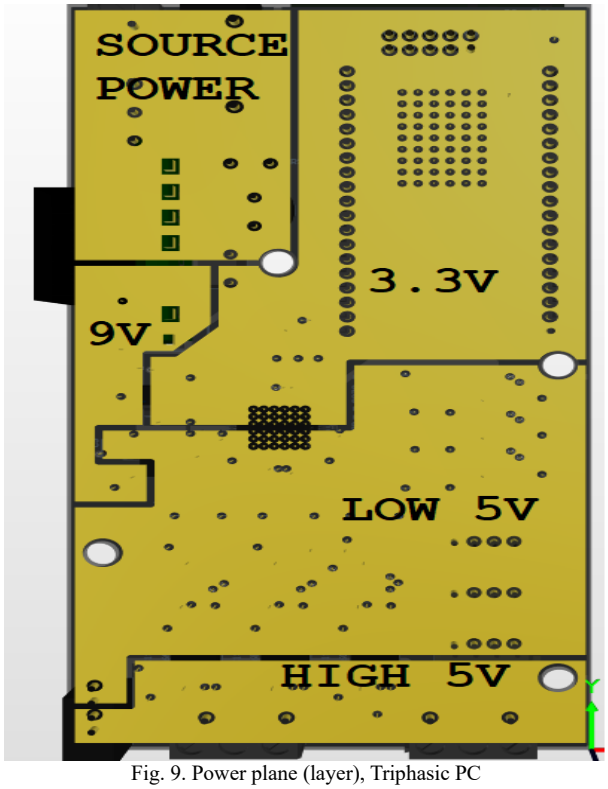

Fig. 9. Power plane (layer), Triphasic PC

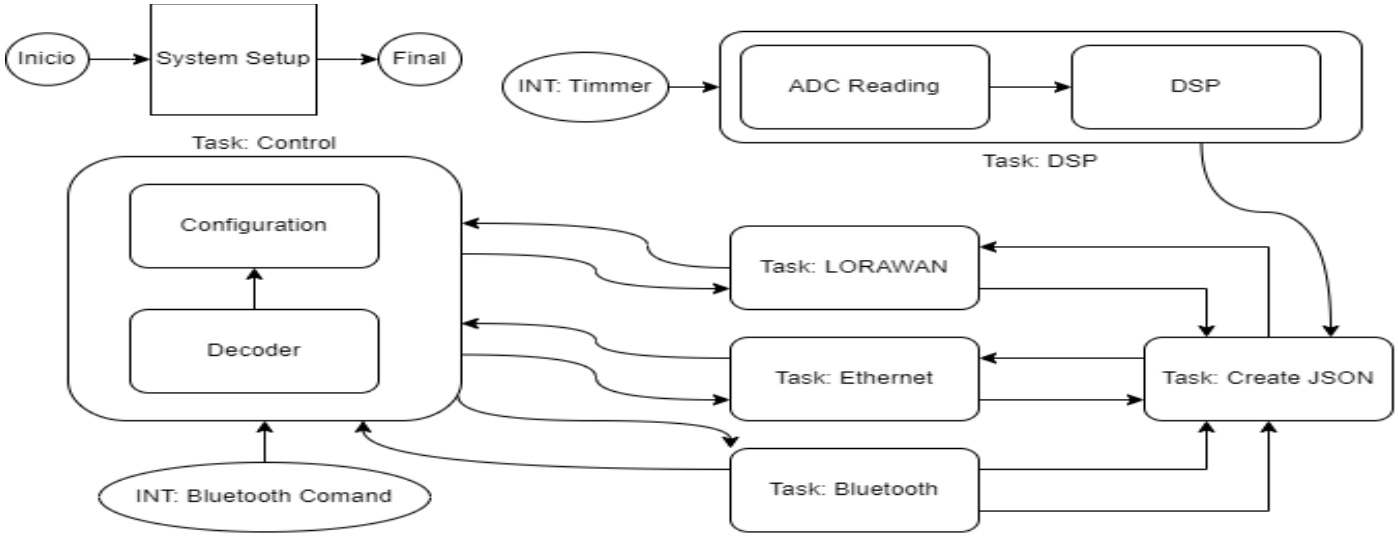

Fig. 10. Firmware's flow diagram

The full code can be found at: https://github.com/Juan13x/Smart_Meter_Firmware_UdeA_Bachelor

1) Flow Diagram:

Fig. 10 represents the task diagram.

Basically, the system starts by configurating timers, tasks, creation of variable, initializing the interfaces. Then, every time a timer interrupts the "DSP" task, this does a "reading" (takes multiple samples) of the power line and its process at the "DSP method". The task "create JSON" is called After some readings have been finished and there's enough information to form a significant package (up to 8 reading). Afterwards, each communication interface (tasks: "LORAWAN", "Ethernet", "Bluetooth") sends the data if it's configured to do it. Only new packages are sent over the interface if it is available when they are ready; if not, they are discarded or delivered to any available interface. This is adequate for slow connection, no connectivity or any problem while transmitting the data, specially over Internet, thus, waiting for only one interface to be available again would create a bottleneck. In the other hand, the task "control" is executed when a Bluetooth command is received. Remember that the user interface was stated to be over Bluetooth connection. Here, the command is decoded and afterwards the configuration process is run. Any configuration regarding the communication interfaces is carried out only when these are Idle.

2) Database:

The connection to the database is done by using the REST API. Data has no encryption.

Each entry in the database is call a collection. Each collection has documents and this one has pairs of key-values. Each document has a size of maximum 1MB.

The format to represent the data is as follows:

1) <DeviceID> -> JSON -> _<YEAR><day>_<timeMiliseconds>: <data or payload>
2) <DeviceID> -> JSON -> _<counter>: <data or payload>

Where:

- <DeviceID> is the name given to the device and it's a collection
- -JSON is the name for the document. For the final version of the project this may change.
- -_<YEAR><day>_<timeMiliseconds> key that defines the first option.
- -_<counter>: key that defines the second option.
- -<data or payload> is the data to be saved. This is a string variable in JSON format. It holds the information for all the variables sent. If an application reads such data, it can extract or read the data in a JSON format.

It is important to respect the limits of the database, so, by now, each document will save a register of some previous measurements of the smart meter. There are 2 possibilities to work this out: one (option 1) is to create a new document when a new day comes out and keeps the old one while its measurements are still valid after some time, then delete it. The second one (option 2) is not to use a timespan as key, but a counter. The timespan would be part of the payload and each time the counter reaches a limit it resets, overwriting data. By the time this thesis was written, option 1 is the one being used.

VI. RESULTS

A. Schematics

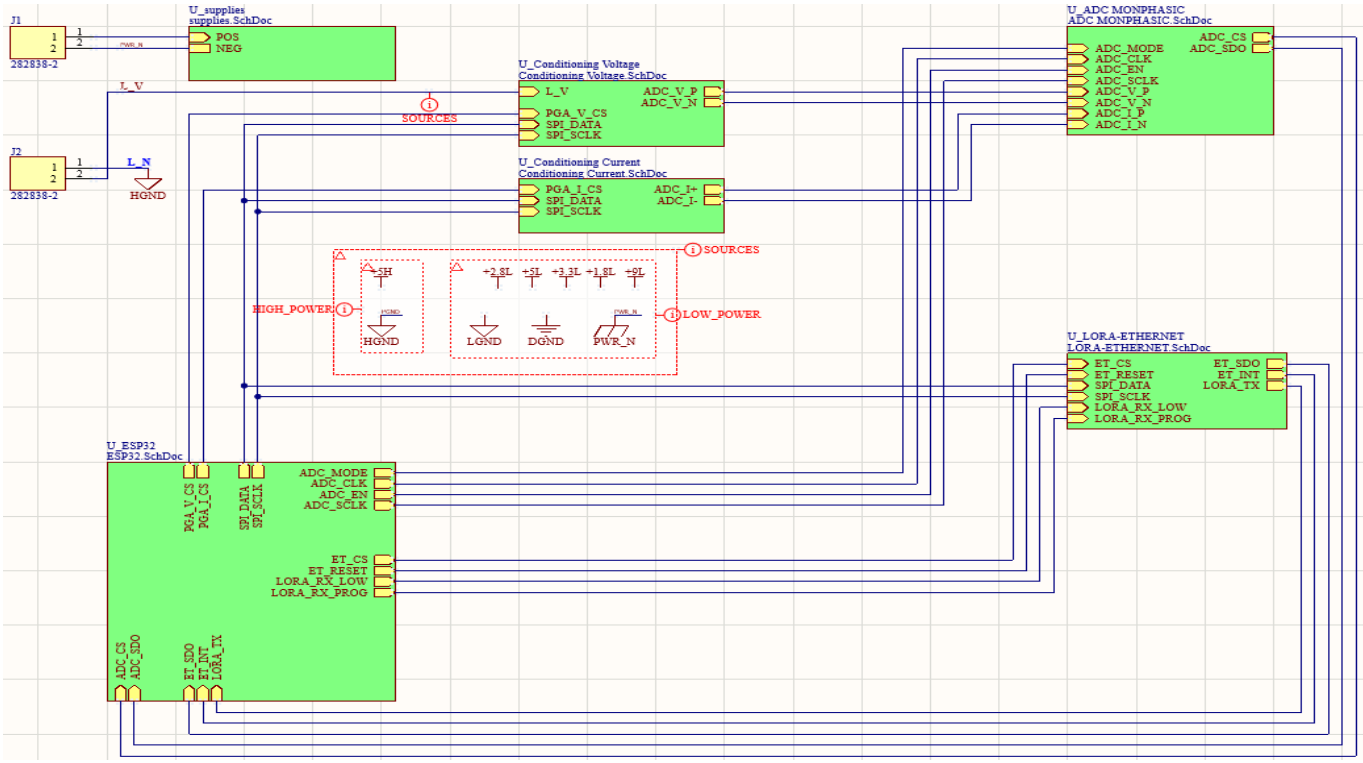

Fig. 11. Schematic of monophasic system

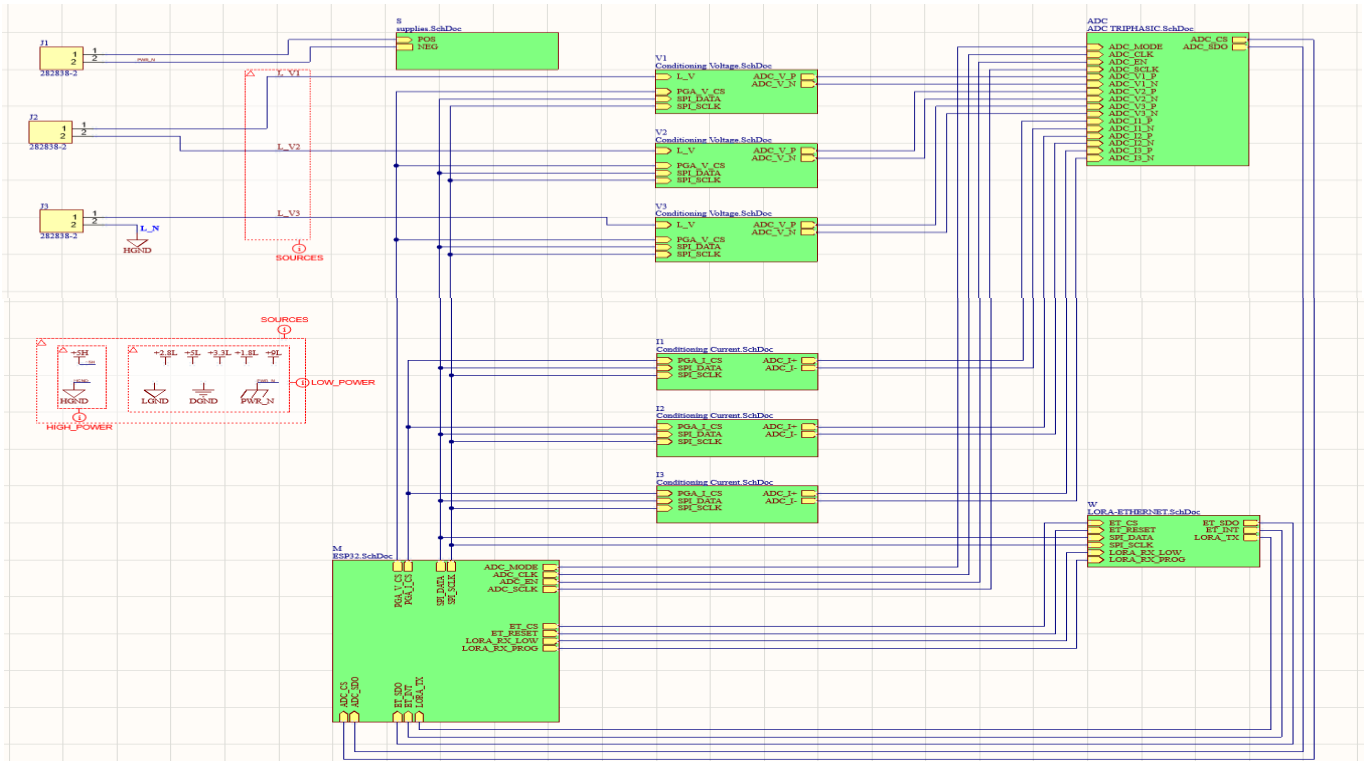

Fig. 12. Schematic of triphasic system

B. 3D Models

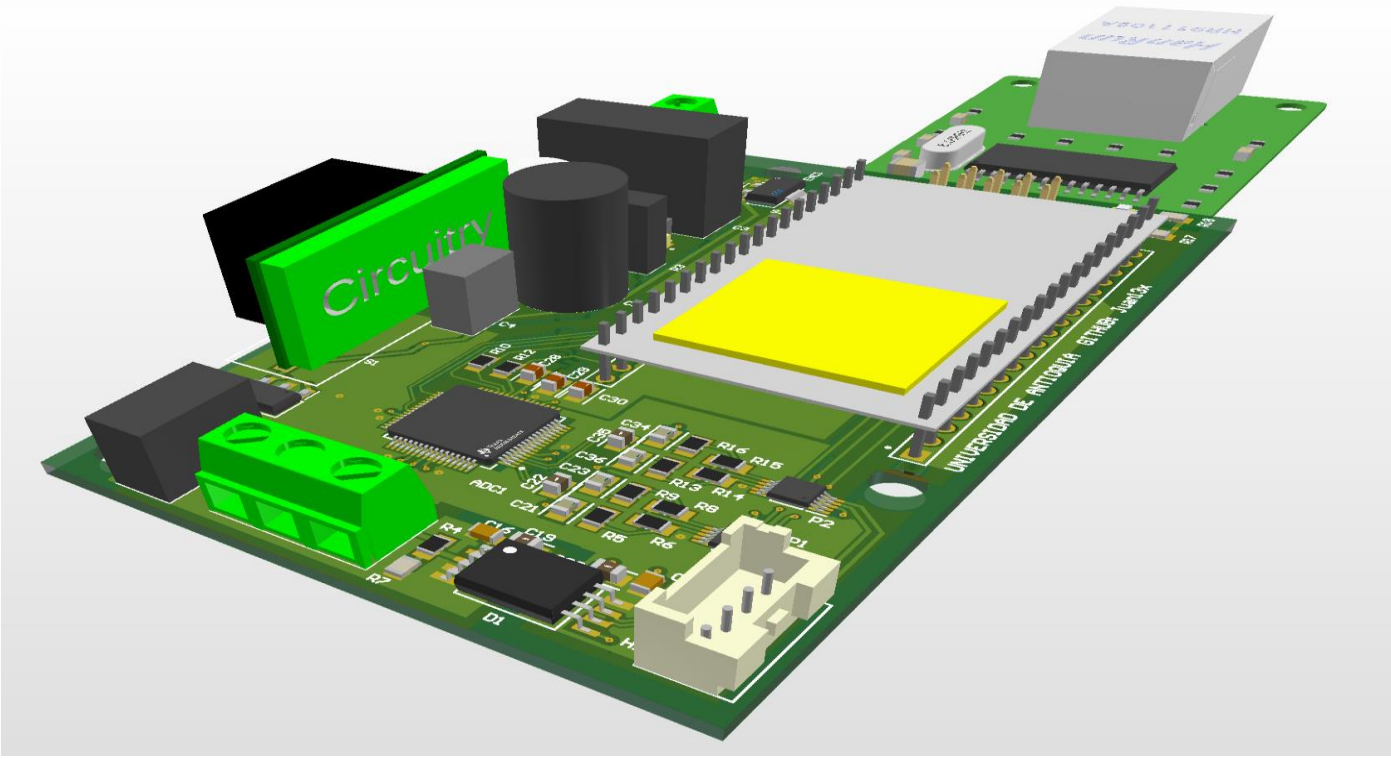

Fig. 13. 3D Model of the monophasic system

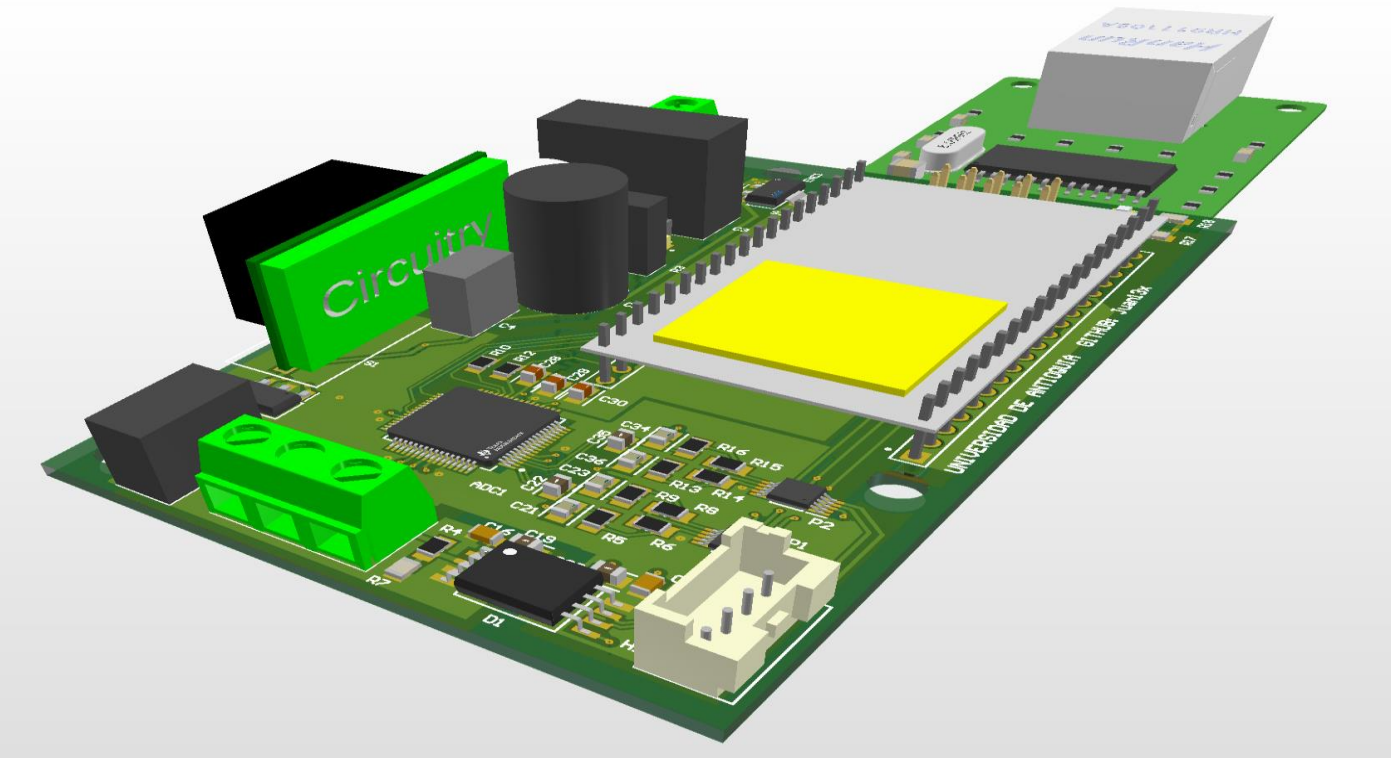

Fig. 15. 3D Model of the triphasic system

C. Physical PCB:

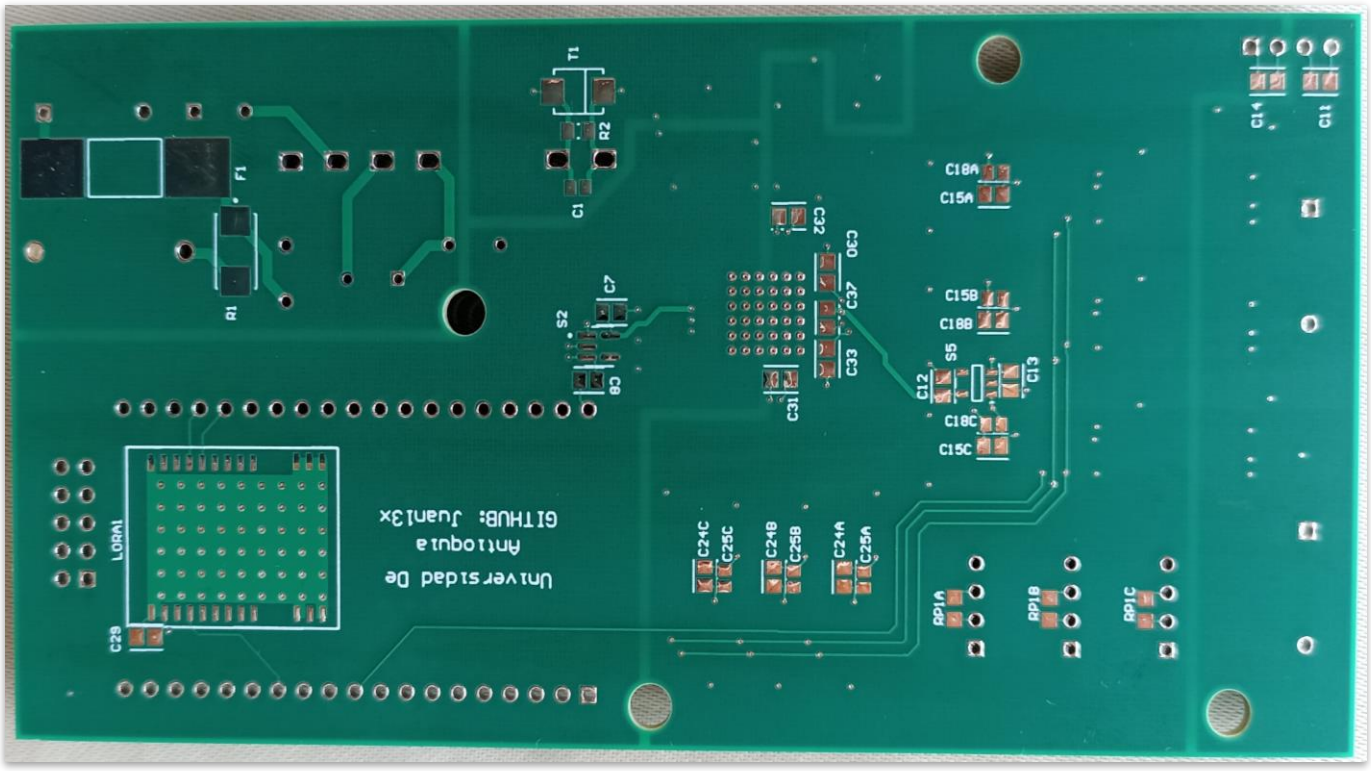

Figura 15. Bottom of physical PCB

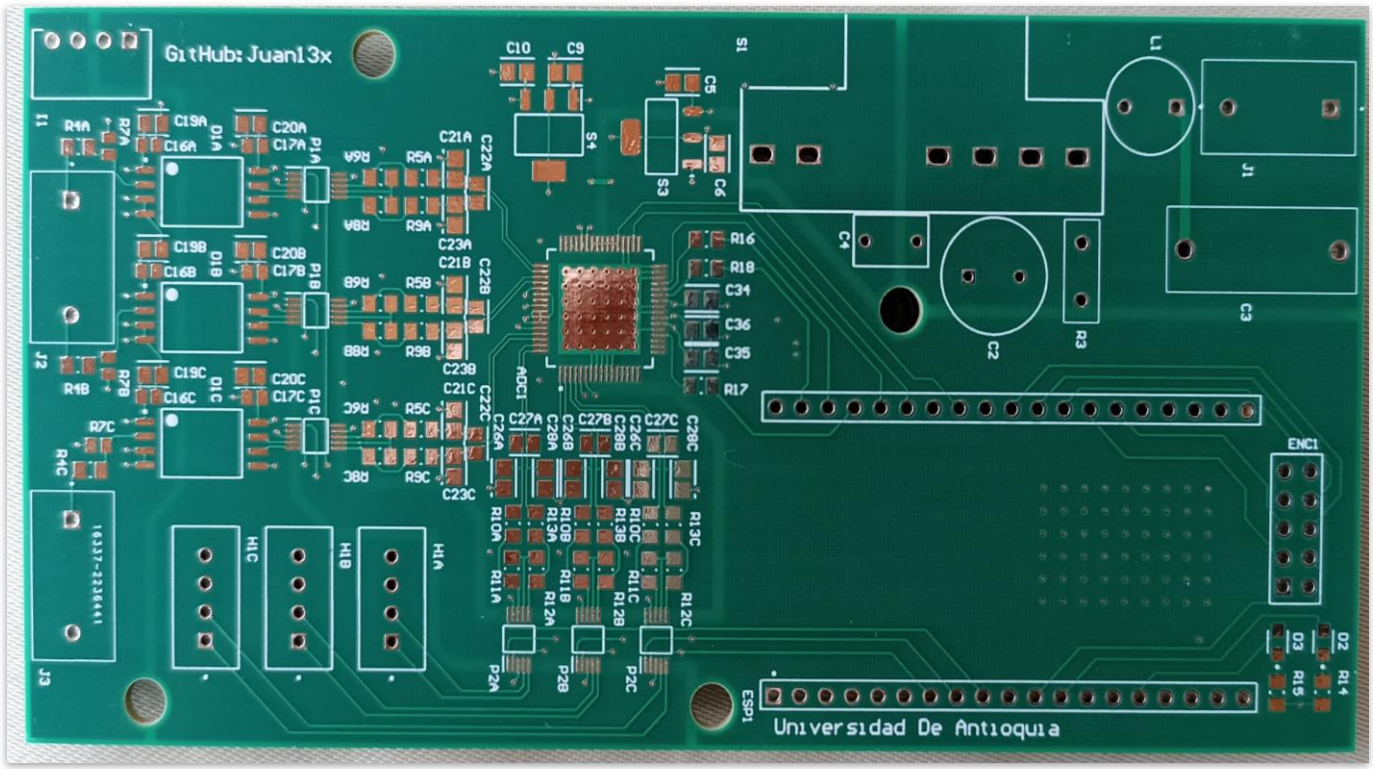

Figura 16. Top of physical PCB

D. BOOM

TABLE 11. Production price 1 vs 100 units

Units	Monophasic Production Price ($)	Triphasic Production Price ($)
1	95 + 6.20 = 101.2	172 + 10.625 = 182.625
1000	63 + 1.225 = 64.225	112 + 2.575 = 114.575

TABLE 12. Commercial products

Commercial Reference	Commercial Price ($)	Application
S31 & S31 Lite Wi-Fi Smart Plug US Type	19	Domestic
ADW300 IoT 3-phase Wireless Smart Energy Meter	85	Domestic, industrial
EFR32xG21 Wireless Gecko Starter Kit	479	Industrial, High Quality

E. Reports:

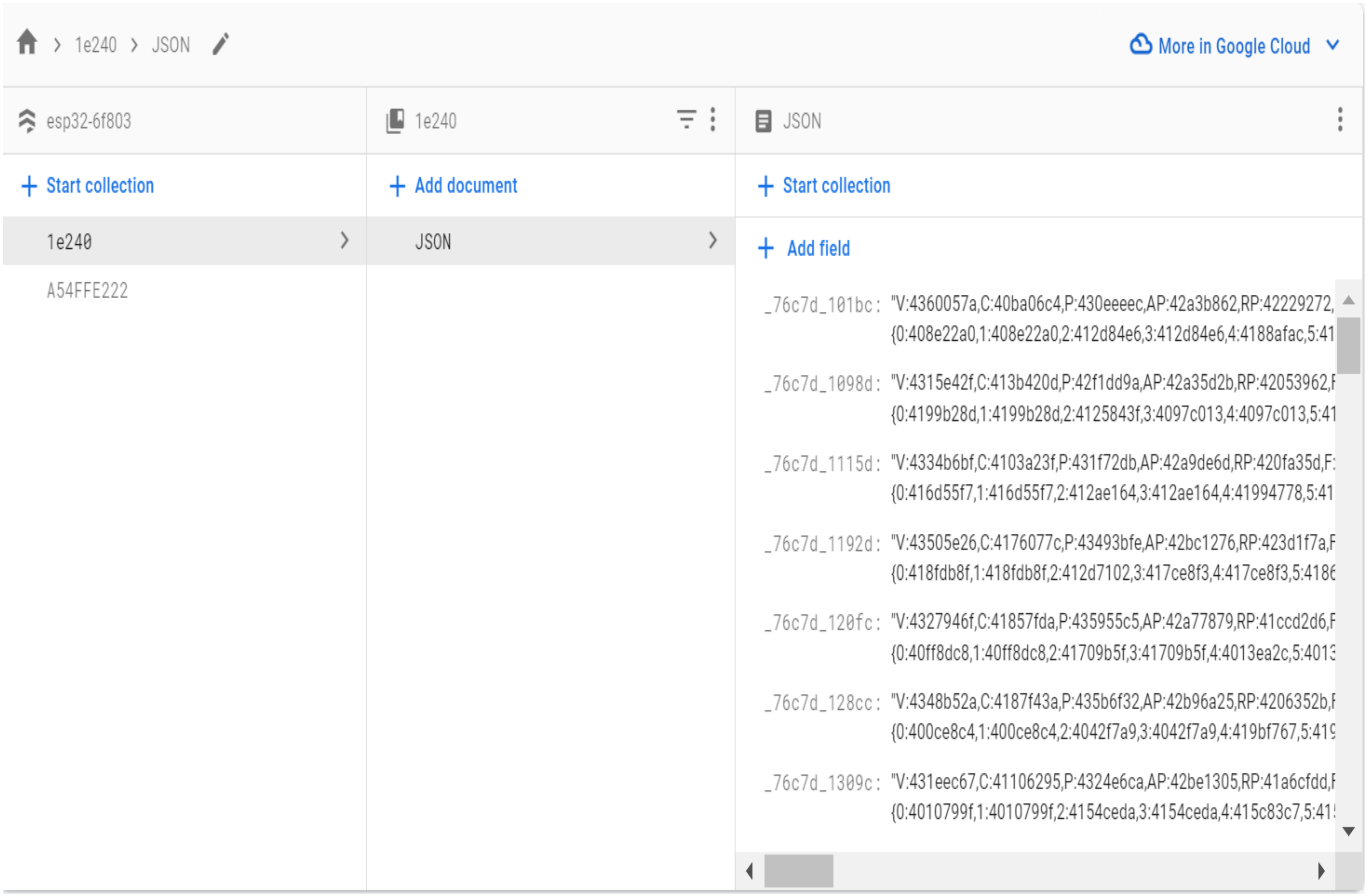

Fig. 17. Report to Firestore Database.

VII. ANALYSIS

Fig. 17 shows some data recorded in the Firestore database. Note how the data structure resembles the format describe for the database, stated at the design process for the database (section V → literal C → numeral 2). The current data of the payload is simulated, not measured from the power line. This is because some components haven't been welded on the PCB by the writing of this thesis, due to delays in the arrival of them. With this, it is checked that a connection with Firestore database was successful.

By analyzing the schematics and the 3D models, Fig. 11-14, it can be inferred that the systems are very similar. In fact, the DC system is the same as the monophasic and the triphasic one is an extension of the former. This is important because it helps to reduces production costs, by buying more quantity of each component. Of course, for this prototyping version just a few samples were design, but for a mass production the price would drop down significantly, as indicated in TABLE 11. However, even with 1000 samples is not enough to compete against commercial products. It is important to acknowledge that the developers of these products reuse their designs into multiples projects to reduce cost, and on top of that, many design use ICs that calculate all the variables they need. I.e., cheaper but limited.

TABLE 12 displays the commercial price for 3 commercial references of smart meters; 1 is for domestic use, another for domestic and industrial, and the last one is special for industrial purposes and includes high quality features. Our product is very similar to this last one when it comes to analog quality, but is overwhelmed for all its software functionalities, which means there are a lot of improvements to do.

With the current state of the smart meter, it is possible to connected to any data base. Here, on this bachelor's degree, only Firebase was accounted. It is possible to implement DSP algorithms to make very simple calculation, like calculating the voltage of the power line, or very complex algorithm with machine learning. Still, there are problems unsolved: It has no security or data encryption or well-defined steps to warn about problems on the network, like alarms or notifications, only the led indicator.

The system was designed as a prototype of a smart meter; a system that provides several tools for a utility programmer or engineer to satisfy many needs presented in a smart grid. Its features make it perfect to operate in very environments, such as domestic or industrial, monophasic o triphasic power lines. However, there's still work to do to incorporated it into an AMI.

In this way, a future works might consist in connecting the smart meter to a MDMS or an AMI. In this case, Snap4City is a tempting option as the new data platform. Also, a version with DSP algorithms is not so far to be accomplish. Remember that the data uploaded to the database was simulated, not measured from the power line. In general, this project, this smart meter, provides infinity of applications, it is up new researchers or programmer to exploit all its potential.

VII) Conclusions

-The system is capable to be supplied by AC or DC sources, whence it is adaptable to many scenarios: Domestic, academic or Industrial.

-The triphasic system is an extension of the monophasic one, and the DC system is the same as the latter. Whereby, it is a way to save costs for mass production.

-The system connects to the database, sends and receive (if requested)

-The ESP32 allows different type of implementations, resulting in a system with flexibility up to changes.

-The High-power side is isolated from the Low-Power Side, and the current is measured in a non-invasive way, reducing the possibility of damage from powerful transient on the power line. This leads to sustainability for the customer or companies.

-The ESP32 is a well-documented and popular microcontroller. This allows new programmers to understand and modify the firmware easily. This leads to productivity and scalability.

-The quality of our product increases its priced, resulting in a product better for industrial or professional purposes.

VIII) References

[1] V. G. Vilas, A. Pujara, S. M. Bakre and V. Muralidhara, "Implementation of metering practices in smart grid," 2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM), Avadi, India, 2015, pp. 484-487, doi: 10.1109/ICSTM.2015.7225465.

[2] B. S. England and A. T. Alouani, "Multiple Loads-Single Smart Meter for Measurement and Control of Smart Grid," 2019 IEEE Innovative Smart Grid Technologies - Asia (ISGT Asia), Chengdu, China, 2019, pp. 2440-2444, doi: 10.1109/ISGT-Asia.2019.8881529.

[3] G. R. Barai, S. Krishnan and B. Venkatesh, "Smart metering and functionalities of smart meters in smart grid - a review," 2015 IEEE Electrical Power and Energy Conference (EPEC), London, ON, Canada, 2015, pp. 138-145, doi: 10.1109/EPEC.2015.7379940.

[4] "Medellín Ciudad Inteligente". Alcaldía de Medellín. https://www.medellin.gov.co/es/secretaria-de-innovacion-digital/ciudad-inteligente/ (accedido el 15 de abril de 2023).

[5] "S31 & S31 Lite Wi-Fi Smart Plug US Type". Sonoff. https://sonoff.tech/product/smart-plugs/s31-s31lite/. (accedido el 15 de abril de 2023).

[6] "Reference Design to Measure AC Voltage and Current in Protection Relay with Delta-Sigma Chip Diagnostics". Texas Instruments. https://www.ti.com/tool/TIDA-00810. 2016.

IX) Appendixes

a. List of Components

TABLE 13. List of components

Component	Description	Order Part	Current(mA)
Clamp TVS Diode	22V Clamp 12VWM 27.3A Ipp Tvs Diode Surface Mount (DO-214AA)	SMBJ12E3/TR13	X
Inductor 2.2mH	2.2 mH, 350 mA 3.2Ohm Max, 5mm Radial, Vertical Cylinder	RLB1112V4-222J	X
Fuse 1 - 2A	2 A 250 V AC DC Fuse Cartridge, Glass Requires Holder 5mm x 20mm	0618002.MXP	X
Varistor (MOV)	VARISTOR 130VAC Varistor Voltage 200V 1.2KA DISC 7MM	MOV-07D201KTR	X
Cap 2.2nf Low Voltage	CER 2200PF 50V C0G/NP0 0805 5%	CL21C222JBFNNNG	X
Cap 0.1uf Low Voltage	CER 0.1 µF ±10% 50V X7R 0805	CC0805KRX7R9BB104	X
Cap 1uf Low Voltage	CER 1UF 25V X7R 10% 0805	CL21B105KAFNFNE	X
Cap 10uf Low Voltage	CER 10UF 10V X7R 0805 10%	GRM21BR71A106KA73K	X
Cap 0.1uf High Voltage	CAP FILM 0.1UF 10% 310VAC RADIAL 7.5mm	104MKP275KC	X
Cap 1nf High Voltage	CAP FILM 1nF 10% 400VDC 200VAC RADIAL 5mm	R82MC1100DQ50K	X
Cap 10pf Low Voltage	CAP CER 10PF 50V C0G/NP0 0805	C0805C100J5GACTU	X
Cap 22uf high Voltage	22 µF 200 V Aluminum Electrolytic Capacitors Radial 5mm	UCY2D220MPD1TD	X
SMD 2.32M ohm RES	SMD RES 2.32M OHM 5% 1/4W 0805	RS-2.2M-0805 *	X
SMD 1.2M ohm RES	SMD 1.2M OHM 5% 1/4W 0805	RS-1.2M-0805 *	X
SMD 1M ohm RES	SMD 1 MOhms ±0.1% 0.333W 1206 25ppm/°	RNCF1206BKE1M00	X
SMD 10.2k ohm RES	SMD 10.2K OHM 0.1% 1/8W 0805 25ppm/°	ERA-6AEB1022V	X
SMD 10k ohm RES	10K OHM 0.5% 1/4W 0805 25ppm/°C	RNCF0805DTE10K0	X
SMD 100 ohm RES	Resistencia 100Ω 0805 SMD 1/4W 5%	RS-100R-0805 *	X
SMD 47 ohm RES	SMD 47 OHM 5% 1/4W 0805	RS-47R-0805 *	X
SMD 6.8 ohm RES	SMD 6.8 OHM 5% 2W 2616 Wirewound	SMW26R8JT	X
AMC1350DWVR	Fully Differential Isolated Op Amp Rail-to-Rail	AMC1350DWVR	18
MAX9939	PGA SPI interface fully differential Input and Output, biased output	MAX9939AUB+T	7
ENC28J60	Ethernet Module on Board with Rj45 connector	ENC28J60***	200
ESP32-WROOM-32D-DEVKIT	MCU with embedded Bluetooth and WIFI connectivity	ESP32 – WROOM - 32D – DEVKIT *	400
E78-868LN22S	LORA module, LORAWAN, Ipex antenna, UART Interface	E78-868LN22S**	132
868MHz Ipex Antenna	868 - 915 MHz Ipex antenna	ANT-900MHZ-3DBI*	X
ADS1174	ADC 4 differential channels, high CMRR, 16 bits, variable voltage reference, SPI interface, embedded filter with passband (0.1 dB) spanned up to Cutoff frequency. Sampling Rate ≥ 6.3ksps.	ADS1174IPAPR	**1 Channel:** 11 mA
ADS1178	The same as above but with 6 channels	ADS1178IPAPR	//
L37S300S05M	Isolated Hall-sensor, |current range| ≤ 300 A, biased output	L37S300S05M	36
Voltage Regulator 5V	REG LINEAR 5V 1A SOT223 1% accur	AZ1117IH-5.0TRG1	X
Voltage Regulator 3.3V	IC REG LINEAR 3.3V 1A SOT223 1% accur	AZ1117CR-3.3TRG1	X
Voltage Regulator 2.8V	IC REG LINEAR 2.8V 150MA SOT23-5	R1180N281B-TR-FE	X
Voltage Regulator 1.8V	1.8V IC Positive Fixed 1 Output 300mA 5-TSOP 1% accur	NCP114ASN180T1G	X
AD DC Converter	Open Frame AC DC Converters 1 Output 9V 1.1A 85 ~ 305 VAC, 100 ~ 430 VDC Input	LS10-13B09R3	X
DC DC Converter	Isolated Module DC DC Converter 1 Output 5V 200mA 4.5V - 5.5V Input 1% accuracy (in range of needed operating)	1S4AE_0505S3UP	20
Led Rojo SMD 0805	Led Rojo SMD 0805	Led Rojo SMD 0805 *	~ 13

Led Verde SMD 0805	Led Verde SMD 0805	Led Verde SMD 0805 *	~ 13
Wire to Board Terminal	2 Position Wire to Board Terminal Block Horizontal with Board 0.394" (10.00mm) Through Hole	282838-2	X
Connector Header 4 pos	Connector Header Through Hole 4 position 0.098" (2.50mm)	B04B-XASK-1(LF)(SN)	X
M4 Screw 15mm	M4 Screw 15mm Length	T-M4-15 *	X
40p Female Header	40p Female Header 2.54mm	HD40P-H	X

Most components were purchased at *Digi-key Electronics*, those with a * were at *I+D Electrónica,* ** for Alibaba and *** at any available provider (our case, *Mercado libre Colombia*)

b. Sonoff schematic diagram

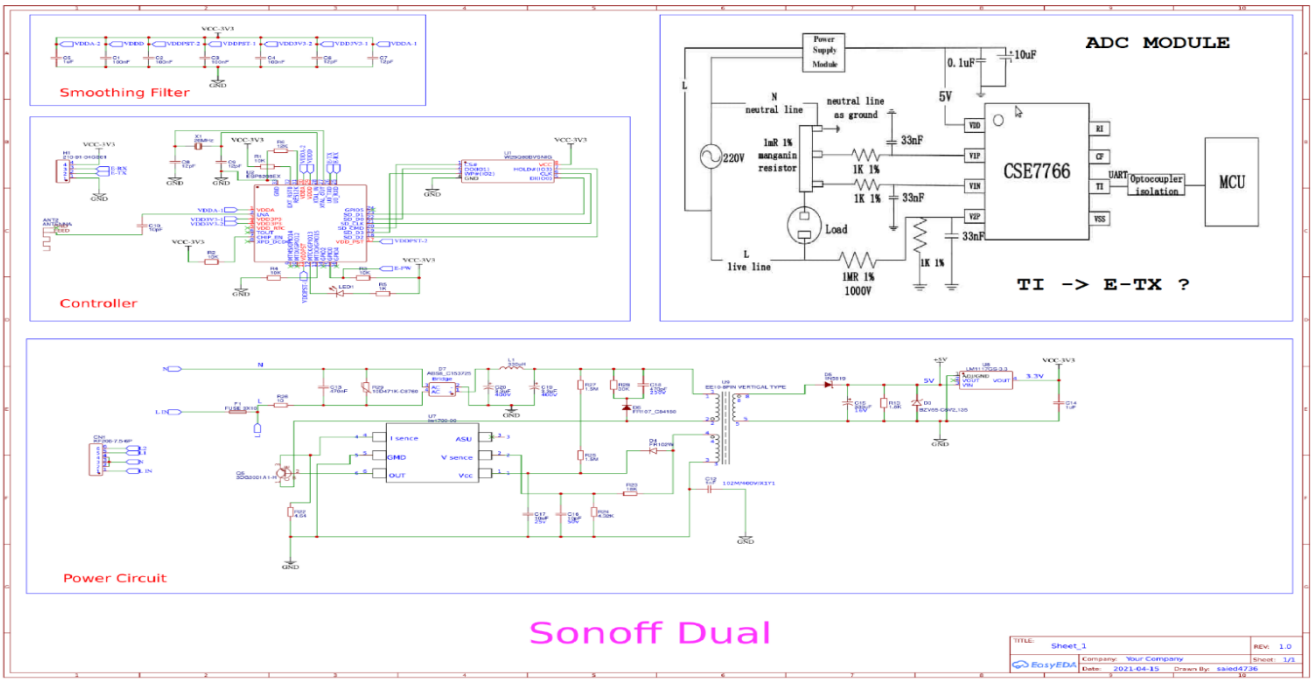

Fig. 18. Sonoff schematic diagram

c. Texas Instruments' schematic circuit design

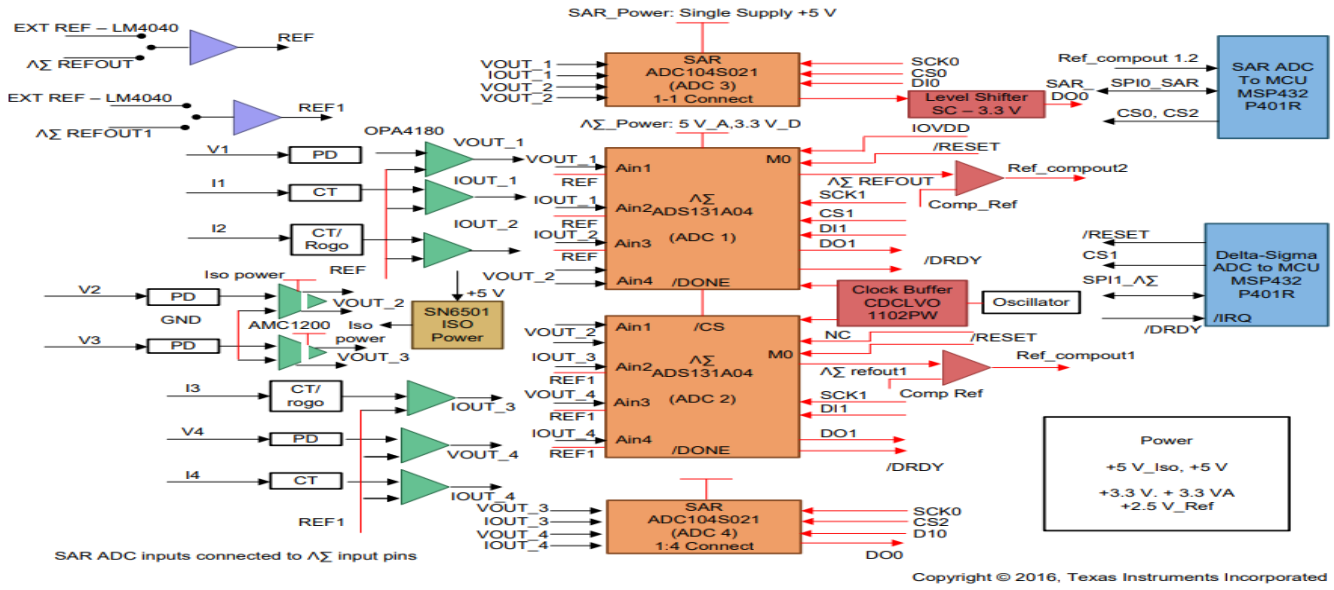

Fig. 19. Texas Instruments' schematic circuit design

d. Monophasic Schematic design

1. Hierarchy:

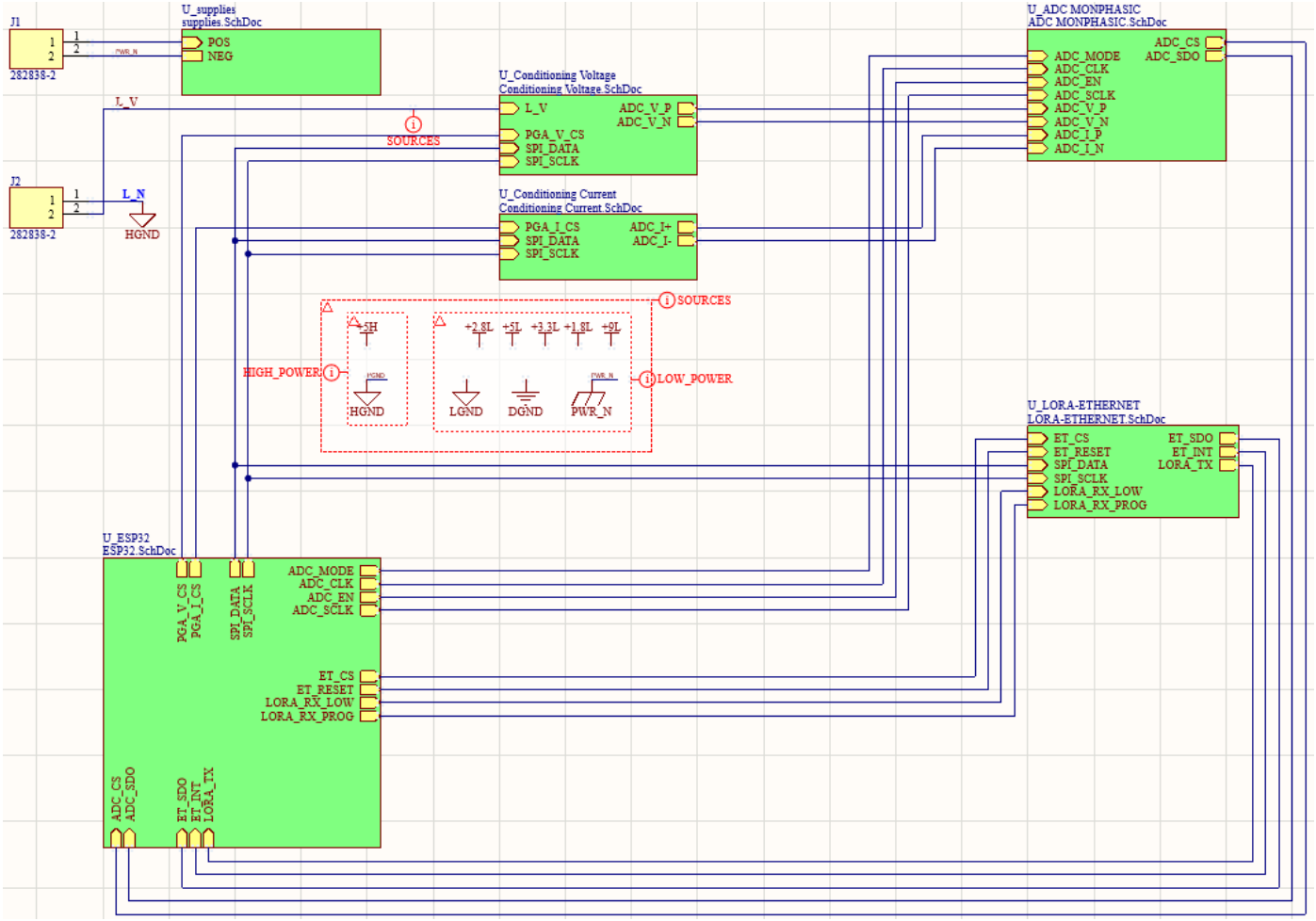

Fig. 20. Hierarchy of the monophasic design

2. Voltage

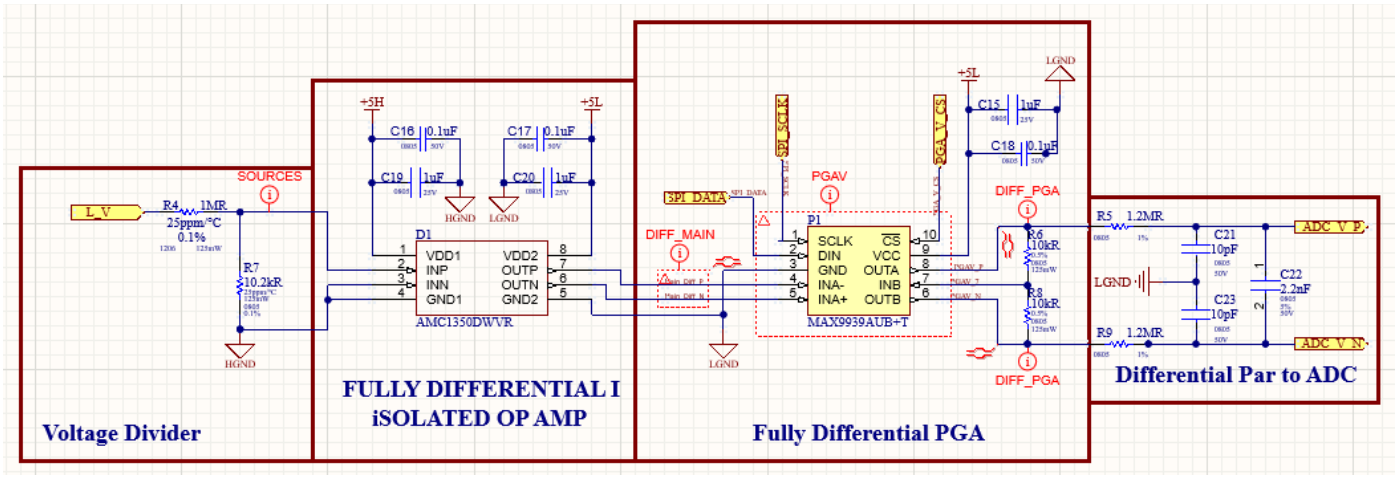

Fig. 21. Voltage conditioning system of the monophasic design

3. Supply

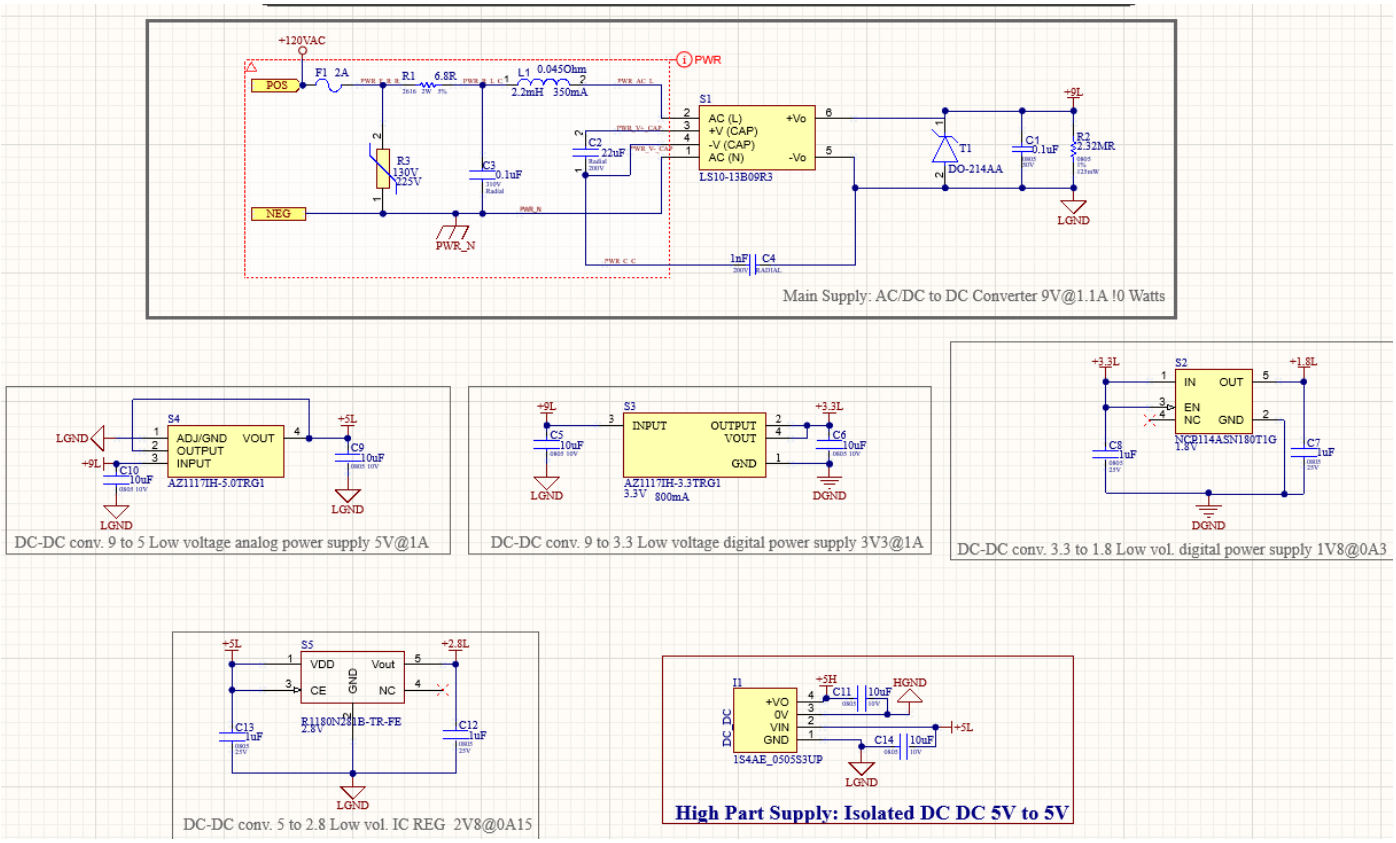

Fig. 22. Supplies of the monophasic design

4. Current

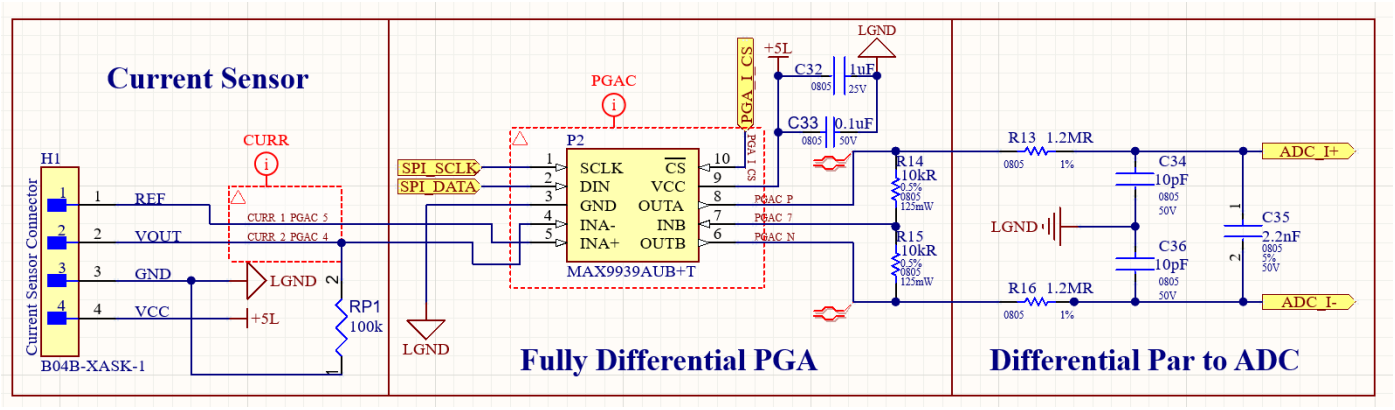

Fig. 23. Current conditioning system of the monophasic design

5. ESP32

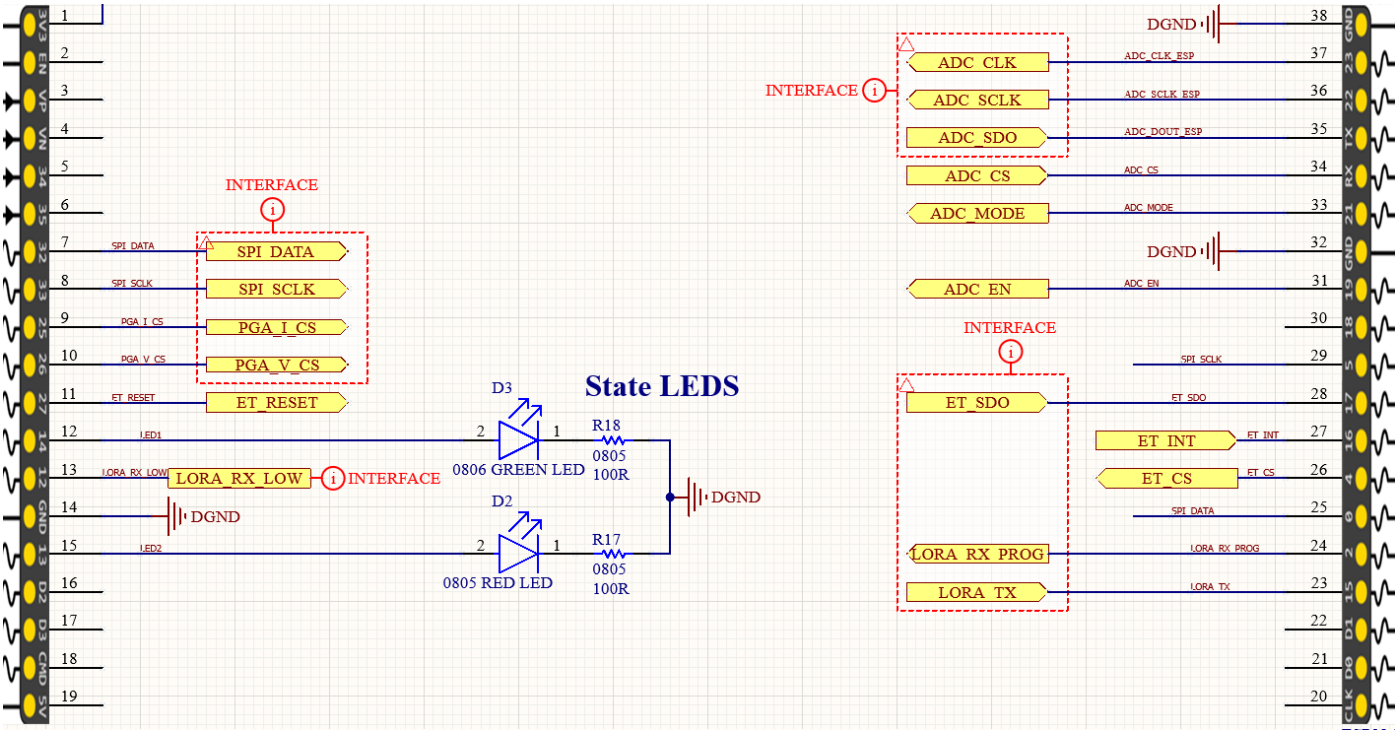

Fig. 24. ESP32 connections of the monophasic design

6. LORAWAN and ENC28j6

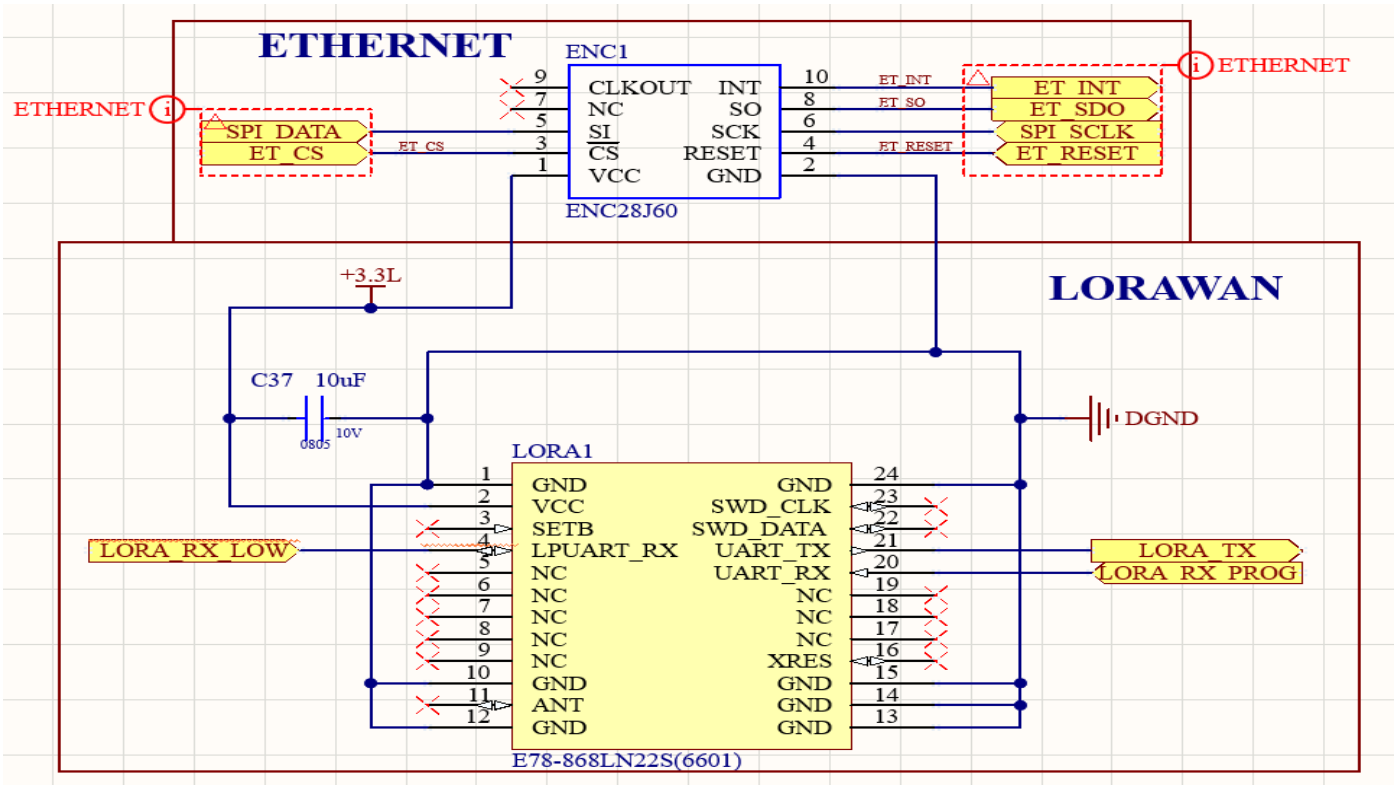

Fig. 25. External communication modules connections of the monophasic design

7. ADC

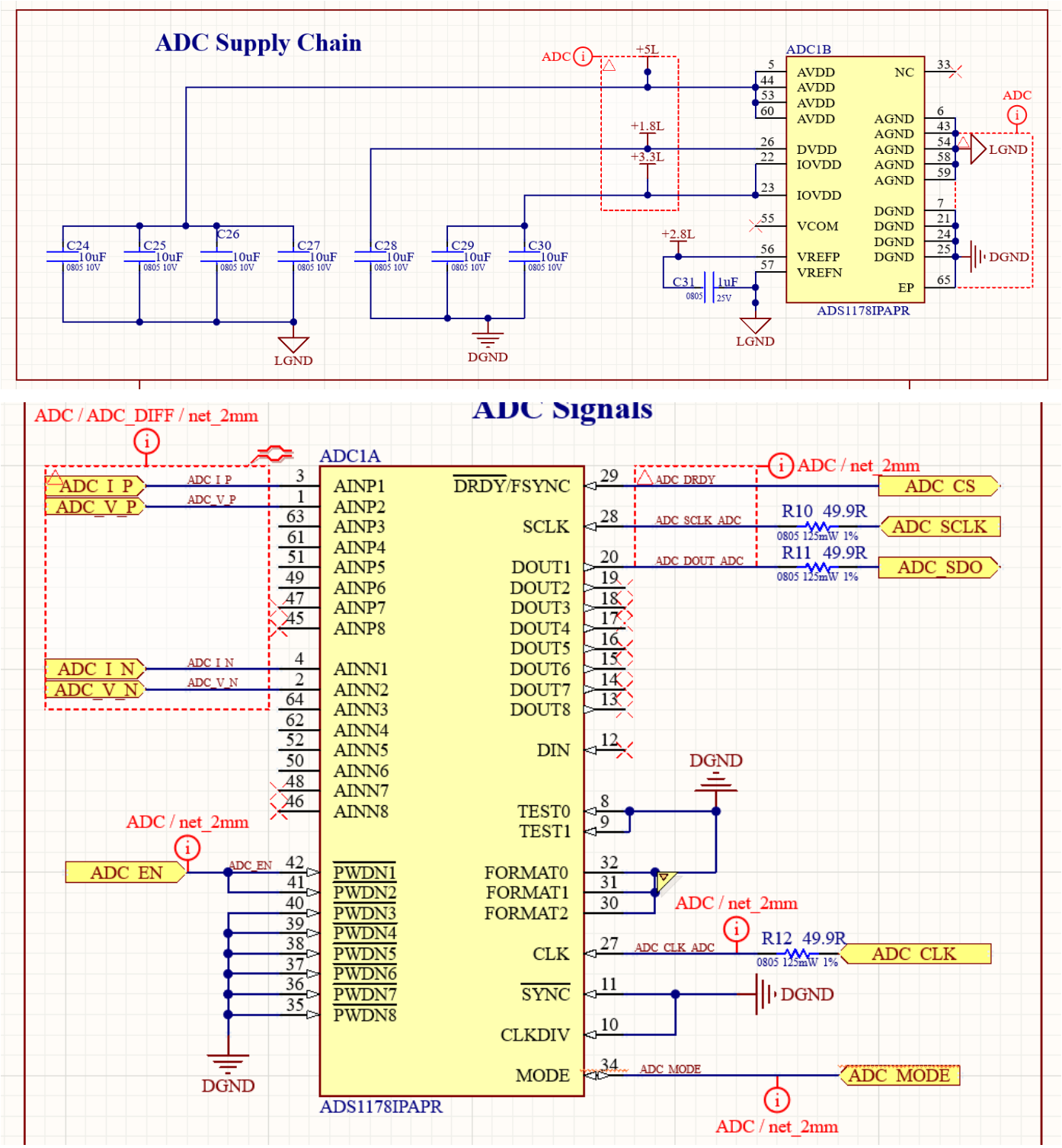

Fig. 26. ADC connections of the monophasic design

8. 3D Model

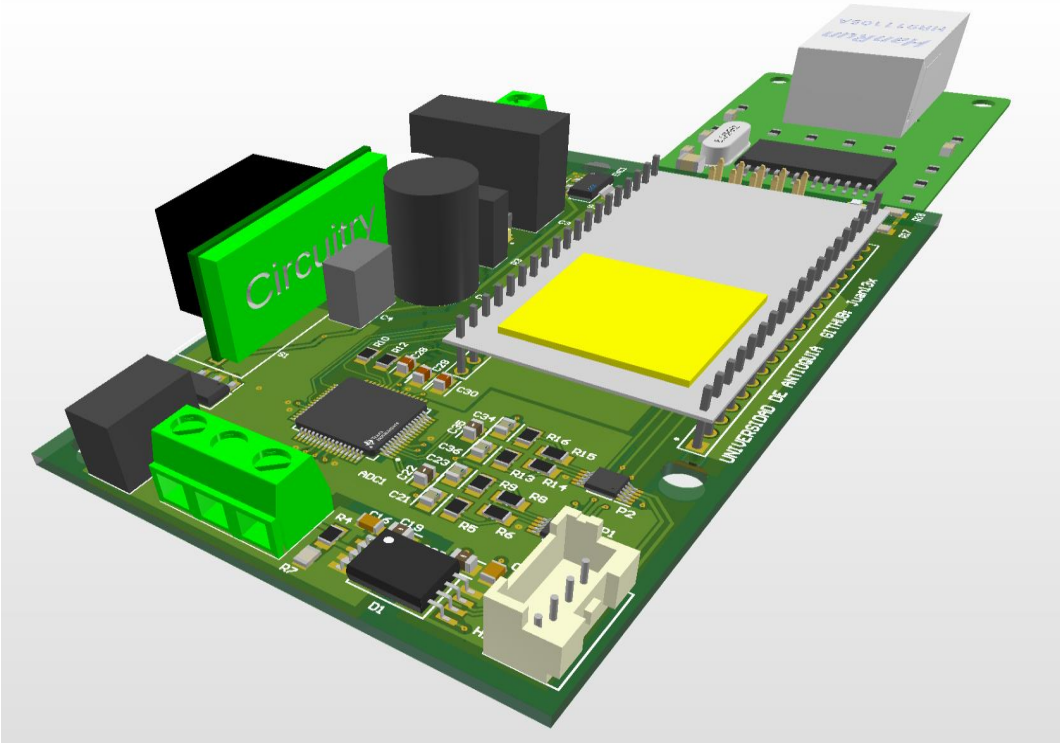

Fig. 27. Top View monophasic system

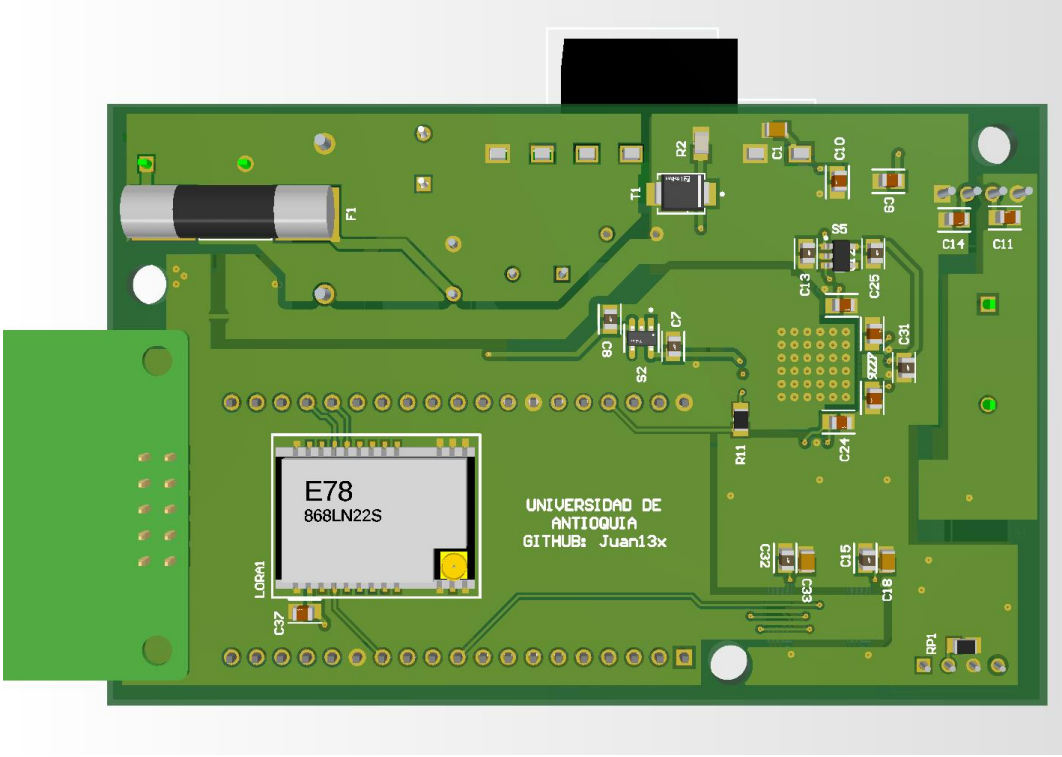

Fig. 28. Bottom View monophasic system

e. Schematics Triphasic design

1. Hierarchy

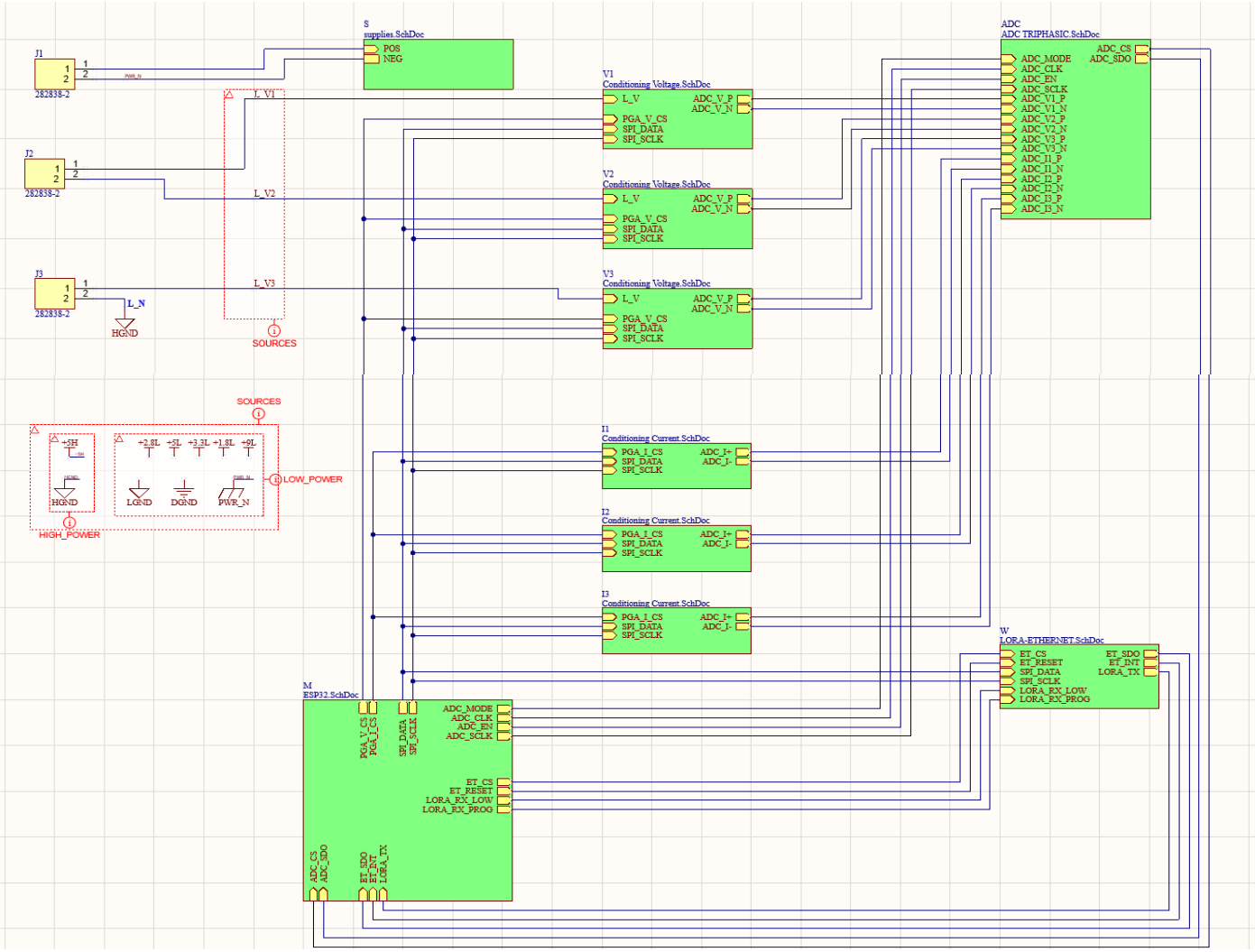

Fig. 29. Hierarchy of the triphasic design

2. Voltage

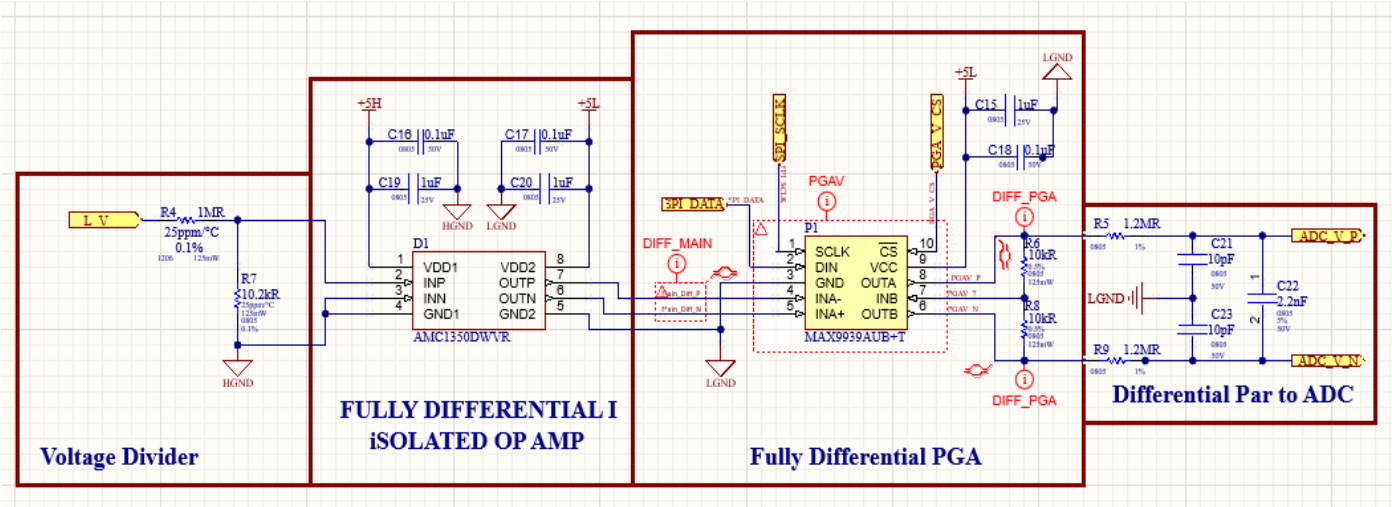

Fig. 30. Voltage conditioning system of the triphasic design

3. Supply

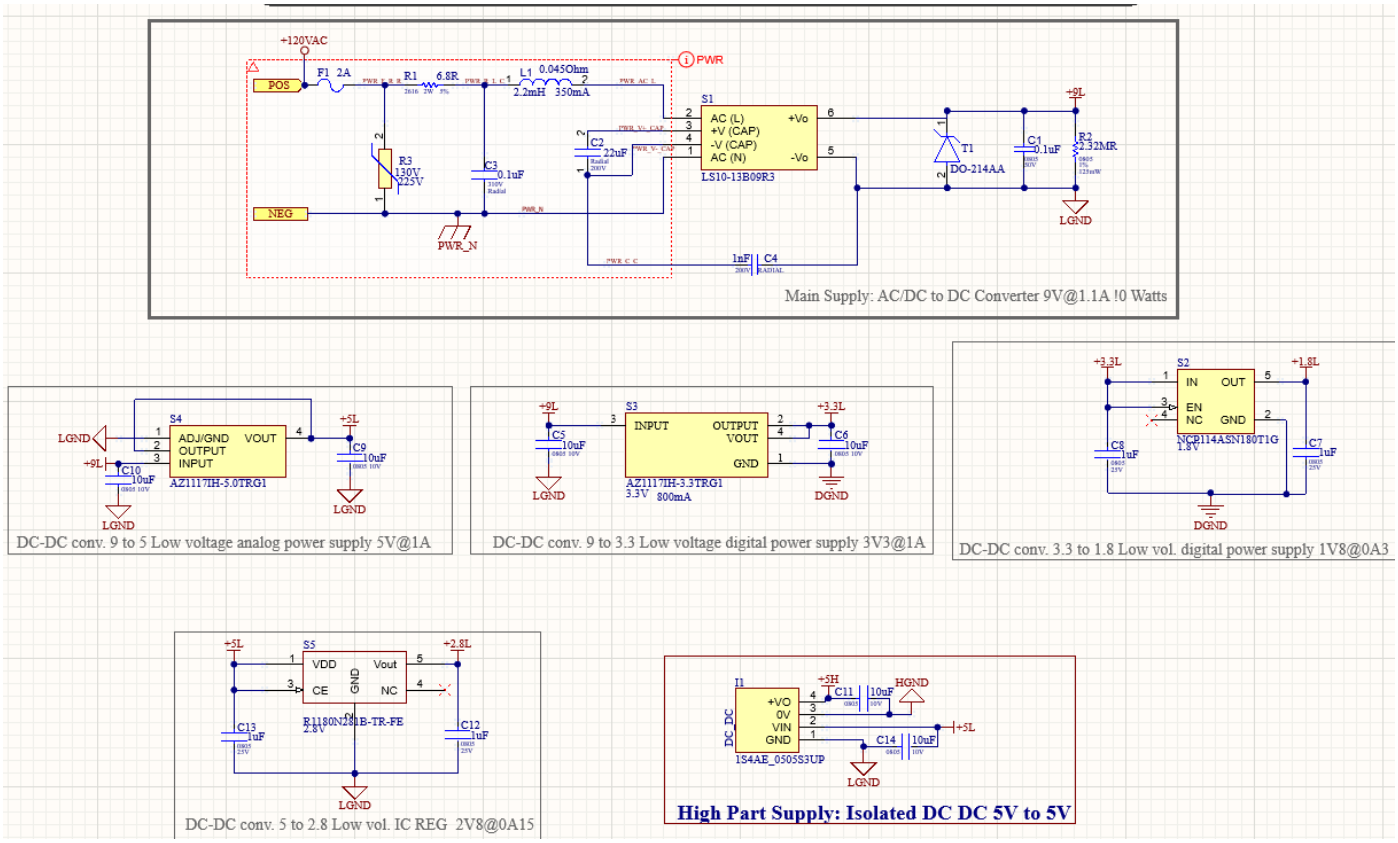

Fig. 31. Supplies of the triphasic design

4. Current

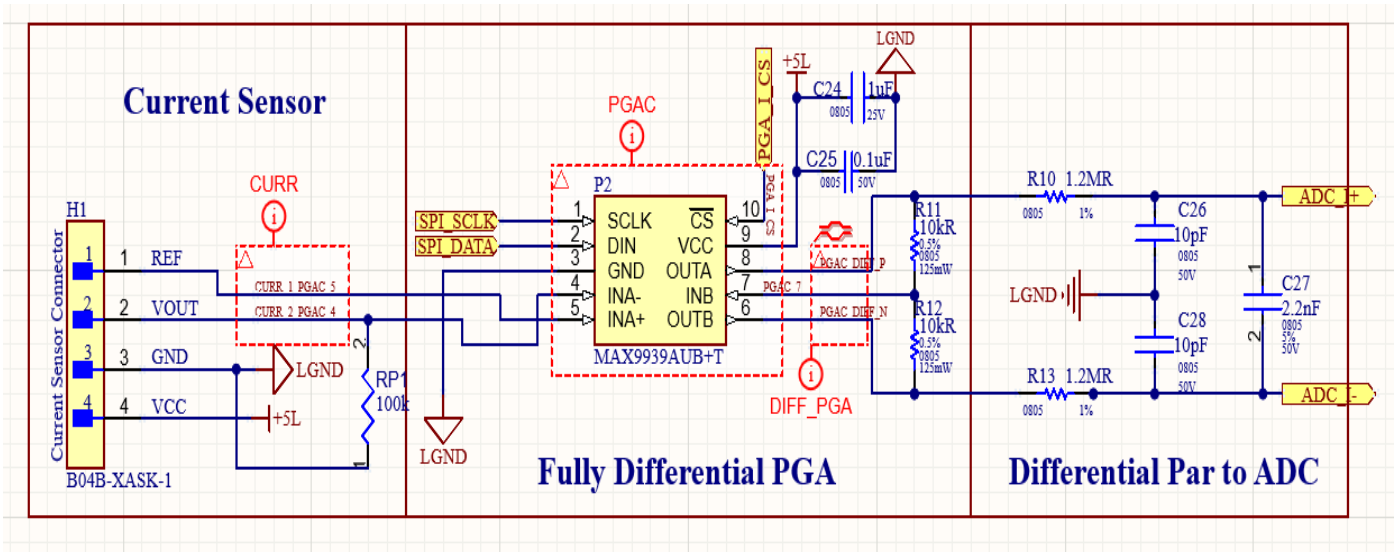

Fig. 32. Current conditioning system of the triphasic design

5. ESP32

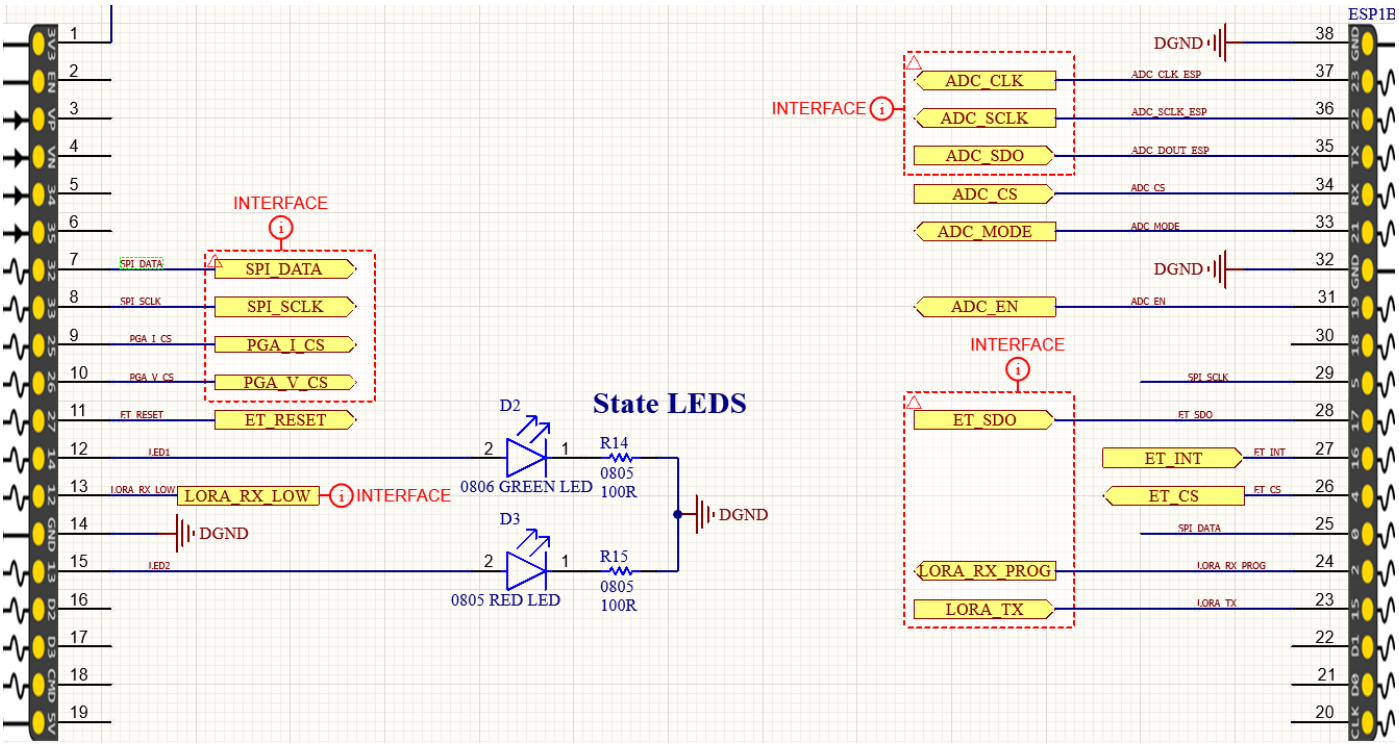

Fig. 33. ESP32 connections of the triphasic design

6. LORAWAN and ENC28j60

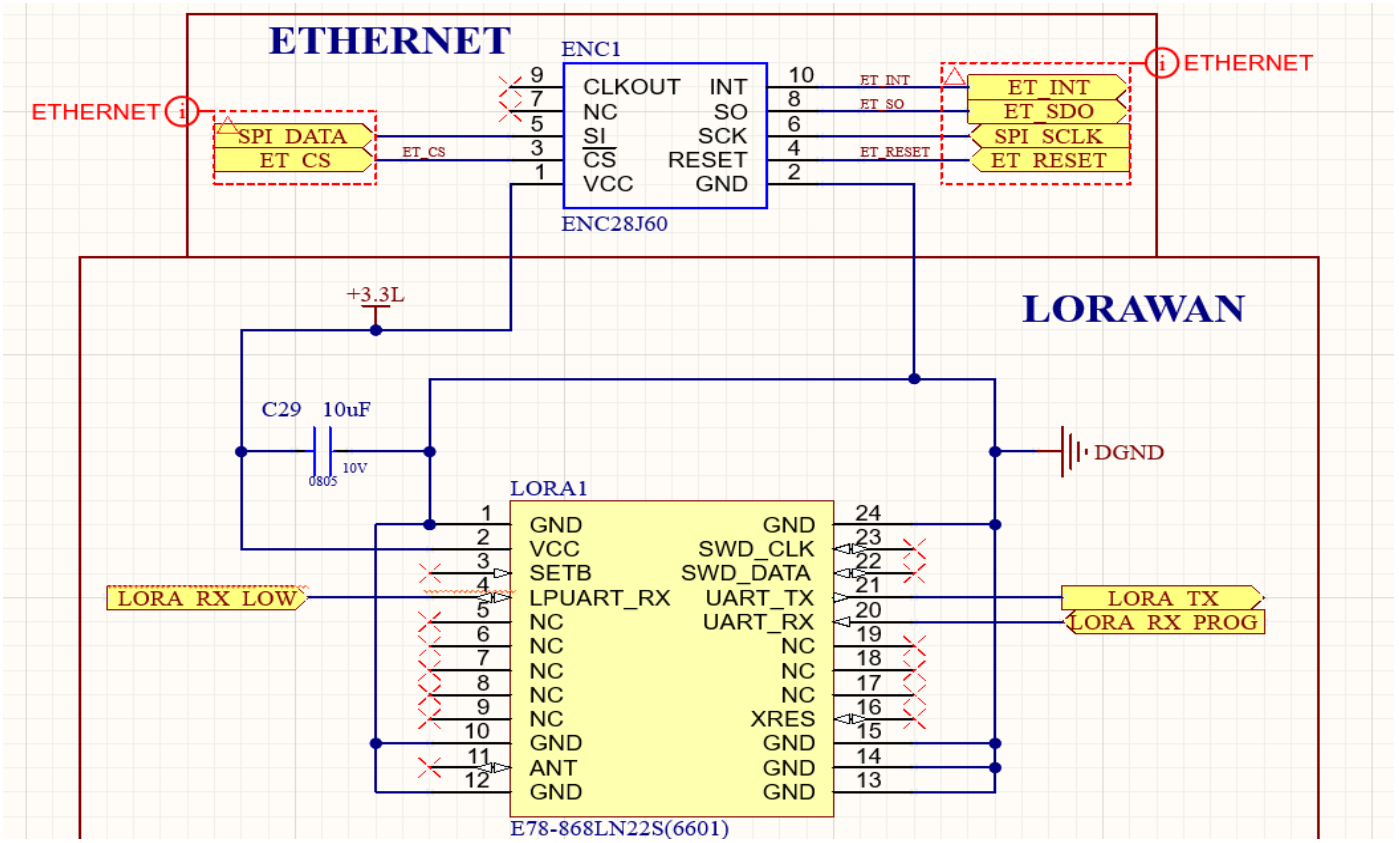

Fig. 34. External communication modules connections of the triphasic design

7. ADC

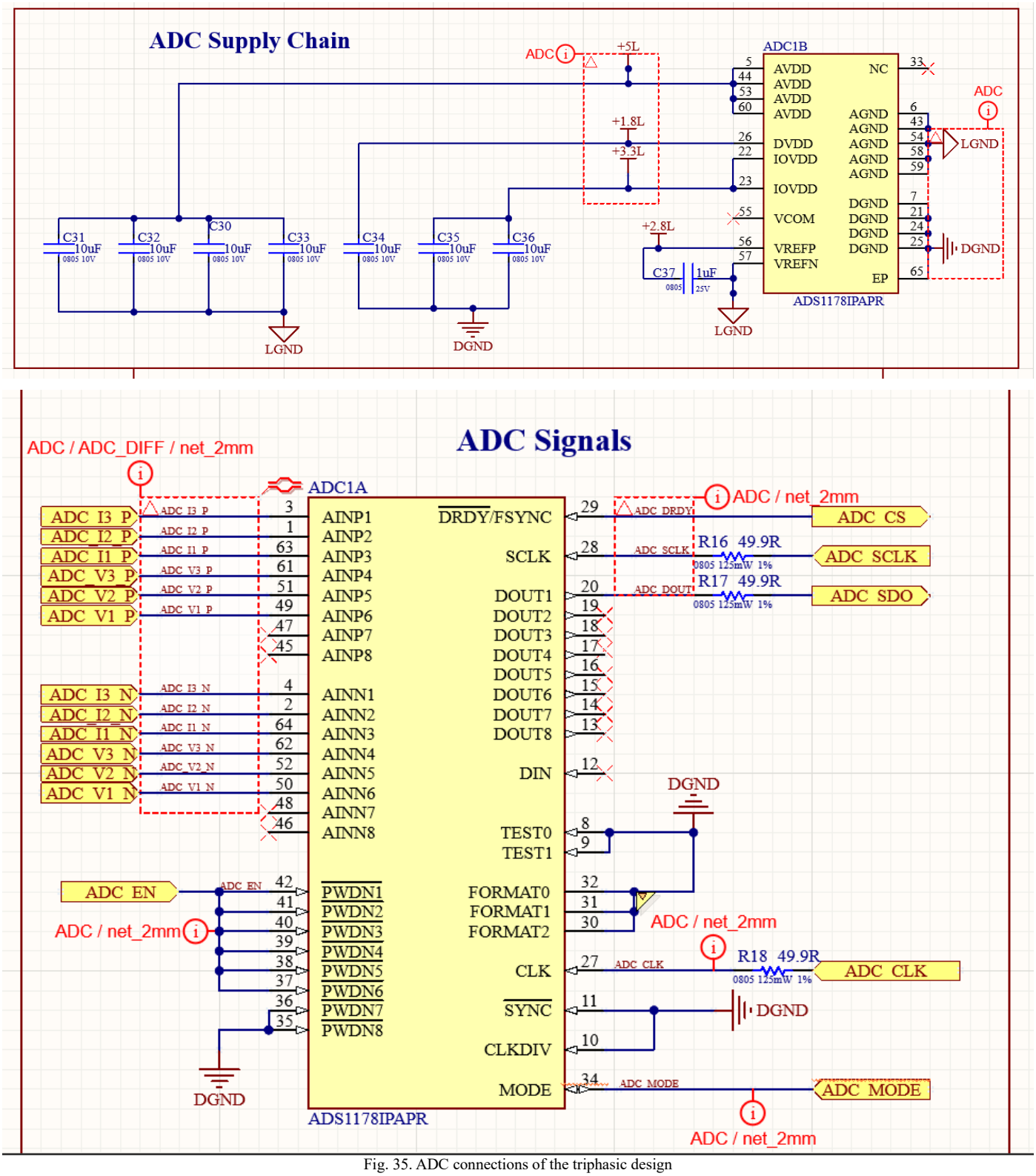

Fig. 35. ADC connections of the triphasic design

8. 3D Model

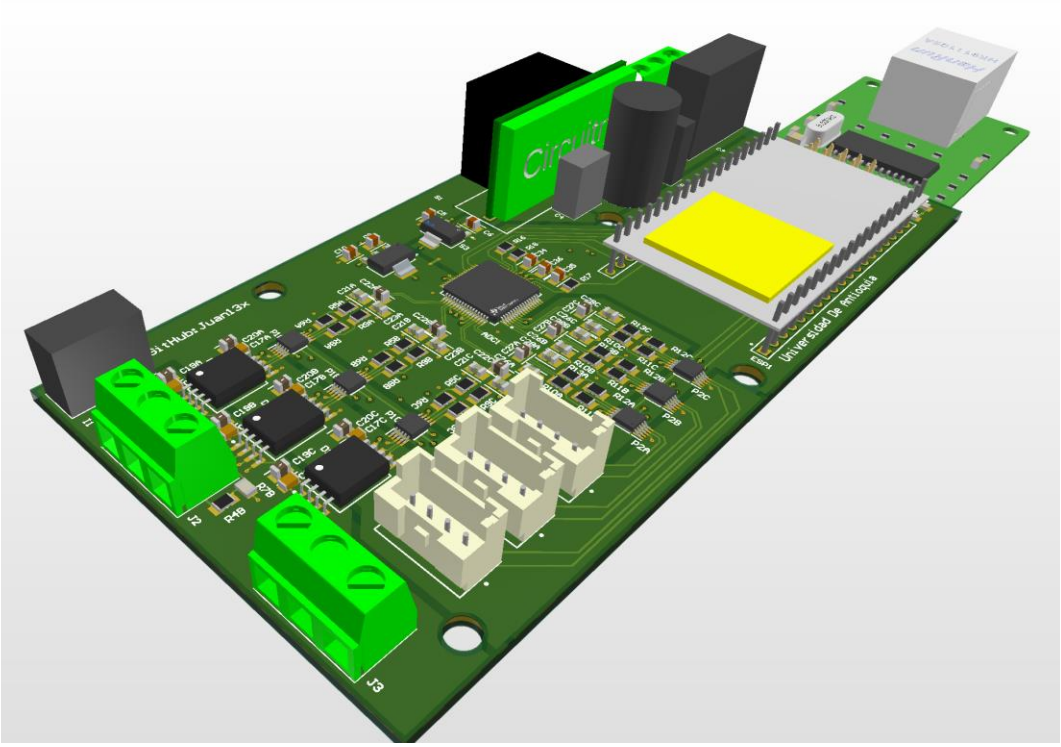

Fig. 36. Top view of the triphasic design

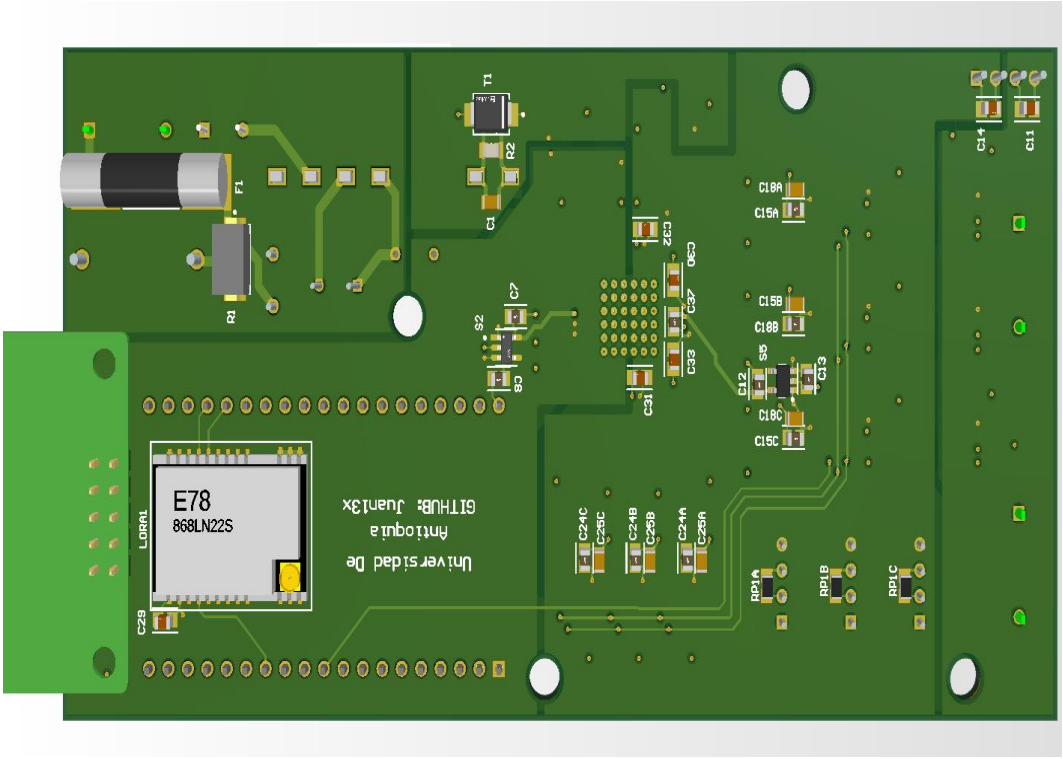

Fig. 37. Bottom view of the triphasic design