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IMPLEMENTATION OF SLIDING MODE CONTROL IN A SEMI-BRIDGELESS BOOST CONVERTER WITH POWER FACTOR CORRECTION

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Abstract

In this research work was implement a Sliding Mode Control (SMC) for a Semi Bridgeless Boost Converter with Power Factor Correction (SBBC PFC). SMC is presented in order to improve the cascade PID controllers currently used in the SBBC PFC. SBBC PFC control needs to manage the energy interchange between load and electrical grid; therefore, SMC is presented as a better control strategy (stable, robust and fast) in comparison with PI control in face of disturbances and normal operation. The SMC design will include SBBC PFC features, stability analysis considering disturbances, load in nominal operation conditions, Power Factor (PF) correction and Total Harmonic Distortion of Current (THDi) according to international normative IEC 61000-3-2. The main goal of this research consists on finding a sliding surface such that SBBC PFC dynamic behavior is improved being able to reject load and source disturbances. The SMC implementation was validated by means of Lyapunov stability criteria and simulation results.

Keywords: Sliding surface; Sliding mode control; Semi Bridgeless Boost Converter; Power Factor Correction; Total Harmonic Distortion.

General objective

• To find a sliding surface for SMC such that the SBBC PFC control dynamic behavior is improved and disturbances are rejected.

Specify objectives

• To obtain a SBBC PFC mathematical model taking into account the nominal operating conditions for control design.

• To propose a sliding surface considering control of input current and output voltage, ensuring the electrical energy quality according to the international normative IEC 61000-3-2.

• To validate the proposed sliding surface by means of sliding mode conditions and Lyapunov stability criteria.

• To validate the proposed sliding mode control by means of simulation results.

INTRODUCTION

This master work begins with an exhaustive search about of topologies of current-controlled rectifiers based on boost converter topology. This search is done in order to select the topology to be controlled with sliding mode control. It is presented as result the paper "A Review of Single-phase AC/DC Boost Converter Topologies with Power Factor Correction for Sliding Mode Control Purpose" (paper annexed); this paper will be submitted to journal "Electronics" (category Q1) from MDPI. In this paper, basic peration , advandsfdfsdfstages and disadvantages of several topologies were analyzed . In review , Semi -bridgeless topologies present better performance than Bridgeless topologies concern to control and electromagnetic compatibility . Then, the selected topology to control with sliding mode control is "semi -bridgeless boost converter with clamped diodes ". This topology presents low CM and DM noise, also power switches can be actuated with the same control signal.

Second paper "Development of a Distribution Static Compensator D-STATCOM: Prototype that will favor the development of devices based on power electronics" gives specifications related with hardware for power electronics devices that includes Semi bridgeless boost converter; this paper will be submitted to journal "Revista AIE". In this paper, considerations to Printed Circuit Boards (PCB) for measurement of voltages and currents as well as power electronics components are presented.

Third paper "Consideraciones técnicas para la sintonización de los controladores de un D-STATCOM real a partir de un modelo simulado" gives specifications about firmware related with control of power electronics devices; this paper is published in journal "Avances Investigacion En Ingenieria" (category C). Fourth paper "Banda de Histéresis Adaptativa para un Convertidor AC-DC Elevador sin Puente, con Correccion del Factor de Potencia y Control por Modos Deslizantes" presents the basic about sliding mode control; this paper is published in journal "Información Tecnológica". This paper shows the procedure to implement an adaptive hysteresis band for sliding mode control in order to avoid switching issues.

Finally, main contribution and results of this research work (it is recommended to revisors take special attention) is in the paper "Sliding Mode Control with Adaptive Hysteresis Band for a Semi-Bridgeless Boost Converter: Simultaneously, Power Factor Correction, Integrative Error and Output Voltage

Control"; this paper will be submitted to journal "Electronics" (category Q1) from MDPI. This paper proposes, presents and analyses a sliding surface for controlling both input current and output voltage without external linear control or PWM signal for the selected topology. Also, a comparative analysis about dynamic behavior is done between proposed SMC, classical PI and hybrid PI-SMC controllers.

Other paper related with this master research are: 1) Unified method for teaching how to solve the equivalent circuit of transformers; this paper is published in journal "Revista espacios". Power electronics devices need an electrical grid coupling, this link generally is done with transformers. Also, AC/DC converters can be modeled as transformers and this paper presents a procedure to obtain transformer variables in steady state. Main variables to considered for AC/DC converters and transformers are voltages, currents, powers, losses, efficiency and sequence group. 2) Power Loss Minimization for Transformers Connected in Parallel with Taps Based on Power Chargeability Balance; this paper is published in journal "energies" (category Q1). This paper uses an optimization method to set taps of transformers in parallel connection. In this master research work, the sliding coefficients are were set according to behavior in simulation, nevertheless, an optimization method as genetic algorithm can be used for a future research work.

MDPI

Article

Review of PFC Single-Phase AC/DC Boost Converters: an Overview of Bridge, Semi-bridgeless and Bridgeless Topologies

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Abstract: This paper presents a review about state of the art for PFC single-phase AC/DC converters based on boost topology; a categorization semi-bridgeless and bridgeless) according to converter construction features is done in order to unify technical language for this devices; advantages and disadvantages of conventional, semi-bridgeless and bridgeless topologies are explored. An analysis of behavior, power factor correction, total harmonic distortion, control, power, electromagnetic compatibility, elements and efficiency for low, medium and high voltage applications is presented. New trends as well as arisen control techniques are discussed in order to compare and make a viability analysis between PFC boost converter topologies.

Keywords: Single phase AC/DC converter; bridge boost converter; semi-bridgeless boost converter; bridgeless boost converter; power factor correction; review

1. Introduction

Economical issues by electrical energy consumption are directly related with Power Factor (PF), power losses and energy quality from electrical installation. Therefore, Power Factor Correction (PFC), Electro-Magnetic Interference (EMI) and Total Harmonic Distortion in Current (THDi) are topics concern to users, distributors and generators of electrical energy. DC loads are characterized by damage energy quality due to rectification actions caused by its feeding source; nevertheless, with the arisen of power electronics technology, rectification can be done of controlled form by means of AC/DC converters, increasing at the same time PF of equipment. Converter main function consists on ensuring a constant voltage to the load; in addition, converter can be used to improve energy quality depending on its topology and control, emulating a resistive load for electrical grid; in this way, converters operate as filter between load and electrical grid for efficient energy management [1].

AC/DC Bridge Boost Converter (BBC) or boost PFC conventional topology has been widely used to feed DC loads due to its reduced components [2]. Converter operates as a current-controlled rectifier and it needs a robust control strategy to ensure both PFC and DC bus stabilization [2–4]. Control action of BBC is limited, converter only have one power switch [5] and rectifier bridge causes Electro-Magnetic Compatibility (EMC) issues [6]. In [7], it was proposed a control scheme for operating the converter with variable switching frequency. This control modifies switching frequency with two purposes: first, to reduce switching losses by decrease frequency around of current-signal peak; second, to reduce THDi by increase frequency during zero crossing of current. This control reduces THDi, nevertheless, current-waveform is not totally sinusoidal and THDi reduction does not comply with the international

normative IEC/EN 61000-3-2 and IEEE Std. 519 [8]. On the other hand, In [9], it was developed a filter in order to reduce EMI caused by the BBC operation, it is observed that designed filter is robust for low power applications. In general, operation of BBC needs a high control (non-linear) system together with a great filtering process for ensuring simultaneously electromagnetic compatibility, THDi reduction, PFC, bus DC regulation and fast response [10]; in addition, BBC produces high power losses when it is used in medium-high voltage applications and interleaved topologies for this applications also must be explored [3,4,11,12]. For these reasons, several modifications to conventional topology and new trends based on boost converter have been analyzed in this paper [13–19].

AC/DC Semi-Bridgeless Boost Converter (SBBC) topologies are characterized by replace the two diodes from rectifier bridge inferior level; these topologies can be used to reduce common mode noise and simplify the control system in comparison with other topologies [20,21]. SBBC topologies can be improve for EMC by adding elements (diodes, capacitors, inductors or switches) in symmetrical form for both lines phase and neutral.

Bridge-Less Boost Converter (BLBC) topologies are characterized by situate the converter elements in asymmetrical form in converter branches; these topologies can reduce reverse-recovery of diodes; nevertheless, asymmetry requires a high control strategy [22–24].

In [1,25], reviews about bridgeless and semi-bridgeless topologies based on boost converter are presented. An analysis of Electromagnetic Compatibility focus on differential and common mode noise for several topologies is done without considering interleaved topologies for medium and high voltage applications. These reviews are over 10 years old, in consequence, new trends in switch technologies, filtering and control present some solutions for reducing Electro-Magnetic Interference (EMI), noise and power losses for the topologies explored in these reviews.

This paper has sections as follow: 1) a description of conventional AC/DC converter topology based on boost converter is presented; 2) description of Semi-bridgeless boost converter topologies are analyzed; 3) bridgeless boost converter topologies are analyzed; finally, most relevant conclusions and selected topology to control are presented.

2. Conventional Boost PFC Topology

This section presents the basic topology of single-phase AC/DC converters with PFC based on DC/DC Boost converter. BBC converters have a complete rectifier bridge, therefore, All presented BBC topologies need a line EMI filter to comply with international normative [8] for reducing THDi.

2.1. Conventional AC/DC Boost Converter PFC Topology

Fig. 1 shown the conventional AC/DC BBC topology where feeding source is electrical grid and rectifier action is done by means of a diode bridge (D_1, D_2, D_3 and D_4). [1–4,13,14]; inductor L interchanges energy with capacitor C (DC bus), diode D avoids reverse currents and Load obtains a DC voltage from C. Generally, control is done with classical cascade PI control for DC bus stabilization by means of Pulse Width Modulation (PWM) signal applied to switch Q. Converter receives as feed a rectified sinusoidal signal and control takes as reference voltage signal from electrical grid in order to set in phase input voltage and current waves for PFC. In converter control designing, it is necessary to consider loss issues for medium and high voltage applications; gain and efficiency are reduced for duty cycles greater than 60% or 70% (depending on application) due to power and switching losses; then, control actions that require a great duty cycle can produce a contrary effect bringing converter to instability [11,26]. This PFC boost converter topology has direct connection with electrical grid, rectifier bridge and switching introduce harmonics and noise; then, an additional intermediate filtering equipment for Electro-Magnetic Interference (EMI) mitigation is necessary together with a robust control strategy [15,27,28].

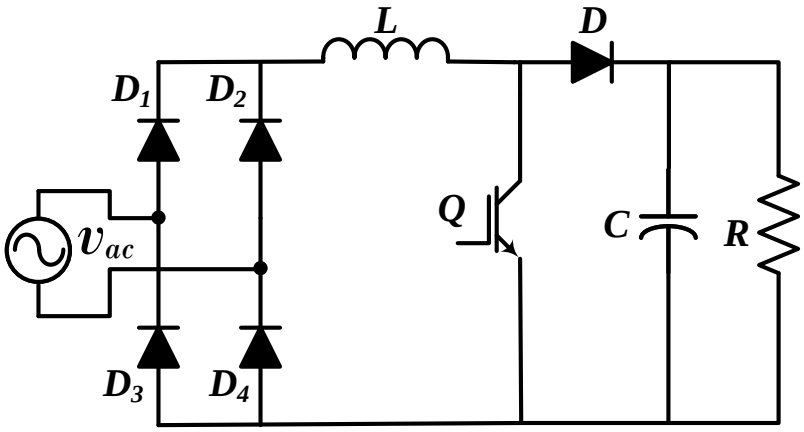

Figure 1. Conventional PFC topology.

2.2. Conventional Interleaved PFC Topology based on Boost Converter

Interleaved topology consists on several levels of boost converters connected to same rectifier bridge and DC bus. this topology reduce ripple in input current, additionally, distribution of currents implies a less sizing of converter elements due to thermal stress reduction. Interleaved topology adds a boost converter by each level depending on output voltage desired and it is necessary a split DC bus for medium voltage applications. This topology is not recommended for high voltage due to the fact that power losses and EMI issues are high, therefore, it is necessary robust filtering between electrical grid and converter combined with soft switching circuits for each level. Fig. 2 shows the interleaved BBC topology with two stages for industrial applications in low voltage [29]. This paper presents a detail procedure for calculating the converter elements including EMI filter taking into account PFC, voltage control, switching frequency and power losses. experimental results present efficiency major than 97% (high efficiency) and power factor up to 0.995 operating to nominal load. In conclusion, it is possible to obtain high efficiency and PF for this topology considering power losses since design.

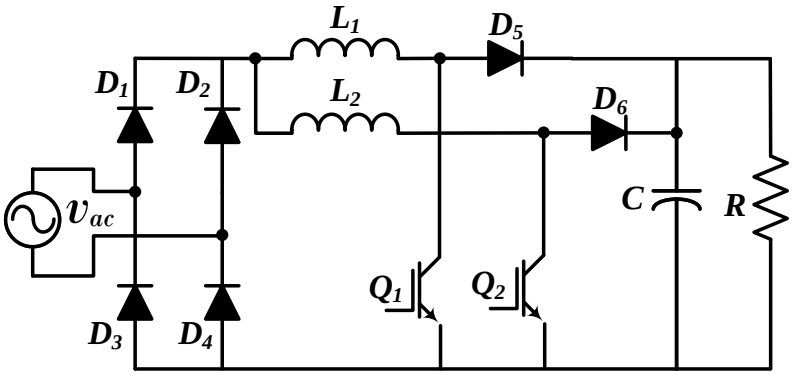

Figure 2. Interleaved PFC topology.

2.3. Conventional Hybrid Interleaved PFC Topology based on Boost Converter

In [12] a interleaved hybrid BBC topology with three levels is presented (Fig. 3). This topology can have efficiency major than 97% with cascade PI control. Also, compliance of THDi normative is reached with a line EMI filter. Distribution of currents reduce ripple in comparison with interleaved of two levels, so that, thermal stress in switches is minor; nevertheless, feature cost increases by the additional boost converter. Hybrid interleaved topology is recommended for medium voltage applications due to its low ripple and THDi in comparison with conventional BBC converter. Also, this topology of three levels is recommended in low voltage applications when it is necessary to feed high power loads.

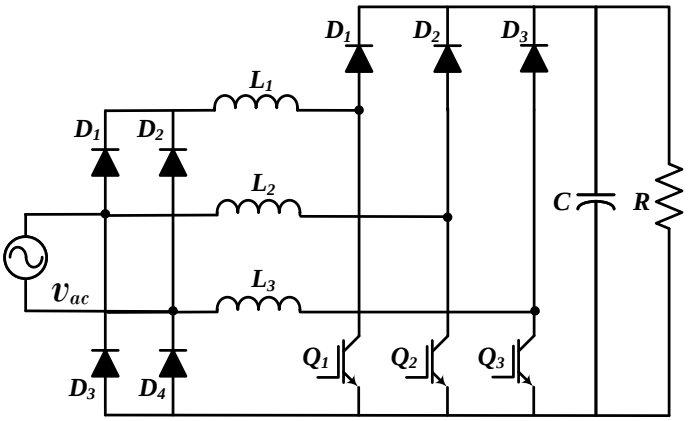

Figure 3. Hybrid Interleaved PFC topology.

2.4. Conventional PFC Topology with Bidirectional Switch

Fig. 4 shown Conventional PFC Topology with Bidirectional Switch [19,30]. This topology changes converter inductor L_1 and switching (Q_1 and Q_2) before rectifier bridge; also, $L_2 = L_1$ can be added in neutral line to mitigate thermal stress in L_1 and diodes D_1 and D_4 are fast-recovery diodes. This modification reduces common mode noise, nevertheless, a EMI filter also is necessary. A same control signal is used for both switches; it is noted that switches are inverted in order to avoid reverse currents when both are open, in consequence, both control signals must be isolated.

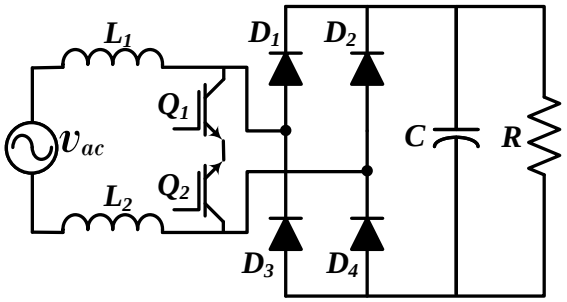

Figure 4. Conventional PFC Topology with Bidirectional Switch.

Several modifications has been proposed in order to improve behavior of BBC bidirectional topology [30,31]. Fig. 5a shown PFC Topology with Bidirectional and flexible switches. This converter adds two auxiliary switches (Q_3 and Q_4) and a split DC bus (C_1 and C_2). Auxiliary switches allow feeding the converter with two input voltage levels, both Q_3 and Q_4 are open o closed at same time depending on operating input voltage. Fig. 5b shows BBC PFC Interleaved Topology with Bidirectional switch. In this case, Q_1 and Q_2 from upper level operate in positive half-cycle and switches from lower level are open; in the same way, in negative half-cycle Q_1 and Q_2 from lower level are operating and switches from upper level are open. this action allows a better control in DC bus.

In conclusion, Bidirectional switch topologies only are recommended in low voltage and power applications. Additional switches increase implementation cost. Additional considerations as isolation and control design can be solved with not bidirectional BBC topologies with a EMI filter. In half and high power applications, bidirectional topologies present low efficiency because converter currents are not splitted in each half-cycle, increasing thermal stress and power losses; also, this increases differential mode noise.

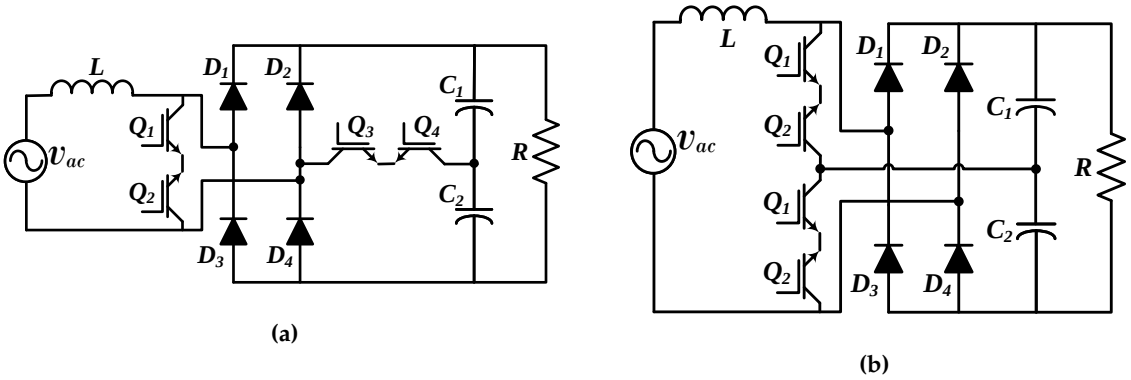

Figure 5. BBC converter with bidirectional switch: a) bidirectional and flexible switches, b) bidirectional and interleaved.

3. Semi-Bridgeless Boost Converter Topologies

SBBC topologies are based on conventional PFC topology (Fig. 1) replacing by switches the two diodes of rectifier bridge low level (half-bridge). Also, this change requires moving the inductor between electrical grid and half-bridge due to the fact that current control is done without complete rectification.

3.1. Conventional Semi-Bridgeless Boost Converter Topology

Fig. 6 presents the basic symmetrical topology or conventional SBBC topology [20,21]. This topology adds two switches (Q_1 and Q_2) instead D_3 and D_4, also removes the diode and switch used to coupling L with C. L is moved for coupling with electrical grid. This SBBC topology is characterized by using the same inductor for each semi-cycle of sinusoidal wave.

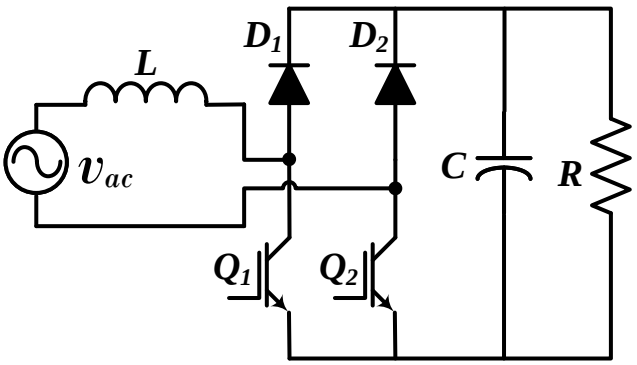

Figure 6. Semi-bridgeless boost converter topology.

SBBC conventional topology reduces power losses by conduction due to semiconductor reduction in the current path (current through of two semiconductors per cycle). Also, two switches allow an independent control for each semi-cycle of voltage sinusoidal signal from electrical grid [28,32].

Conventional SBBC topology has a low Common-Mode (CM) and Differential-Mode (DM) noise in comparison with conventional PFC topology with bridge. DM noise and thermal stress in L can be reduced adding an inductor to neutral conductor [16,33]. In this case, inductors operate in series in each semi cycle; in addition, CM noise also can be reduced if both inductors are coupled [34,35].

3.2. Conventional Semi-Bridgeless Boost Converter with Soft Switching

On the other hand, an additional circuit (snubber) formed by switch Q_3, inductor L_3 and capacitor C_1 can be used to reduce switching losses from SBBC (Fig. 7) [36]. In this case, the snubber circuit is focus on actuates Q_1 and Q_2 with zero voltage transition during their operation.

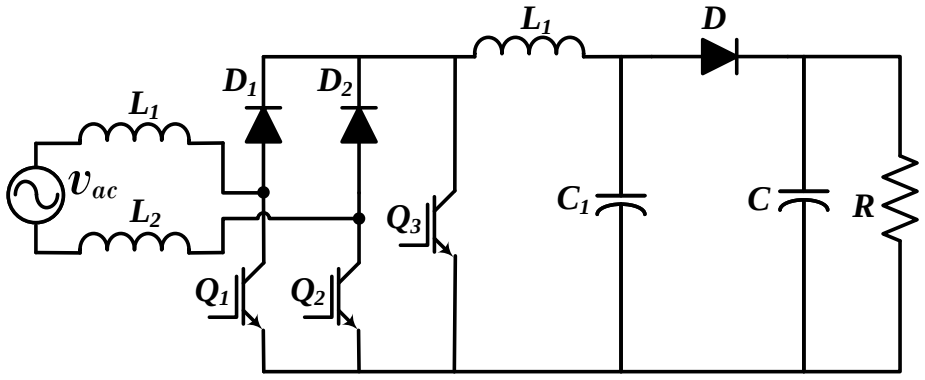

Figure 7. Semi-bridgeless boost converter with soft switching.

3.3. Semi-Bridgeless Boost Converter with Isolation

Fig. 8 shown a modification to SBBC conventional topology [37]. Modification consist on connecting a switch (Q_3) in series for isolate grid of DC bus and controlling input current when inductors are charging. This topology presents a reduction of leakage current to neutral form grid. Nevertheless, power losses are increase for adding other semi-conductor that actuates in discharge period; also, it is necessary an additional control action and a higher filter in comparison with SBBC conventional topology.

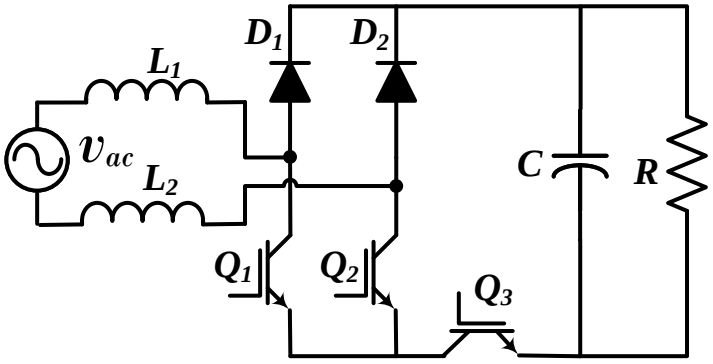

Figure 8. Semi-bridgeless boost converter with isolation.

3.4. Semi-Bridgeless Boost Converter with Clamped Diodes

Fig. 9 presents the topology for SBBC with Clamped Diodes or pseudo totem-pole SBBC topology. This topology adds two diodes (D_3 and D_4) to symmetrical topology. In consequence, it is obtained two boost converters, each one operating in each semi-cycle of sinusoidal wave [28,32,33,38–41].

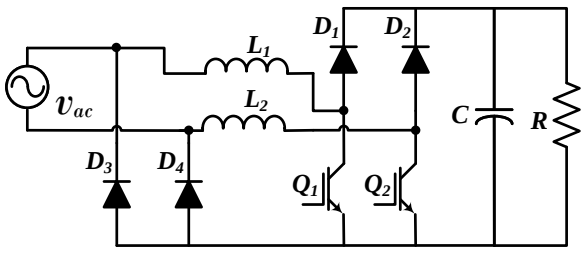

Figure 9. Semi-bridgeless boost converter with clamped diodes.

L_1, Q_1 and D_1 operate in positive semi-cycle; in the same way, L_2, Q_2 and D_2 operate in negative semi-cycle. control system is simplified because switches can be actuated with same control signal.

This topology reduces CM noise due to additional diodes which mitigates the coupling between ground and grid; nevertheless, DM noise and ripple is increased by operation of an only inductor in each semi-cycle. In comparison with conventional topology with rectifier bridge, it is obtain a reduction of input current ripple, DM and CM noise; therefore the input filtering can be reduced in this case [13]. [32] presents a cascade control system based on PID controllers, obtaining a power factor of 0.99 together a reduction of THDi up to 3.9%; this implies a significant energy quality improvement if the SBBC control system also is focus on harmonic mitigation. Additionally, CM noise also can be reduced if coupling inductors are used [42] and switching losses are reduced if an snubber circuit is added [43,44].

3.5. Semi-Bridgeless Boost Converter with Clamped Switches

Fig. 10 presents SBBC hybrid clamped topology or SBBC with active virtual ground [45]. This topology adds a capacitor C_1 two clamped switches (Q_3 and Q_4) instead diodes. Main advantage of this topology consists on actuate all switches in order to do two third order LCL filters (with L_1, L_2 and C_1) between SBBC and electrical grid, depending on semi-cycle of voltage sinusoidal wave; this control reduces DM noise and this topology needs a less robustness EMI filters than SBBC with clamped diodes; C_1 reduces CM noise, but it increases conduction losses by adding other passive element and it is recommen needs better control system (non-linear) [46].

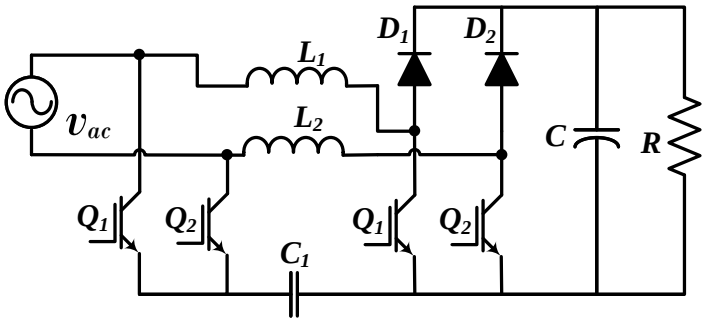

Figure 10. Semi-bridgeless boost converter with clamped switches.

3.6. Semi-Bridgeless Boost Converter with Clamped Diodes and Switches

Fig. 11 presents a high efficiency SBBC based on clamped topology with diodes [47]. This topology adds two switches (Q_3 and Q_4) in series connection to basic topology with clamped diodes such that each boost converter operates with two switches. Conduction loss through return path are decreased and additional switches reduce CM noise; nevertheless, increase of semi-conductors not causes an increase of power losses in comparison with topology with only clamped switches; clamped diodes (D_3 and D_4) only actuates for the pre-charge of DC bus and this diodes are excluded of current path in normal operation conditions or steady state.

3.7. Semi-Bridgeless Boost Converter with Clamped Capacitors

This topology (Fig. 12) has two clamped capacitors (C_1 and C_2) instead diodes or switches [48]. Capacitors actuate as first order filter with low impedance in each semi-cycle and reduces CM noise for high frequency. However, ripple in inductors is approximately double in comparison with topology with clamped diodes; in same way, efficiency is lower than SBBC with clamped diodes and switches. In this case, is very important clamped capacitors with same values (minimal difference between both values), otherwise, CM noise can increase and control system must be designed independently for each switch.

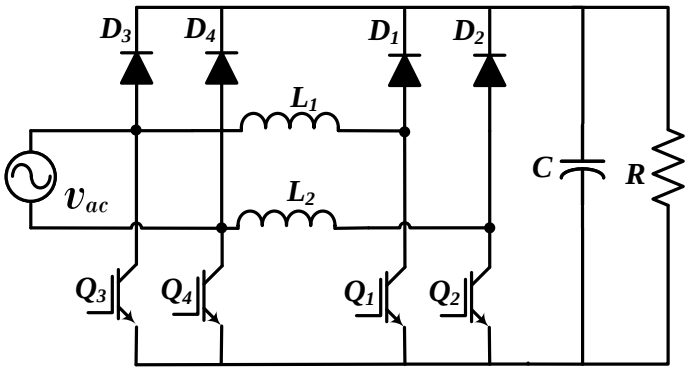

Figure 11. Semi-bridgeless boost converter with clamped diodes and switches.

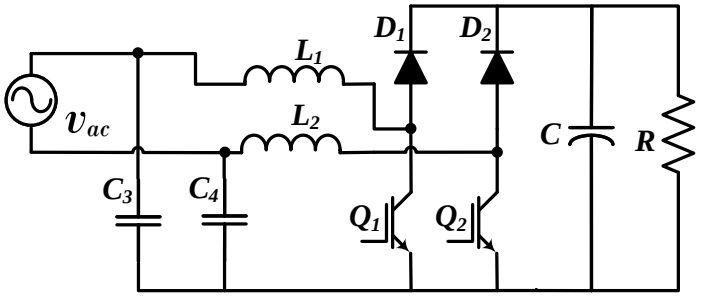

Figure 12. Semi-bridgeless boost converter with clamped capacitors.

3.8. Semi-Bridgeless Boost Converter with Clamped Capacitors and Coupling Inductors

Fig. 13 shown a variation of topology with clamped capacitor [49]. This topology adds two coupled choke inductors (L_3) in converter input in addition to l_1 and L_2 for CM noise reduction. In this case, capacitors also are used to reduce the magnetization current from L_3. Choke inductors present high impedance in its terminals and clamped capacitors present low impedance, these conditions allow a wide range for CM noise reduction.

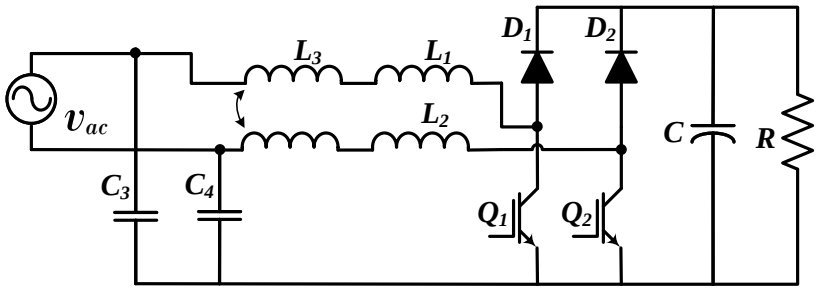

Figure 13. Semi-bridgeless boost converter with clamped capacitors and coupling inductors.

3.9. Semi-Bridgeless Boost Converter with Zero Voltage Transition

Fig. 14 presents the SBBC topology with zero voltage transition [50]. This topology adds an additional switch (Q_3) to SBBC topology with clampled diodes. Q_3 main function consists on control the snubber circuit composed by diodes D_5, D_6, D_7 and D_8, inductor L_3 and capacitor C_1. Snubber circuit provides a soft switching for Q_1, Q_2 and Q_3 in order to reduce swiching losses and reverse recovery losses from D_1 and D_2. Finally, other topologies with snubber circuit for SBBC soft switching are presented in [51–53] in order to reduce power losses due to power switches.

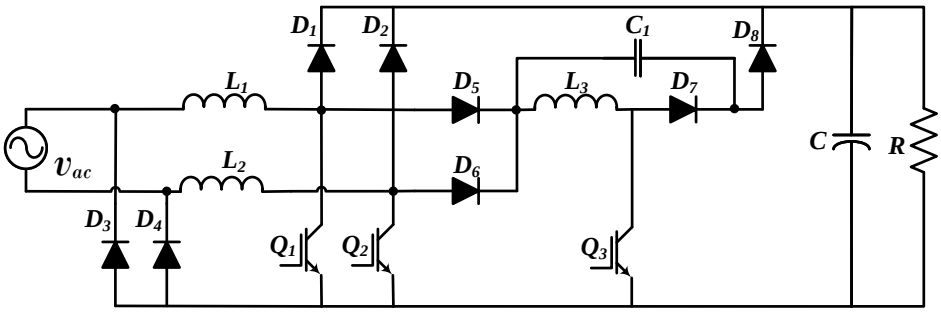

Figure 14. Semi-bridgeless boost converter with Zero voltage transition.

4. Bridgeless Boost Converter Topologies

This section presents the topologies for BBC characterized by situate different or asymmetrically switches and diodes of converter branches.

4.1. Conventional Bridgeless Boost Converter Topology

Fig. 15 presents the asymmetrical or basic totem-pole topology of bridgeless boost converter [22–24]. This topology situates switches (Q_1 and Q_2) in first branch of converter and diodes (D_1 and D_2) in the second branch.

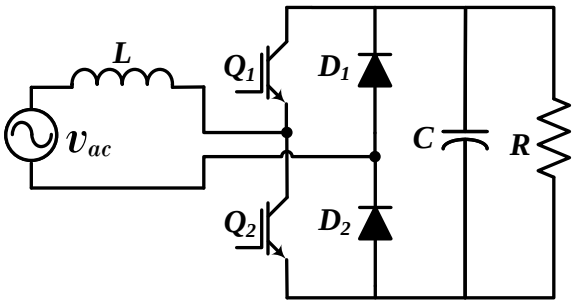

Figure 15. Bridgeless boost converter, totem pole topology.

Totem-pole topology only operates with a switch and diode in each semi-cycle of electrical grid. In positive semi-cycle, Q_2 is open, DC side is connected with neutral line from electrical grid by means of D_2 and Q_1 actuates for controlling. In negative semi-cycle, Q_1 is open, DC side is connected with positive line from electrical grid by D_1 and Q_2 actuates in this semi-cycle.

Totem-pole topology cans operate in boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) [54], reducing reverse-recovery of diodes. Boundary operation causes a variable and aleatory ripple, requiring a additional considerations in control strategy as operation limits; Also, hard switching causes high power losses that can be reduce with a circuit of soft switching [55–58].

4.2. Bridgeless Boost Converter, Pseudo Totem-Pole Topology

Fig. 16 presents the BBC topology built with two AC/DC boost converters called pseudo totem-pole topology [59,60]. In positive semi-cycle, first boost converter actuates due to polarization of D_4, it is formed by L_1, Q_1 and D_1. In negative semi-cycle, second boost converter actuates due to polarization of D_3, it is formed by L_2, Q_2 and D_2. This configuration requires different control signal for both switches and Q_1 requires gate drivers for different reference control signal [18]. Pseudo totem-pole topology needs coupling inductors for CM noise reduction, auxiliary circuit for soft switching its correct behavior [61,62]; therefore, this topology is not commonly used.

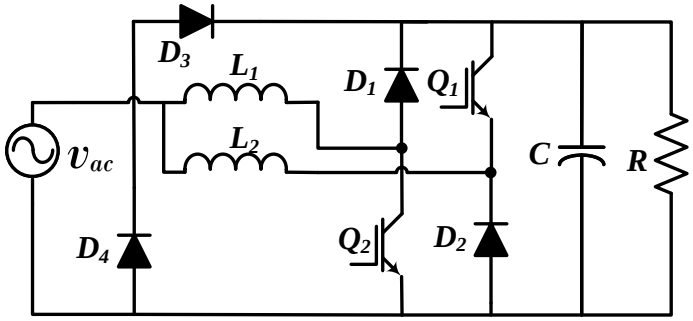

Figure 16. Bridgeless boost converter pseudo totem-pole topology.

Table 1 presents a summary about topologies explored in this paper. Several topologies presents low THDi, high power factor and high efficiency by using non-linear control instead classical PI control. power factor of 0.99 is reached for each topology with linear control, then, challenges are focus on reduce THDi and increase efficiency. All topologies need a line EMI filter, however, SBBC topologies need a filter less than other topologies due to reduction of CM noise obtained by its symmetry in construction. Efficiency increases by using multiple paths for currents, switching losses are reducing by soft switching circuits; nevertheless, in topologies without symmetry must be consider an additional isolation for switching circuits.

Table 1. Add caption

Converter	Topology			Control		PFC > 0.99	THDi < 5%	n > 0.97
	BBC	SBBC	BLBC	Linear	Non-linear			
Conventional	X			X		X	X	X
Interleaved	X			X		X	X	X
Bidirectional	X			X		X		
Conventional		X		X		X		X
Soft switching		X		X		X	X	X
Isolation		X		X		X	X	
Clamped diodes		X		X	X	X	X	X
Clamped switches		X			X	X	X	
Clamped diodes and switches		X			X	X	X	X
Clamped capacitors		X		X		X	X	X
Clamped capacitors and inductors		X		X		X	X	X
Zero voltage transition		X			X	X	X	X
Conventional			X	X		X		X
Pseudo totem-pole			X	X		X		X

5. Conclusions

In this paper, a review about SBBC and BBC topologies for PFC was done; Basic operation, advantages and disadvantages were analyzed. SBBC topologies present better performance than BBC and BLBC topologies concern to control and electromagnetic compatibility. Then, the topology selected to control with sliding mode control is "semi-bridgeless boost converter with clamped diodes". This topology presents low CM and DM noise, also power switches can be actuated with the same control

signal. Also, review about this topology shows THDi according to international normative "IEEE Std. 519 and IEC/EN 61000-3-2" with classical linear controller.

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Development of a Distribution Static Compensator D-STATCOM: Prototype that will favor the development of devices based on power electronics

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***Abstract*—This paper describes the implementation of a distribution static power compensator (D-STATCOM) for reactive compensation in power grids, being presented as a platform for future developments of our research group GIMEL for improving quality power. In general terms, the development puts us at the forefront in the development of power electronic devices. A three-phase inverter of six pulses with two levels was developed. Hardware implementation of different stages (sensors, power switching, passive elements, and processor) is fully described. Firmware that allows D-STATCOM operation was implemented on a TMS3202F DSP (Texas Instruments) using a modular approach. Correct operation of the D-STATCOM prototype was verified with experimental results.**

***Index Terms*— Development of prototypes, D-STATCOM, reactive power compensation, FACT's, power electronics.**

I. Introduction

Reactive energy is mainly associate with the operation of electric devices such as transformers in power systems and motors in industrial applications [1]. Reactive energy is a bi-directional interchange between the load and the source in power systems causing power losses, reduction in the effective network capacity and deterioration of power quality [2]. Most of countries have regulation that penalizes the excessive use of reactive consumption due to the over cost that causes in distribution and transmission networks and also in generators [3], [4]. Reactive energy must be compensated regulating its circulation in the power system to the permissive limits.

An alternative to reactive power compensation is the use of capacitor banks. Capacitor banks are devices that are composed of switching capacitors. Compensation by means switching capacitors is made in a discrete way being useful in networks with variable loads. The continuous change in the topologies of the load and the power network could cause resonance problems when capacitor banks are installed, implying the mal-functioning of the power network due to the presence of over voltages and currents [5]. These problems can be solved by the using of controlled power electronics devices, if stability is guaranteed through the controller [6], [7], [8].

D-STATCOM is a promissory power electronic device to dynamic reactive power compensation and also compensation of harmonics and umbalances currents in power networks. It is connected in parallel with the load and can operate in a continuous way, reaching a power factor near to the unity and avoiding operative problems. The most commonly topologies for D-STATCOM are multi-pulse and multi-level [7], [9]. Multi-level topology has more than six switches, each branch has three or more switches depending of the voltage level, which mean a complex control and higher cost [10]–[15]. Meanwhile, multi-pulse topology has six switches [16], two switches by branch. This topology has the minimum switches for a three-phase inverter [7], [8], [17]. Due to its lower cost and simplicity in the control, multi-pulse topology was chosen in this research.

This paper has as a purpose the description of the implementation of a D-STATCOM. Hardware implementation is described, including design details in Printed Circuit Boards (PCB). PCB of sensors, power switching, passive elements, and processor are fully described. Also, Firmware that allows D-STATCOM operation was described. TMS3202F DSP (Texas Instruments) is shown using a modular approach.

This paper is structured as follows: II) fundaments of reactive compensation and D-STATCOM operation are described; III) D-STATCOM hardware development is presented; IV) Firmware modules are described, V) results are presented, showing D-STATCOM operation VI) finally, most relevant conclusions are included.

II. D-STATCOM Operation

Reactive power is an oscillating energy that bi-directionally flows between electrical grids and loads; however, many loads as motors need reactive power in their operation; D-STATCOM can provide this reactive power improving energy quality of the power network. Fig. 1 shows the reactive energy

compensation by means of D-STATCOM with three elements: network, load and D-STATCOM. All elements are in parallel, having the same voltage (grid voltage v_G); i_G, i_L, i_D are grid, load and D-STATCOM currents respectively.

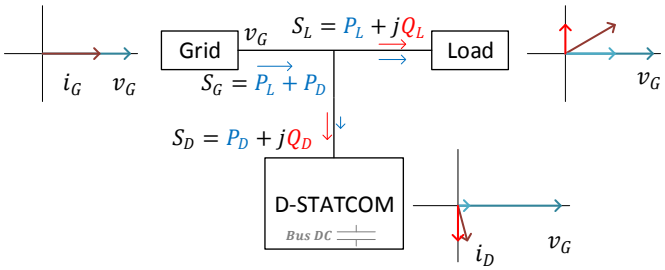

Fig. 1. D-STATCOM operation.

Using v_G as the reference in the horizontal axis, phasor diagrams are presented for each element in Fig. 1. Current i_L has a phase angle respect to v_G, thus can be decomposed into a horizontal (direct) projection (associated to load active power P_L) and a vertical (quadrature) projection (associated with load reactive power Q_L). During D-STATCOM operation, the quadrature component of i_D is controlled in order to be equal to the quadrature component of i_L with opposite sign. In this way, the grid current i_G has no quadrature component and thus no reactive power is interchanged with the grid.

In Fig. 1, D-STATCOM apparent power S_D is represented as the sum of an active power P_D and a reactive power Q_D. P_D corresponds to the power consumed by D-STATCOM (including power losses) necessary for its operation. Q_D is used to compensate Q_L. Notice that, grid apparent power (S_G) is equal to P_L plus P_D i.e. the grid only provides active power when D-STATCOM is in operation.

III. Hardware Description

Fig. 2 shows D-STATCOM scheme and complementary elements for its operation. Fig. 2a presents D-STATCOM converter topology (two levels and six pulses) [7], [9]; while Fig. 2b shows additional electronic modules in charge of measurement and converter control.

D-STATCOM main component is the three-phase inverter (Voltage Source Converter, VSC), in charge of power flow regulation between AC grid and DC-bus (Fig. 2b). Inverter consists of six insulated gate bipolar transistors (IGBTs) and is controlled by means of six switching signals: M^a, M^b, M^c for the upper transistors and $M^{a\prime}$, $M^{b\prime}$, $M^{c\prime}$ for lower transistors.

DC-bus is composed of capacitors C_1 and C_2 that are used to energy storing and guarantee a constant DC voltage for three phase inverter operation. Two stabilization resistors, in parallel with each capacitor, are used to minimize capacitor voltage unbalances due to neutral currents [18]. Also, to limit start-up currents when DC-bus is discharged, a pre-charge circuit was added between inverter and bus [17]. The pre-charge circuit consists of a series resistor that is short-circuited once the DC-bus has reached a pre-set voltage.

Three-phase grid connection is achieved by using a set of coupling inductances (L_a, L_b and L_c). Coupling inductances function is to filter high frequency components of output D-STATCOM currents (i_D^a ,i_D^b, i_D^c). Also, for safety and practical reasons, series connection contactors (C_e) are used to D-STATCOM disconnection.

The following sensors were implemented. Current sensors were used to measure D-STATCOM output currents (i_D^a ,i_D^b, i_D^c that are resumed as the vector i_D^{abc}) and load currents (i_L^a ,i_L^b, i_L^c that are resumed as the vector i_L^{abc}). Voltage sensors measure DC-bus voltage (v_{DC}) and three-phase grid voltages (v_G^{abc}). Sensor implementation and signal conditioning where implemented in the Current and Voltage Measurement PCBs (Fig. 2b.).

Sampling, calculations, control algorithms, control signal generation (M^{abc} and $M^{abc\prime}$) and communications are carried out by a microcontroller. Microcontroller PCB (Fig. 2b.) contains all the associated necessary circuitry for the correct microcontroller operation.

Table I summarizes the main specifications for the developed D-STATCOM. Next subsections describe in more depth the implementation of the different hardware blocks.

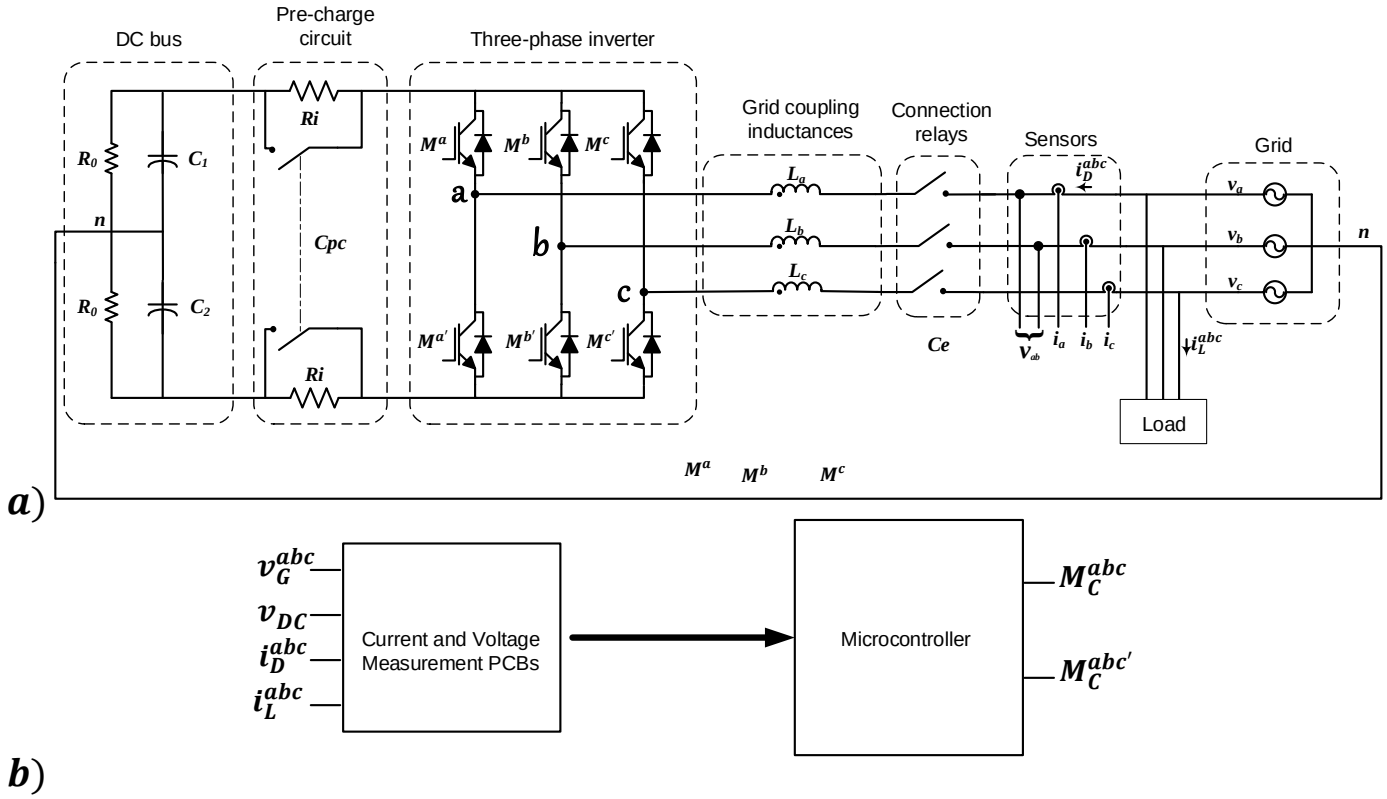

Fig. 2. D-STATCOM scheme and PCBs.

TABLE I
D-STATCOM CHARACTERISTICS

Characteristic	Value
Power	337.611 VA
Voltage	44 Vrms (transformer coupled to 220V grid)
Current	4.43 Arms
DC bus Voltage	283 Vdc
Coupling inductances	14 mH
Capacitors	2200 uF
Power factor correction	Inductive and capacitive

A. PCB for VSC

Fig. 3 presents the PCB implemented for the VSC and gate drivers. This PCB has three main stages: 1) VSC implementation, 2) Bootstrap capacitor implementation and 3) optocouplers implementation.

First stage, VSC implementation: The VSC was built with an Integrated Power Hybrid IC with internal shunt Resistor (IRAM136-3063B); this module has six power switches (IGBT) with anti-parallel diodes. Maximum operation current is 15 Amp (100°C) while collector-emitter voltage is up to 600 Volts. Module includes gate-drivers for appropriated IGBT switching, allowing its control by means of 5V digital signals.

Second stage, Bootstrap capacitor implementation: Bootstrap capacitors are used to adequate the voltage signal for upper switches of VSC.

Third stage, optocouplers implementation: six optocouplers were used for isolation between the control system (microcontroller) and the VSC.

Finally, this PCB has a common connector for switching signals generated from the microcontroller (M_C^{abc}, $M_C^{abc\prime}$), terminals for bus DC connection and terminals for VSC output.

To guarantee safety, durability and scalability, this PCB was designed taking into account the recommendations from IPC standard 2152 [19] for route sizing respect to maximum current and IPC standard 2221 [20] and for clearance respect to maximum voltage. These recommendations were also applied to the rest of PCBs developed.

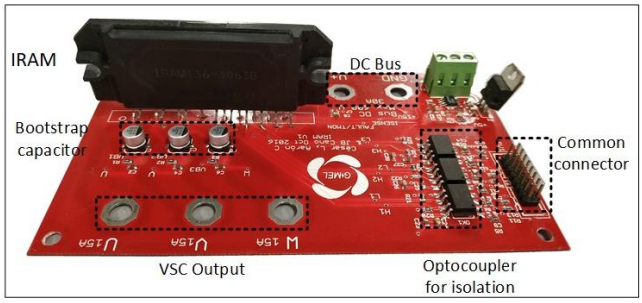

Fig. 3. PCB IRAM136-3063B and Gate Drivers.

B. Current and Voltage Measurement PCBs

Voltage measurement (v_{DC}, v_G^{abc}) and current measurement (i_D^{abc}, i_L^{abc}) were implemented in independent PCBs. Fig. 4 presents the voltage measurement PCB. This PCB is based on the AMC1200 isolation amplifier, allowing measurements up to 1000 Volts. AMC1200 is powered trough an isolated DC-DC power source. AMC1200 output is filtered through an active analog filter using the Sallen-Key topology. Analog signals from this PCB are in the range from 0 to 3.5V and are

carried out to the microcontroller PCB through a common connector.

Voltage PCB can measure up to four different signals, thus a single card is enough for D-STATCOM requirements (v_{DC}, v_G^{abc})

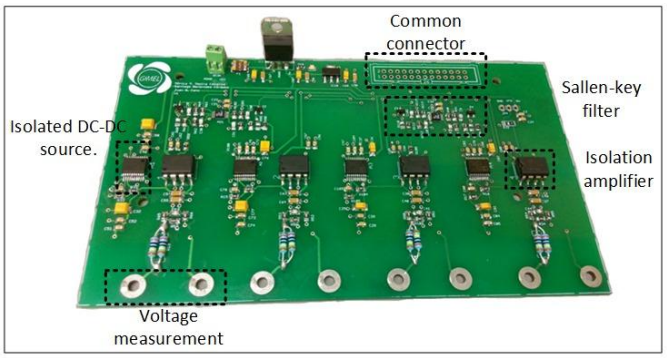

Fig. 4. Voltage measurement PCB.

Fig. 5 presents the current measurement PCB. This PCB has three current inputs and is based on the ACS174 hall effect sensor. ACS174 provides an isolated voltage output proportional to the sensed current, in the range from 0-5V. Signal conditioning is completed by a Sallen-Key filtering and attenuation to 0-3.5V range. Two PCBs are used, first for D-STATCOM currents measurement (i_D^{abc}) and second for load currents measurement (i_L^{abc}).

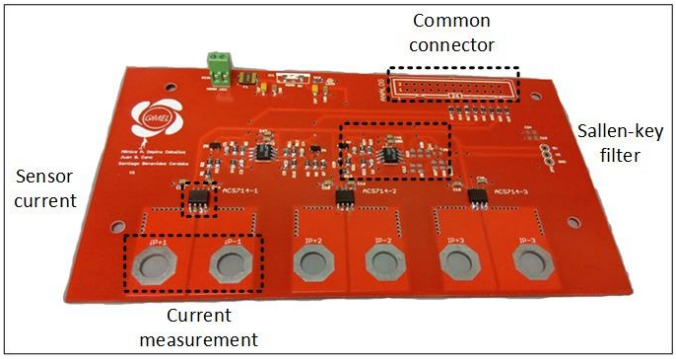

Fig. 5. Current measurement PCB.

C. Passive elements

DC-Bus and coupling inductors define limits for D-STATCOM compensation and this sub-section presents their sizing.

Coupling inductor sizing: inductor designing is done based on current signal geometry according [21], [22]. Equation 1 presents the inductor value L, where Δi_L is the current ripple, f_{sw} is switching frequency and n depends on numbers of the inverter levels. In this way, the select coupling inductance for each phase is $L = 14\ mH$ (Fig. 6) in order to filter the current signal given by the IGBT module (Grid coupling inductances in Fig. 2).

$$L = \frac{1}{n} \cdot \frac{v_{DC}}{\Delta i_L \cdot f_{sw}} \quad (1)$$

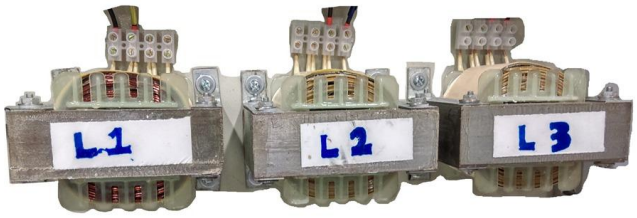

Fig. 6. Inductors for grid coupling.

DC bus sizing: capacitance value is defined by means of equation 2 from [21], [23]. Where $v_{out-peak}$ is the output voltage peak, i_{n-peak} is the neutral current peak, f_G is the grid frequency and Δv_c is the voltage ripple. In this case, D-STATCOM has 4 capacitors (split DC-Bus) of $2200\ \mu f$ (commercial value). In addition, 2 resistances of 30 kΩ are used to regulate the DC-Bus charge (pre-charge circuit in Fig. 2).

$$C = \frac{v_{out-peak} \cdot i_{n-peak}}{4\pi \cdot f_G \cdot v_{DC} \cdot \Delta v_c} \quad (2)$$

D. Microcontroller

D-STATCOM is a power electronics device that needs data measurement, serial communication, PI (Proportional Integral) controller and high-speed processing. Therefore, a microcontroller with DSP is necessary, in this case, D-STATCOM controller was developed using a microcontroller TMS320F28335 (specialized in power electronics [24], [25]). Fig. 7 presents the PCB designed and implemented for the microcontroller. This PCB has 4 main stages:

First stage, microcontroller: this is a microcontroller DSP TMS320F28335 manufacturer by Texas Instruments. TMS320F family is focus on power electronics applications.

Second stage, common PWM terminals: these terminals are used to control the VSC.

Third stage, Common measurement terminals: these terminals are used to receive measures from sensor PCBs.

Fourth stage, Serial Communication: these terminals are used to do an interface between microcontroller and users by means of USB port (SCI-USB).

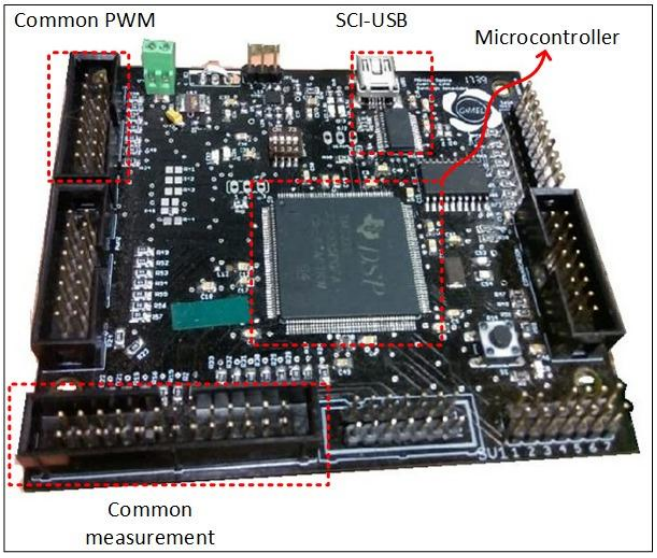

Fig. 7. PCB for microcontroller TMS320F28335.

IV. Firmware Description

This section describes the firmware that was implemented in the DSP TMS320F28335. TMS320F family manufacturer (Texas Instruments) provides specialized libraries in motor control [26], frequency analysis response [27] and photo-voltaic solar energy [28]. Also, the supplier provides detailed libraries with explanation of microcontroller peripheral programing for controlling power switches [29].

Math operations in a control system imply complex processing operations, which must be executed in a period of time shorter than the sampling period of the system. For this reason, it is convenient a microcontroller with floating-point (programmed for DSP) and fixed-point libraries in order to execute faster numeric calculations.

The DSP has an Arithmetic Logic Unit (ALU) module that is used to support the processor with complex math operations. Fixed-point libraries are codes to perform high speed math operations. Table II shows some functions for math operations of TMS320F family.

TABLE II
Functions of Fixed-Point and Floating-Point Libraries

Functions	Fixed-point	Floating-point
Complex FFT	6	1
Real FFT	8	2
Inverse Fourier Transform	1	0
Vector operations	7	0
Statics using vector	3	0
Infinite Impulse Response (IIR)	0	2
Design filter examples	0	4

Fig. 8 shows main functions that TMS320F28335 executes for D-STATCOM operation. Voltages and currents digitalization is accomplished by using the ADC (Analog to Digital Converter) peripheral. Activation of the VSC IGBTS is accomplished using the PWM (Pulse Width Modulation) peripheral [30]. SCI (Serial Communications Interface) peripheral is used for communications while GPIO (General Purpose Input Output) peripheral is used for contactors activation (grid connection and pre-charge circuit).

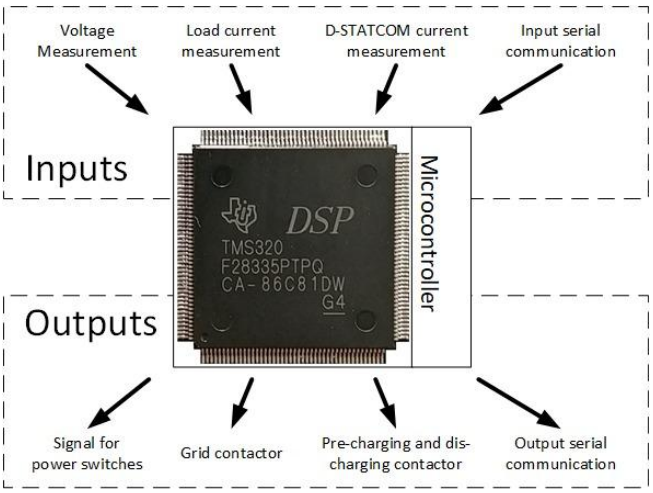

Fig. 8. Peripheral used in D-STATCOM development.

In order to control microcontroller peripherals, a set of firmware modules were developed. These modules are shown in Fig. 9 and are described in the next subsections.

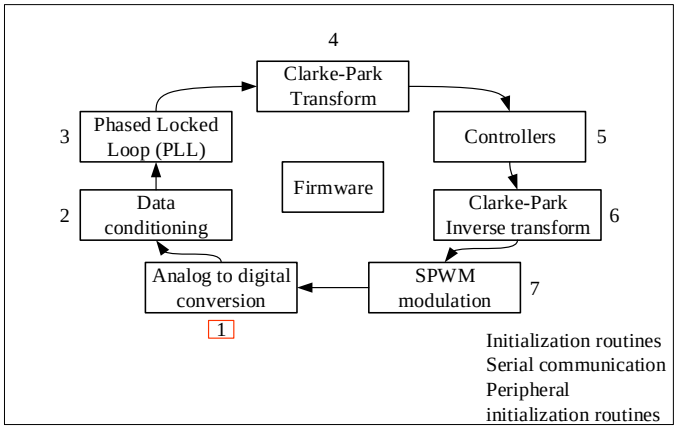

Fig. 9. D-STATCOM operation routines.

A. Analog to digital conversion and data conditioning

Control process initiates by measuring all voltage and current signals of the system (i_D^{abc}, i_L^{abc},v_{DC}, v_G^{abc}). TMS320F ADC was used. ADC resolution is 12 bits and sampling frequency is 20 kHz. Data conditioning consists of ADC data scaling, that permits to convert binary data to engineering units through an offset correction and a gain factor.

B. Phase-Locked Loop (PLL)

A phase-locked is a control system which permits the generation of signal whose output is related to the phase of an input signal. For power electronic devices, PLL is used to synchronize the voltages and currents of the system with a reference. In this case, the signal which is the reference of the system is the grid voltage of phase a (v_G^a). PLL was implemented using the library C28x Solar library [20], PLL algorithm is updated at every ADC sampling.

C. Clarke-Park transform

Clarke-Park transform changes three-phase AC signals into DC signals referenced to a rotational frame (dq0 frame) [31], [32]. It allows the representation of all phase currents in its direct and quadrature components using as reference the voltage v_G^a. This transform gives information about active power related to the direct current component and also reactive power related to the direct current component. Clarke-Park transform is performed by a sequence of instantaneous matrix operations that is performed at the same ADC sampling frequency. This transform comes from solar library [28] and uses the voltage and current data sampled from ADC and the phase angle determined by PLL. Using this transformation, D-STATCOM currents in dq0 frame (i_D^{dq0}) are obtained from i_D^{abc}, and load currents in dq0 frame (i_L^{dq0}) are obtained from i_L^{abc}.

D. D-STATCOM Controllers

D-STATCOM controllers generate control signals for IGBT power module. Cascade control and closed loop control are used to compensate reactive power. Fig. 10 shows D-STATCOM control schemes: Fig. 10a presents the DC voltage control loop and Fig. 10b presents reactive current control loop.

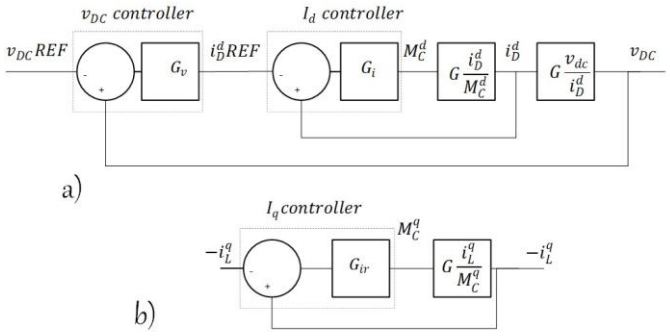

Fig. 10. D-STATCOM controller system.

DC voltage is controlled by absorbing or delivering active power from the grid (Fig. 10a). The input to the v_{DC} controller (G_v) is the error signal between the set point ($v_{DC}REF$) and sensed v_{DC}, and its output is the direct current component set point (i_D^dREF). In this way, G_v controller determines the amount of i_D^d (that is related to active power) required to keep v_{DC} at its desired level. Direct current controller (G_i) function is to keep the i_D^d value fixed at the level i_D^dREF by modifying the direct modulation output (M_C^d) that defines IGBT switching. Blocks $Gi_D^d/M^d$and Gv_{dc}/i_D^d represents the transfer functions for D-STATCOM model [18].

Fig. 10b presents reactive current control loop. Notice that, in this case, a voltage controller is not necessary. This is due to the oscillating nature of reactive power, which does not affect v_{DC} average value but affects its ripple. The set point for the closed loop controller (G_{ir}) is the negative value of the load quadrature current ($-i_L^q$). In this way, this controller guarantees that the D-STATCOM system behaves as a controlled current source, that is always equal to the reactive current of the load. The output from this controller is the quadrature modulation (M_C^q) that defines IGBT switching.

All controllers uses PI (proportional integrative) control law and were implemented using Texas instruments libraries and tuned using the methods described in [17] . Sampling rate for current controllers (G_i , G_{ir}) is 4KHz, and for DC voltage controller (G_v) is 800Hz.

E. Inverse Clarke-Park transformation

Controller outputs (M_C^d and M_C^q) are related to dq0 frame. M_C^{dq} must be converted to time domain using inverse Clarke-Park transformation. Inverse Clarke-Park transformation provides three sinusoidal signals (M_C^{abc}) with a difference of 120° between phases which will be used as reference in the SPWM modulation. For inverse transformation, it is assumed that $M_C^0 = 0$, implying that the D-STATCOM output currents are balanced.

F. SPWM modulation

SPWM (Senoidal Pulse Width Modulation) generates switching signals for the IGBT modules that are based on the results from inverse clarke-park transformation. SPWM modulation is carried out by using the microcontroller enhanced Pulse Width Modulation (ePWM) peripheral.

Fig. 11 shows bipolar modulation for an arbitrary phase. Modulation consists in the comparison between a sinusoidal signal (reference signal) and a triangular signal (carrier signal). In this implementation, the reference signal is M_C^{abz} while the triangular signal is generated by a digital counter in the ePWM peripheral.

Reference and Carrier signals are continuously compared. Every time that the reference signal is higher than the carrier signal, the upper IGBT is activated and the lower IGBT is deactivated. Instead, when reference signal is lower than carrier signal, the upper IGBT for that phase is deactivated and the lower IGBT is activated. Notice that this process is executed for the three phases, providing the six switching signals of Fig. 2a (M^{abc} for upper IGBT and $M^{abc\prime}$for lower IGBT).

Also, ePWM peripheral provides dead time functionalities, which avoid VSC destruction due to simultaneous activation of upper and lower IGBTs of the same phase.

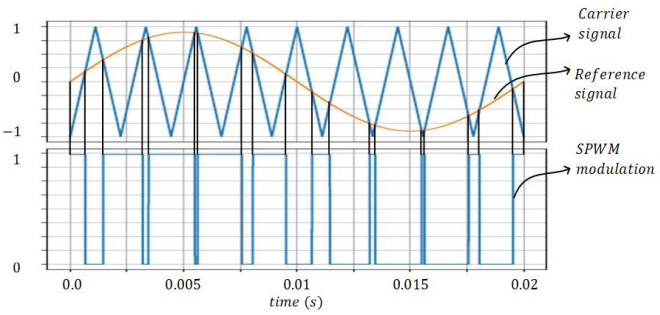

Fig. 11. Bipolar SPWM modulation.

G. Initialization routine

After a power on condition, and before system operation, a series of initialization steps must be carried on in order to

guarantee a proper initial condition for controllers and a safe start operation.

Fig. 12 shows the algorithm for D-STATCOM initialization: 1) Initial conditions: Initially, grid connection contactor is opened while microcontroller initializes all its peripherals. 2) DC bus discharge: Microcontroller verifies that the DC bus is discharged before initiating operation. 3) Delay for DC level measurement: During a given period, measurements of all sensors (current and voltage) are captured for offset compensation. 4) Grid connection: Grid contactor is closed. 5) Capacitor pre-charging routine: DC voltage starts to increase, but DC-bus current is limited by the two pre-charging resistors, once voltage reaches a given threshold, pre-charging resistors are short-circuited using pre-charging contactors. 6) Controllers initialization: Control loop described in previous sections is started.

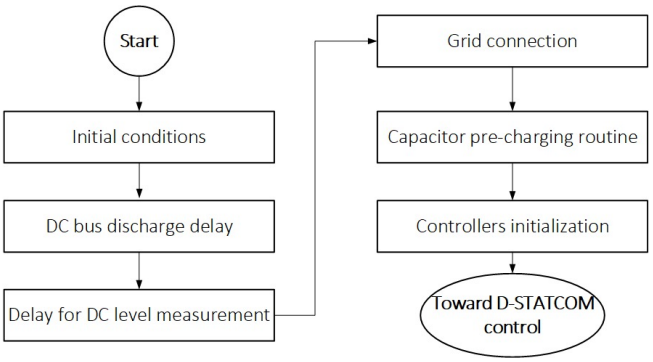

Fig. 12. Initialization algorithm

H. *Serial communications.*

This firmware module controls the SCI peripheral which using a FTDI232 interface provides USB communication for the D-STATCOM. This module consists of a finite state machine that receives request of information from user and responds sending data.

Part of microcontroller's memory is reserved for saving data of load currents (i_L^{abc}), D-STATCOM current (i_D^{abc}), grid voltage (v_g^{abc}), dq0 transformations (i_L^{dq0}, i_D^{dq0}), control variables (M_C^{dq}). Memory contents are serially transferred under user request. This mechanism helps to diagnose system operation and was used to obtain some of the results for the next section.

V. Results

In this section, main results obtained from D-STACOM prototype are presented. Subsections present results for selected individual modules and finally D-STATCOM operation is shown.

Fig. 13 shows the implemented D-STATCOM and its main components: 1) Coupling contactor for grid connection, breakers and fuses for protection of PCBs and voltage sources. 2) Voltage measurement PCB. 3) microcontroller PCB. 4) Current measurement PCB. 5) Pre-charge contactor. 6) Pre-charge resistances. 7) PCB of VSC IRAM136-3063B. 8) Relays for actioning contactors. 9) DC bus capacitors. 10) Inductors for grid coupling.

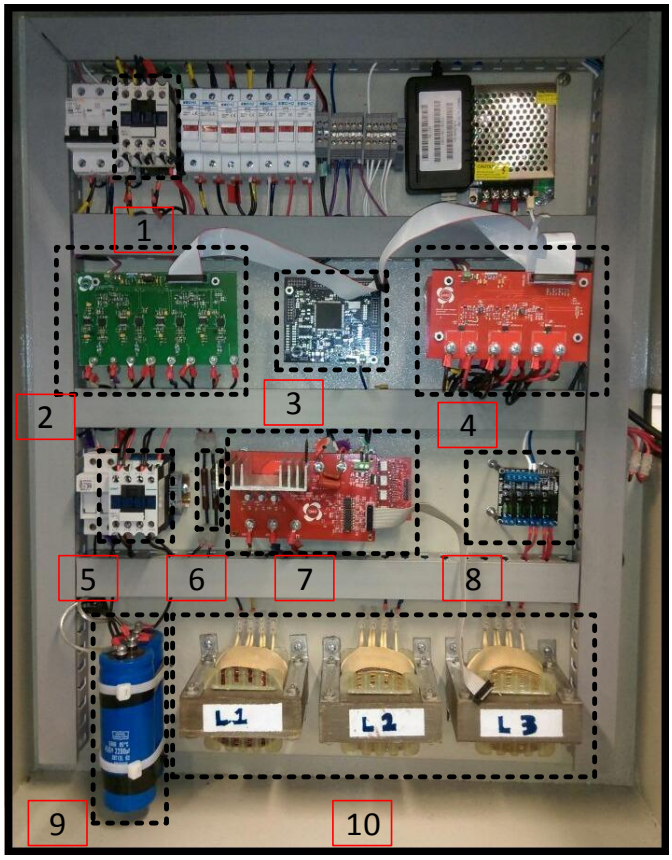

Fig. 13. D-STATCOM.

A. *Sensors, Analog to digital conversion and data conditiong*

In this section, a validation of the measurement systems is shown. Table III presents the measured voltage by means of a scope GW INSTEK GDS-2240A and with the sensor voltage PCB. Fig. 14 presents a plot and linear regression of data from table III; it is shown the linearity of sensor for voltage measurement with a $R^2 = 0.996$; this property allows the sensor calibration using any calibration device.

TABLE III
MEASUREMENT OF VOLTAGE SENSOR

Input voltage measured (rms)	Microcontroller voltage (rms)
60.10	0.6717
50.00	0.5727
40.20	0.4737
30.40	0.3747
20.20	0.2616
10.50	0.1626

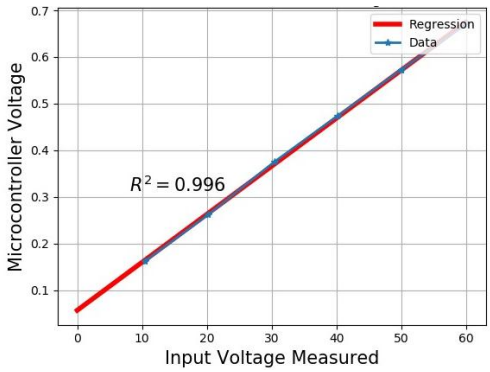

Fig. 14. Sensor linearity.

Same procedure was applied to all current and voltage sensors, providing reliable measurements. Fig. 15 shows a sinusoidal signal from electrical grid that is captured by the ADC and its respective binary vector.

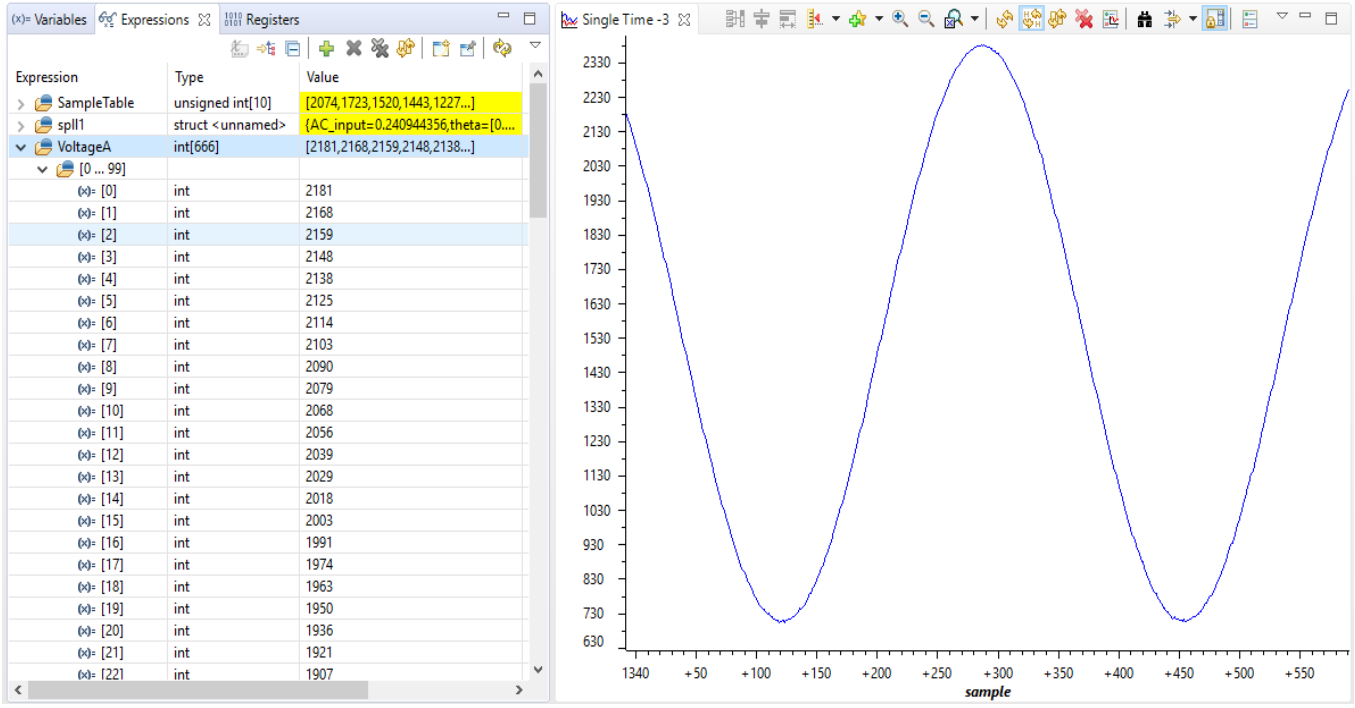

Fig. 15. Voltage measurement of phase A.

B. Phased locked loop (PLL)

Fig. 16 shows the PLL algorithm behavior (PLL algorithm following the grid signal). In this figure, the red sinusoidal signal corresponds to the grid voltage that is measured trough sensor PCB, sampled by ADC and entered to PLL algorithm. Blue signal is a digital signal generated by the microcontroller, it is programed to change state every time that the PLL algorithm predicts a zero cross of the grid signal. PLL correctly works when the square signal changes its state with sinusoidal signal zero crossing. Fig. 15 presents three stages: 1) microcontroller off, blue signal is off; 2) microcontroller turns on and PLL start to search for grid synchronization; and 3) PLL is synchronized with the grid.

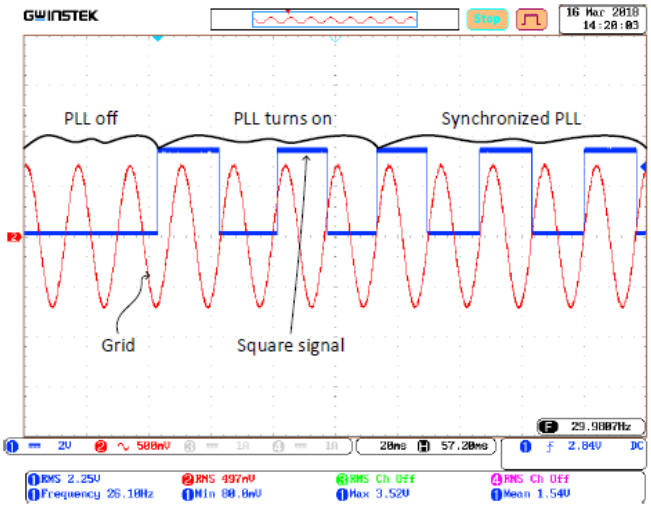

Fig. 16. PLL behavior.

C. Clarke-Park transform

Fig. 17 shows Clarke-Park transform done by the TMS320F28335 microcontroller. Fig. 17a shows time domain of three-phase D-STATCOM currents in open loop without load; currents (i_D^{abc}) are shown in solid blue (i_D^a) orange (i_D^b) and green (i_D^b) colors, also grid phase (v_G^a) voltage of phase A is shown in dotted black (only for the reference phase). In figure 17a, i_D^a is leading to v_G^a, it means that D-STATCOM has a capacitor behavior.

Fig. 17b shows dq0 transformation of current signals using the algorithm described at previous sections. Blue signal represents current direct component (i_D^d) associated to the D-STATCOM active power, orange signal represents current quadrature component (i_D^q) associated to positive reactive power and finally green signal represents zero component (i_D^0) associated at unbalances between phases.

Notice that the time domain signals exhibited unbalances due to load imperfections, this explains the presence of i_D^0 component in its dq0 transformation.

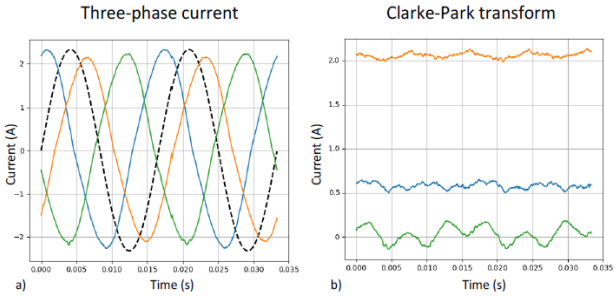

Fig. 17. Park transform done by microcontroller TMS320F28335.

D. SPWM modulation

Fig. 18 shows microcontroller SPWM modulation at minimum and maximum values of reference signal.

Reference signal (M_C^a) is shown in green and SPWM modulation is shown in red. Notice that when reference signal is at its minimum, modulation signal is at low level most of the time (i.e. lower IGBT activated). Instead, when reference signal is at its maximum, modulation signal is at its maximum value (i.e. upper IGBT activated) most of the time.

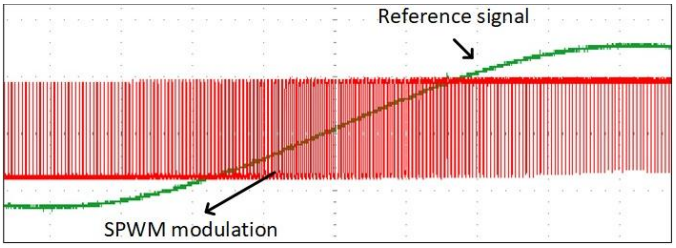

Fig. 18. SPWM modulation implemented.

E. D-STATCOM operation

In this subsection, operation of D-STATCOM as a complete system is evaluated. Inductive and capacitive loads where connected to the grid and D-STATCOM capacity to compensate reactive power was observed.

Fig. 19 shown the D-STATCOM behavior operating as capacitor taken from oscilloscope. In Fig. 19a, it is observed currents (4.43 Arms) from phases A (upper graphic), B (middle graphic) and C (low graphic) are leading respect to grid voltage (44 Vrms). Phasor diagram is presented in Fig.19b; figure shown a D-STATCOM angle of 81.63° (close to 90° due to active power losses) respect to grid voltage. Fig. 19c presents the harmonics from current signal of phase A, where the THD is minor than 5%.

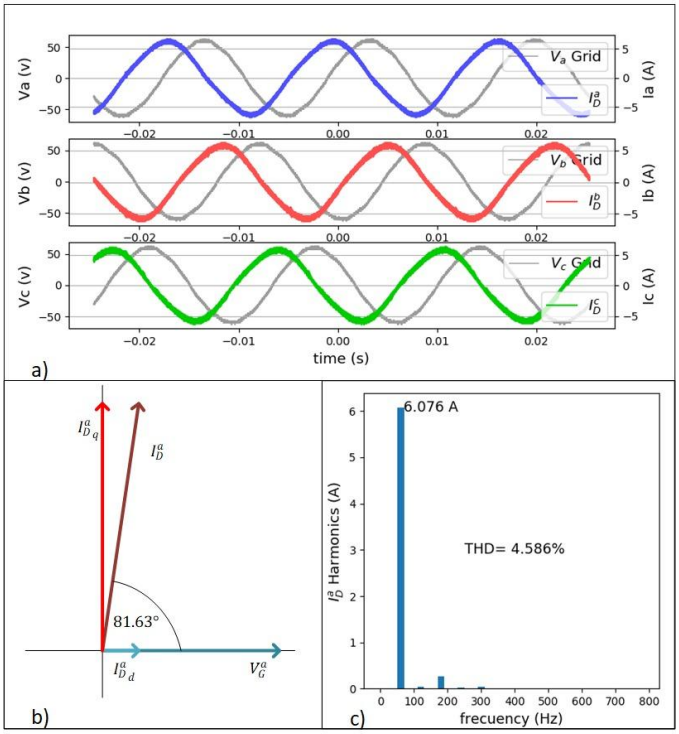

Fig. 19. D-STATCOM operation.

First, a resistive-inductive load was tested. Fig. 20 shows grid current signals in time domain before and after D-STATCOM operation, phase current A is blue, B is red and C is green, also each plot reproduces in gray the respective grid phase voltage in order to have phase references. Notice that Fig 20 plots are divided in two parts: left part shows grid currents without D-STATCOM operation and right part with D-STATCOM operation. Transient condition due to STATCOM start is omitted, showing only steady state.

It can be seen that after D-STATCOM operation, grid currents and voltages appear to be on phase. This can be verified in the phasor diagrams showed in Fig. 20a and Fig. 20b. Before operation, grid current has a -33.02º angle against voltage, after start of operation the angle was reduced to 5.11º. Considering power factor, this corresponds to a correction from 0.83 to 0.99. Notice also that grid current magnitude was decreased.

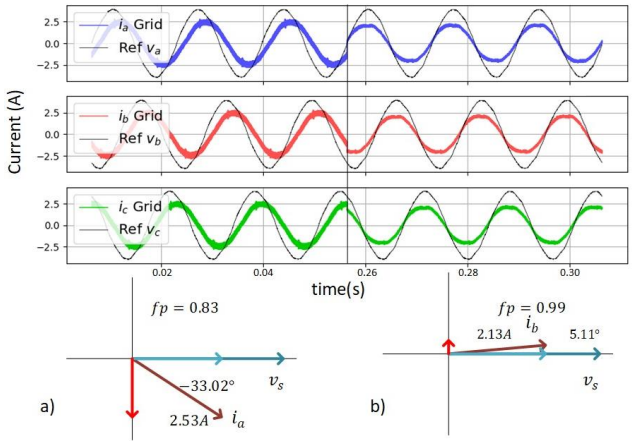

Fig. 20. D-STATCOM operation with resistive-inductive load.

Fig. 21 presents the operation results when D-STATCOM compensates a capacitive load. Capacitive load is nonlinear, demanding reactive power and injecting harmonics to the electrical grid. Fig. 21a shows measurements before D-STATCOM operation. In this state, load has a power factor of 0.049 and phasor diagram shows a load current of 2.04 Amp in quadrature with v_s, i.e. load mainly demands reactive energy. Fig.21b shows measurements after D-STATCOM operation. Power factor is increased up to 0.99 remaining only the harmonic distortion caused by the load. In consequence, the current demanded to electrical grid was decreased up to 0.49 Amp

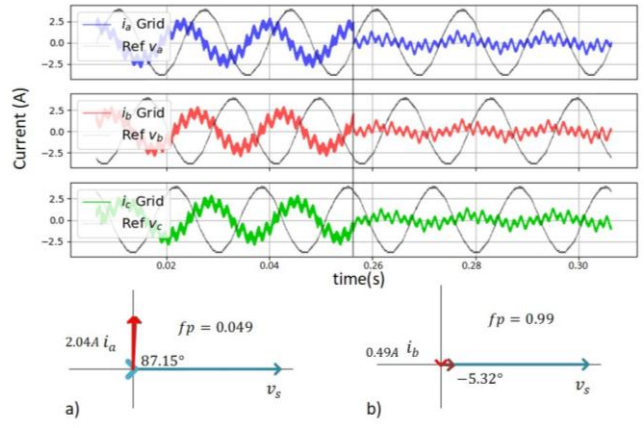

Fig. 21. D-STATCOM operation with capacitive load.

VI. Conclusion

In this paper, a description of hardware and firmware development for a D-STATCOM was presented; D-STATCOM main function is reactive power compensation. The implemented prototype includes voltage and current measurement, signal processing, control algorithms, switching and associated hardware. Most relevant prototype parts were described and its functionality was verified.

D-STATCOM prototype demonstrated that it is technically possible to replace traditional reactive power compensation techniques (as capacitive banks) in distribution networks. D-STATCOM implementation allows a precise control of the reactive power, also digital electronics devices can be remotely monitored, enhancing diagnostics and maintenance.

This prototype becomes a research platform for testing of different control schemes, and even implementation of harmonics and unbalances compensation. Also, due to its modular conception, D-STATCOM can be used in AC systems and power electronics practical teaching.

Acknowledgment

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Consideraciones técnicas para la sintonización de los controladores de un D-STATCOM real a partir de un modelo simulado

Technical considerations for tuning the controllers of a real D-STATCOM by means of a simulated model

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Resumen

Este artículo presenta una herramienta técnica para determinar la primera acción de control de los controladores PI de un Distribution STATic COMpensator (D-STATCOM) real a partir de valores teóricos; además, se muestra la sintonización final de los controladores y un método para cargar el bus DC al voltaje requerido. La topología del D-STATCOM que se utiliza consiste en dos capacitores conectados como bus DC de un Voltage Source Converter (VSC) conectado a la red a través de inductancias. Los valores iniciales se determinan con la teoría de intercambio de energía entre dos fuentes. Este método fue implementado en hardware real basado en un modelo teórico que fue controlado en simulación; sin embargo, el ajuste de los controladores no fue óptimo en el D-STATCOM real. Debido a variables no conocidas como las pérdidas. La mayoría de artículos encontrados en la literatura describen modelos y estrategias de control del D-STATCOM donde asumen el problema de la carga del bus DC resuelto y no explican cómo realizarlo.

Palabras clave: Control PI, D-STATCOM, eficiencia energética, sintonización, VSC.

Abstract

This paper presents a technical tool to determine the first control action of PI controllers for a real D-STATCOM by means of theoretical design; moreover, the final tune of controllers and a method to charge DC bus until required-voltage are shown. The used topology consists of two capacitors like DC bus of SVC which is connected to the grid through inductors. Initial values determination of controller is done with rules based on energy interchange between two sources. This method was implemented in a real hardware base on a theoretical simulated control model; however, the controllers from simulation were not optimums in the real D-STATCOM. These phenomena occur because there are unknow variables like losses. The losses do not provide exactly by fabricator. Most found papers in the literature describes models and control strategies of D-STATCOM where it is supposed DC problem solved, nevertheless, these papers do not explain how to charge DC bus.

Keywords: D-STATCOM, energy efficiency, inverter PI control, VSC.

Introducción

Un D-STATCOM es un dispositivo de electrónica de potencia perteneciente a los Flexible AC Transmission System (FACTS) [1]–[3]. El D-STATCOM tiene la capacidad de comportarse como inductor o capacitor con variación continua de amplitud de corriente; por lo tanto, este dispositivo es utilizado para compensar el factor de potencia en sistemas que tienen presencia de energía reactiva. Este dispositivo es importante porque soluciona directamente el problema asociado con la energía reactiva que está siendo penalizado en Colombia (consumo de energía reactiva artículo 25 de la CREG 108 de 1997). La topología del D-STATCOM estudiado utiliza un VSC [4]–[6]. El D-STATCOM consume energía activa y reactiva de la red; la energía reactiva es utilizada para compensar el factor de potencia asociado a elementos con componente inductiva o capacitiva conectados a la red; la energía activa es utilizada para cargar los capacitores, suministrar energía asociada a pérdidas por resistencias parasitas, por conmutación y térmicas para mantener el bus DC estable.

Los D-STATCOM han sido modelados [7]–[9] y controlados con diferentes estrategias de control [10]–[13]; estos artículos se enfocan en el modelo y el desarrollo, presentando herramientas matemáticas elaboradas para el funcionamiento, sin embargo, no presentan la precarga del bus DC y existe poca información sobre la implementación de un D-STATCOM real.

Un trabajo anterior del Grupo de Investigación en el Manejo Eficiente de la Energía (GIMEL) modeló y proporciono los parámetros de control PI utilizando lazo de control en cascada [10] para un D-STATCOM. El trabajo teórico

proporcionó un D-STATCOM funcionando en simulación; sin embargo, al implementar el D-STATCOM de la simulación en un prototipo real, la determinación de los parámetros asociados a resistencias de los inductores y capacitores, pérdidas térmicas y pérdidas por conmutación requiere tiempo extra para su determinación y dispositivos de medida costosos; este problema hace que la sintonización teórica de los controladores no sea la mejor en un sistema real ya que se desconocen esos parámetros, pero los valores PI proporcionados son la base para llegar a los definitivos; además, la simulación asumía que los capacitores tenían una precarga antes de iniciar el control los controladores reales no tienen la capacidad de estabilizar el bus DC cuando está alejado de su valor nominal.

La sintonización de los controladores en un D-STATCOM real y la precarga del bus DC presentada en este artículo, se obtiene trabajando en la caracterización del dispositivo, utilizando el concepto de intercambio de energía entre dos fuentes. Inicialmente se trabaja con el D-STATCOM en lazo abierto para proporcionar un estado inicial de la modulación Sine Pulse Width Modulation (SPWM). Este estado sirve para obtener los valores iniciales de los controladores del D-STATCOM; además, puede utilizarse como método de control cuando no se cuente con más herramientas. Este artículo presenta una visión del D-STATCOM que permite operar el dispositivo en lazo abierto sin implicar riesgos humanos y costos económicos.

Este trabajo se compone de introducción, una metodología dividida en subsecciones que describe el funcionamiento de un D-STATCOM, la descripción de la topología y el control en cascada, un método para la carga del bus DC, explica como aumentar los niveles del bus DC, un algoritmo para determinar los parámetros del primer valor de control y los pasos para sintonizar el control PI a partir de los controladores obtenidos del modelo simulado; se presentan resultados de los algoritmos propuestos en un D-STATCOM real de laboratorio; y las conclusiones.

2. Metodología

En esta sección se analiza un D-STATCOM, se plantea el control en cascada, se propone un algoritmo para la precarga del bus DC y la sintonización de los controladores del D-STATCOM a partir de los resultados teóricos y simulados.

2.1 Funcionamiento de un D-STATCOM a partir del intercambio de energía

La Figura 1 a) muestra el principio de funcionamiento del D-STATCOM con el que se trabaja en este artículo. En esta topología se utiliza una fuente de voltaje DC que estabiliza un bus DC, un VSC y unas inductancias que sirven como elementos de acople a la red (V_s) y filtro de armónicos. El VSC realiza la inversión DC/AC utilizando la modulación SPWM, la cual tiene la capacidad de imponer la magnitud y la fase del voltaje.

La Figura 1b) se usa para explicar el intercambio de energía bajo un modelo simplificado. En esta figura se tiene V_s y el voltaje en los bornes del D-STATCOM (V_{ev}) conectados a través de una inductancia. La corriente que entrega la fuente de voltaje esta dada (1).

$$I_s = \frac{V_s \angle 0 - V_{ev} \angle \alpha_e}{JwL} \quad (1)$$

En la Ec. (1), I_s representa la magnitud y fase de la corriente resultante del intercambio de energía entre las dos fuentes; V_s tiene ángulo cero porque es la referencia; y V_{ev} tiene el ángulo de desfase entre la fuente V_s y el D-STATCOM. La magnitud y fase de la corriente I_s está determinada por la diferencia entre V_s y V_{ev}; por lo tanto, modificando V_{ev}, se tiene control sobre la corriente que entrega V_s.

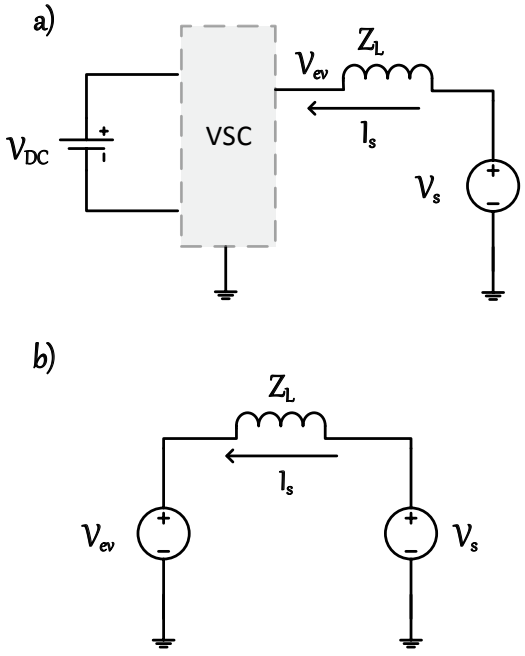

Figura 1. a) Intercambio de energía con el D-STATCOM. b) Intercambio de energía entre fuentes.

2.2 Esquemático del D-STATCOM implementado y control en cascada

En la Figura 1 a) se muestra una topología de un D-STATCOM que utiliza una fuente de voltaje DC para explicar cómo se controla la corriente por medio del intercambio de energía. Sin embargo, en este artículo se utiliza la topología de la Figura 2. Esta topología utiliza dos capacitores para estabilizar el bus DC en vez de una fuente de voltaje DC que es el caso de un D-STATCOM real. En esta figura se muestran las tres fases que tiene el D-STATCOM, las inductancias de acople a la red y relés de conexión del equipo con la fuente. En esta topología se debe utilizar energía activa de V_s para soportar las pérdidas presentes en el equipo y mantener el bus DC estable.

El D-STATCOM utiliza un control en cascada (ver Figura 3 a) para mantener estable el bus DC, y determinar la energía activa que necesita; además, posee un lazo de control simple (ver Figura 3 b)) para controlar la energía reactiva requerida y así compensar el factor de potencia de la red. Las acciones de control de ambos controladores actúan sobre la modulación SPWM, por lo tanto, el índice de modulación M se representa utilizando la transformada de Park como M_d y M_q (ver Figura 3). M_d tiene efecto sobre la energía activa para mantener estable el bus DC y M_d actúa sobre la compensación de energía reactiva.

La Figura 3 a) muestra el esquema de control en cascada utilizado para

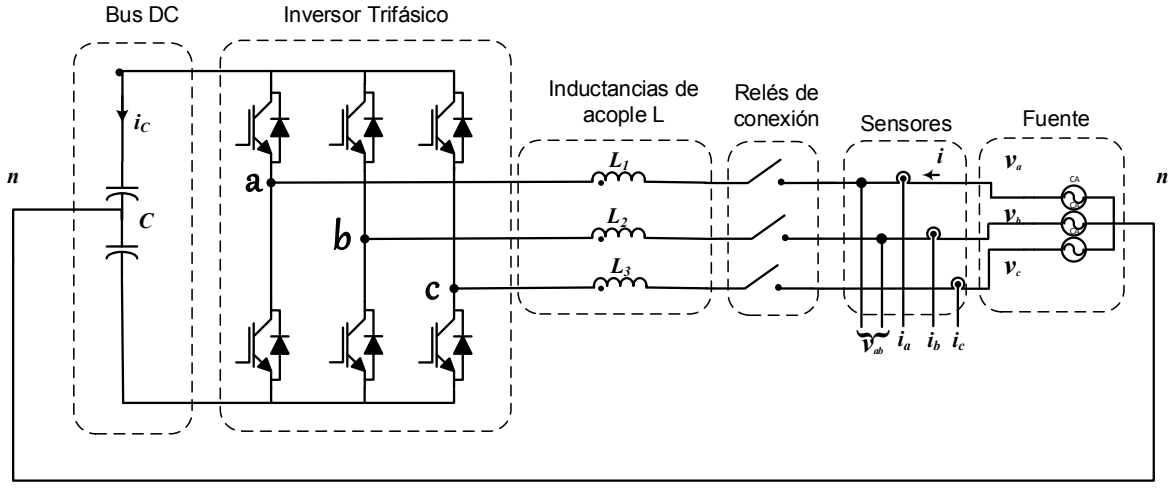

Figura 2. Esquemático del D-STATCOM.

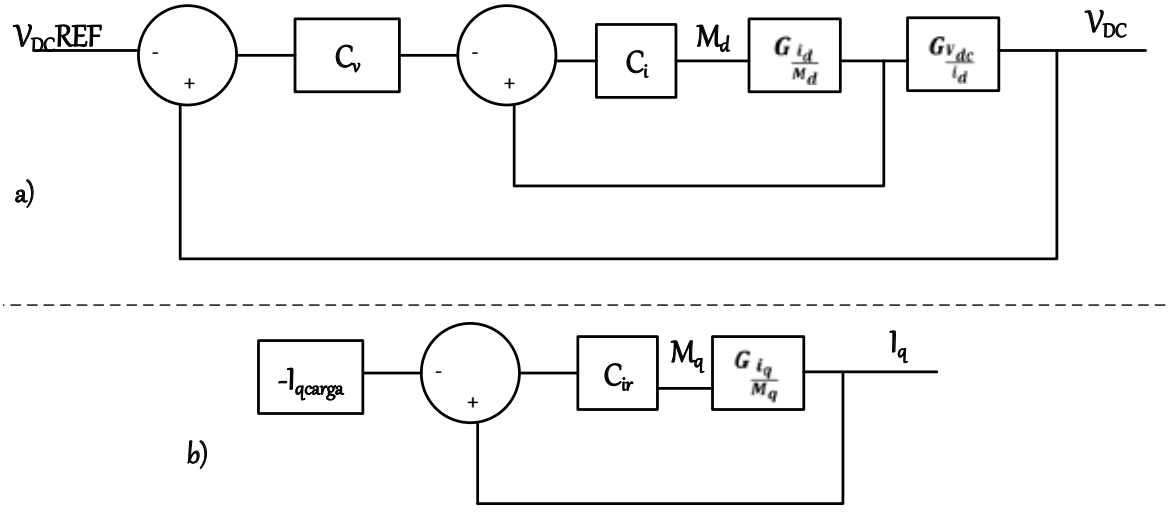

Figura 3. Estrategia de control en cascada para el voltaje del D-STATCOM.

estabilizar el voltaje V_{DC} en los capacitores del bus DC. El control en cascada requiere dos controladores: un controlador para estabilizar el bus DC (C_v) cuyo resultado es la referencia del controlador. El controlador C_i realiza la acción de control M_d que actúa sobre la planta $G_{id/Md}$ para establecer la corriente activa que necesita el dispositivo; la salida de esta planta pasa por la planta $G_{V_{dc/id}}$ la referencia del controlador C_v es el voltaje de operación que se requiere en el bus DC ($V_{DC}REF$) y la acción de control de C_v es la referencia de corriente activa para cargar el bus DC (ver Figura 3a)). La referencia para control del factor de potencia C_{ir} mostrado en la Figura 3b) es el negativo de la corriente reactiva de la carga, la acción de este controlador es M_q que actúa sobre la planta $G_{i_{q/Mq}}$.

2.3 Fenomenos de carga del bus DC y de corriente reactiva

2.3.1 Primera carga del bus DC

El bus DC necesita una precarga ya que el modelo de control utilizado para el D-STATCOM no tiene la capacidad de cargar el bus DC desde cero a los valores requeridos. El voltaje DC de los capacitores debe ser mayor que el voltaje pico de la fuente de energía para tener control del voltaje y realizar el intercambio de energía deseado.

El primer nivel de voltaje de los capacitores se obtiene sin realizar modulación, dejando los interruptores abiertos y permitiendo que los únicos elementos que se activen sean los diodos comportándose como un rectificador (ver Figura 4). La Figura 4 muestra una topología con conexión de neutro, por lo tanto, el voltaje de cada uno de los capacitores es el voltaje pico de la red y el voltaje total es el doble del voltaje pico de la red. La carga de los capacitores demanda corriente alta de arranque, por lo tanto, es necesario que en el tiempo de carga de los capacitores se utilicen resistencias para disipar la energía y evitar daños en el equipo; luego de que se lleva el D-STATCOM a las condiciones iniciales de operación, las resistencias deben ser aisladas para su correcto funcionamiento.

Luego de tener el bus DC cargado con los valores de la red, los interruptores se modulan con índice ($M<\alpha$) igual a uno y un desfase α de cero respecto a la red. Al realizar esta acción se tiene un voltaje V_{ev} (ver Figura 1 b) con la amplitud del doble del voltaje pico de la red V_s y con desfase cero. Esta última condición muestra que el intercambio de energía con la red es cero (Ec. 1) debido a que la red y el D-STATCOM tienen el mismo voltaje.

2.3.2 Carga de capacitores a un voltaje mayor

La primera parte importante consiste en tener el bus DC cargado y el VSC modulando como se muestra en la

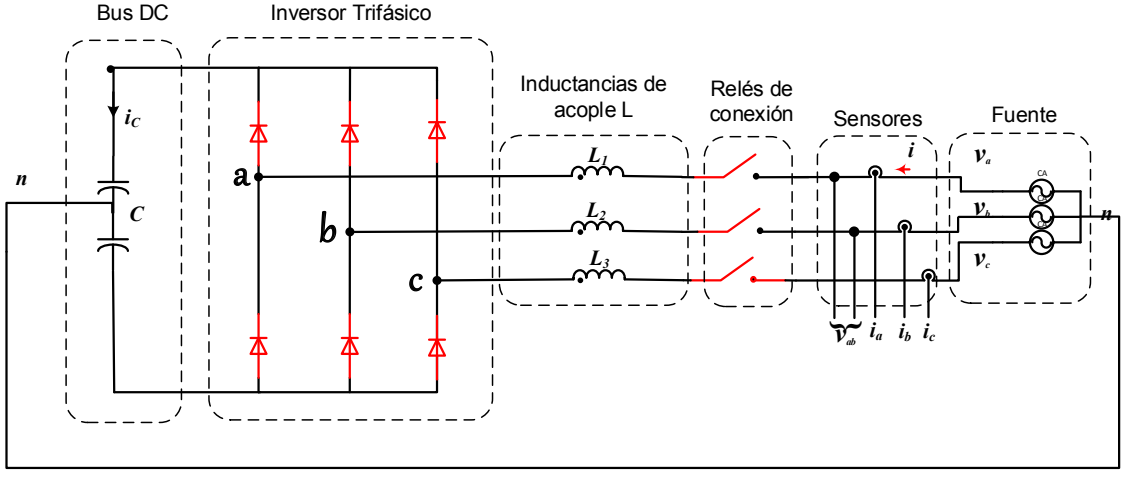

Figura 4. Primera carga del bus DC.

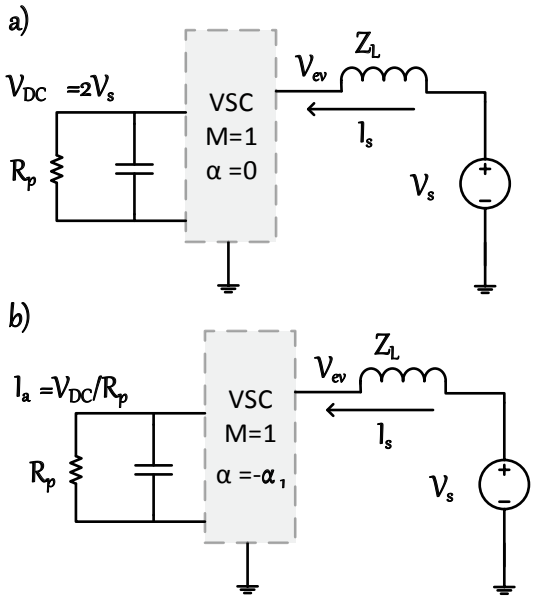

Figura 5. D-STATCOM con resistencia de pérdidas a) y b) .

Figura 5. ($M=1$ y $\alpha=0$); luego de tener el bus DC cargado inicia el proceso para elevar el voltaje variando el valor α. En el momento en que el valor de crece a un valor $-\alpha_1$ la fuente V_s empieza a entregar potencia activa al D-STATCOM (ver Figura 5 b), y como este dispositivo no consume potencia, esa corriente activa la absorbe la resistencia de pérdidas y aumenta el voltaje del bus DC hasta encontrar un equilibrio con el sistema. El hecho de que aumente el voltaje del bus DC, implica la aparición de energía reactiva para mantener el equilibrio (ley de voltajes de Kirchhoff) y una corriente reactiva capacitiva en la Ec. 1.

Es importante apuntar que cuando los cambios de son negativos el bus DC adquiere mayores magnitudes, comportándose como impedancia capacitiva, y que cuando son positivos el bus DC empieza a bajar hasta llegar a cero comportándose como impedancia inductiva. (se sugiere cambiar el valor de paulatinamente en magnitudes de -1 grado, para evitar sobre picos que dañen el dispositivo o afecten el funcionamiento del sistema)

2.4 Algoritmo para cargar el bus DC y determinar los valores iniciales de la modulación SPWM

La Figura 5 muestra el índice de modulación M y un ángulo de desfase α con respecto a la fuente de voltaje $V_{s.}$ El control propuesto en este trabajo se realiza considerando corriente activa y reactiva de forma independiente y las acciones de control sobre los valores M_d y M_q.

La Figura 6 muestra dos valores de M: M_1 y M_2. M_1 tiene ángulo de cero, por lo tanto, $M_{1d} = M_1$ y $M_{1q} = 0$. M_2 tiene ángulo de α_2, por lo tanto, $M_{d2}=M_2\, cos(-\alpha_2)$ y $M_{q2}=M_2\, sen(-\alpha_2)$

La Figura 7 muestra el algoritmo para determinar los valores de M_d y M_q que llevan al bus DC al valor deseado y la corriente reactiva a cero. La condición inicial para la búsqueda de M_d y M_q es

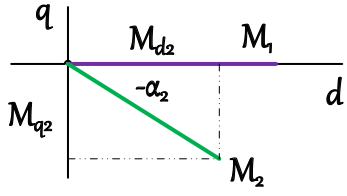

Figura 6. Esquema para determinar con variaciones de .

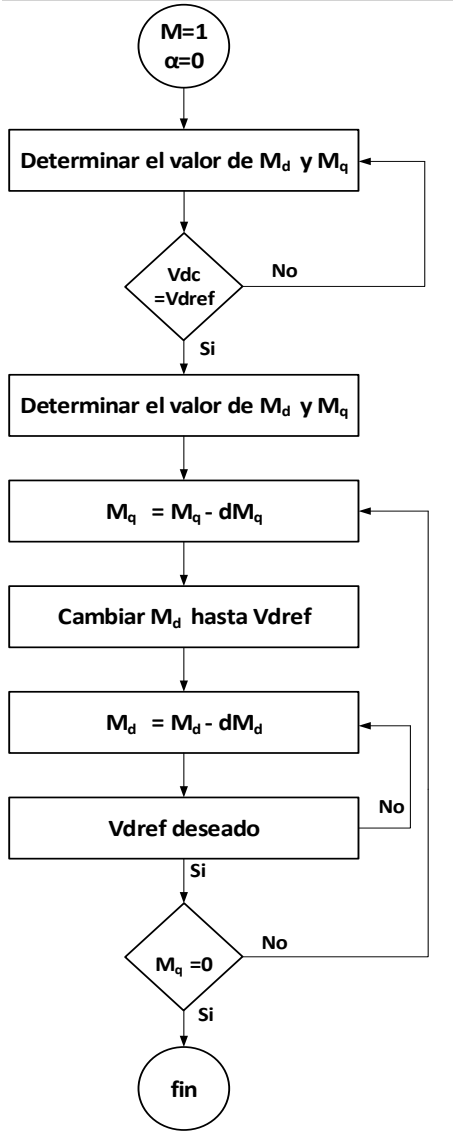

Figura 7. Algoritmo para determinar M_d y M_q para cargar el bus DC.

establecer M=1 y α=0. En esta condición se tiene una carga inicial del bus DC; Luego se cambia α hasta llegar al bus DC de referencia (los cambios de alfa iniciales deben ser pequeños 1 grado o menos, luego de conocer el sistema realiza los cambios como desee); cuando se llega al valor deseado se determina el valor de M_d y M_q. El objetivo es llevar M_q a cero y conocer el valor de M_d que estabiliza el bus DC en el valor de referencia. El algoritmo propone cambiar M_q en dos pasos para reconocer el sistema.

2.5 Sintonización de los parámetros PI de los tres controladores del D-STATCOM

El modelo del D-STATCOM fue simulado en PSIM y se mostró el dispositivo controlando con variaciones de carga; sin embargo, cuando se implementa el dispositivo real no se tiene información suficiente sobre los elementos parásitos. Este problema implica que la sintonización en el dispositivo real debe ajustarse para alcanzar el funcionamiento deseado. Los valores PI del modelo teórico (Figura 3) y el procedimiento proporcionado por la Texas Instrument para la sintonización [14], [15] son utilizados para resolver este problema y obtener los valores finales de control.

El control de este D-STATCOM tiene un control en cascada, por lo tanto, se sintoniza primero el control de voltaje DC, luego se sintoniza el control de corriente activa (ver Figura 3a); y por último se sintoniza el controlador simple de corriente reactiva.

Los pasos para sintonizar el controlador propuestos, basados en la guía de Texas Instrument son:

1. Imponga el control I en el valor simulado previamente, y utilice la ganancia P del valor simulado.

2. Varíe gradualmente la ganancia P hasta obtener un damping entre 0.4 y 0.7 [16].
3. Realice cambios pequeños en el valor de I. El parámetro I puede desestabilizar el sistema fácilmente. A medida que va incrementando el valor de I, es necesario decrementar el valor de P en pequeñas cantidades para que no afecte el sobre pico.

3. Resultados

Los resultados mostrados se toman del D-STATCOM en proceso de desarrollo mostrado en la Figura 8. Este D-STATCOM se conecta a la red por medio de transformadores de 12-120 V. la referencia de voltaje del bus DC es 60 voltios y controla corriente reactiva hasta 1.4 Amperios pico. La medida de corriente del dispositivo está diseñada para medir 5 amperios, por lo tanto, cuando se miden corrientes muy pequeñas, puede haber problemas de ruido. A pesar de esto, el control funciona con la sintonización propuesta.

La Tabla 1 muestra el resultado de aplicar el algoritmo de la Figura 7. En esta tabla se describe el valor de α, M, M_d, M_q, V_{DC}, el valor de la corriente directa I_d y el valor de la corriente en cuadratura I_q. El algoritmo inicia el reconocimiento del sistema variando α paulatinamente hasta llegar a la fila 6 donde se logra el voltaje de referencia; luego se empieza a variar M_d y M_q para tener los valores iniciales del control, que además realizan la precarga del bus DC. La fila 13 de la tabla 1 se resalta con negrilla los valores iniciales del controlador.

Figura 8. D-STATCOM utilizado para el diseño del control.

La Figura 9 muestra el estado del D-STATCOM cuando se llega al voltaje DC de referencia. La Figura 9 está asociada a los resultados de la fila 6 de la tabla I cuando se encuentra por primera vez el voltaje de referencia. La Figura 9 a) muestra el voltaje de la señal trifásica (fase A azul, fase B, anaranjada y fase C verde) que tiene le D-STATCOM y el voltaje DC (rojo) de referencia en 60 voltios. La Figura 9 b) muestra que las corrientes (fase A azul, fase B, anaranjada y fase C verde) en lazo abierto variando α son capacitivas (la señal en fase con la red es la negra punteada) y visualmente son senoidales y la Figura 9 c) muestra la transformada de Par de la corriente mostrada en la Figura 9 b). la transformada de Park muestra que I_d (azul) I_d

Tabla 1. Resultados del proceso del algoritmo de la Figura 7.

fila	α (grados)	M	M_d	M_q	V_{DC} (V)	I_d (A)	I_q (A)
1	0	1	1	0	35.72	0	0
2	-5	1	0.996	-0.087	37.62	0.023	0.081
3	-8	1	0.990	-0.139	40.87	0.063	0.312
4	-10	1	0.984	-0.173	45.19	0.139	0.683
5	-12	1	0.978	-0.207	51.09	0.268	1.116
6	**-15**	**1**	**0.965**	**-0.258**	**63.28**	**0.602**	**2.140**
7	-7.6	0.97	0.965	-0.129	41.56	0.060	0.285
8	-9.1	0.81	0.800	-0.129	50.65	0.084	0.331
9	-10.4	0.71	0.700	-0.129	59.24	0.116	0.421
10	0	0.70	0.700	0	50	0.031	0
11	0	0.65	0.650	0	53.76	0.038	0
12	0	0.60	0.600	0	57.61	0.042	0
13	**0**	**0.56**	**0.560**	**0**	**61.07**	**0.047**	**0**

(anaranjada) se comporta como una línea recta (si fuese ideal sería una línea recta), mientras que I_z (verde) muestra que existe un desbalance. Este desbalance ocurre porque las inductancias de acople a la red no son exactamente iguales.

La Figura 10 muestra el estado del D-STATCOM cuando se llega al voltaje DC de referencia y se ha llevado a cero. La Figura 10 está asociada a los resultados de la fila 13 de la tabla 1 cuando se encuentra al voltaje DC de referencia; esta es la condición inicial del control en cascada. La Figura 10 a) muestra el voltaje de la señal trifásica (fase A azul, fase B, anaranjada y fase C verde) que tiene le D-STATCOM y el voltaje DC (rojo) de referencia en 60 voltios. La Figura 10 b) muestra que las corrientes (fase A azul, fase B, anaranjada y fase C verde) en lazo abierto variando α son aproximadamente cero y la Figura 10 c) muestra la transformada de Park de la corriente mostrada en la Figura 10 b), aproximadamente cero. la transformada de Park muestra que I_d (azul) I_d (anaranjada) e I_z (verde) no tienen una forma definida. Esto ocurre porque la energía que transmite la red al D-STATCOM es muy pequeña. A pesar de este fenómeno, se ve en la Figura 10 c) que I_d es mayor que las otras dos señales. Esto ocurre porque se necesita energía para alimentar las pérdidas del D-STATCOM y mantener el bus DC estable.

La Tabla 1 muestra que si se cambia M_q se debe modificar M_d para estabilizar el bus DC en un valor constante. Estos cambios implican que si se cambia la carga reactiva que se quiere compensar, cambia la referencia de M_d y M_q y se ve un fenómeno transitorio en el bus DC. Resumiendo, cualquier cambio en la carga que se compensa sirve como escalón para evaluar el tiempo de estabilización de los controladores y determinar el damping.

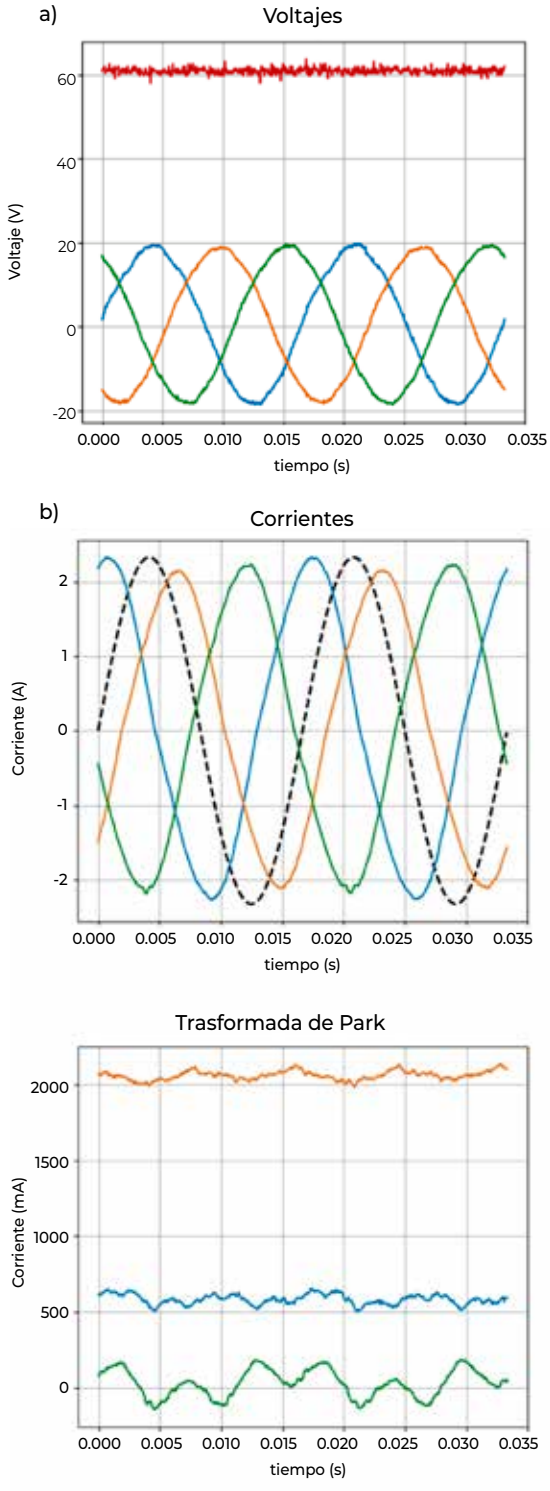

Figura 9. Resultados gráficos de la fila 6 de la Tabla 1.

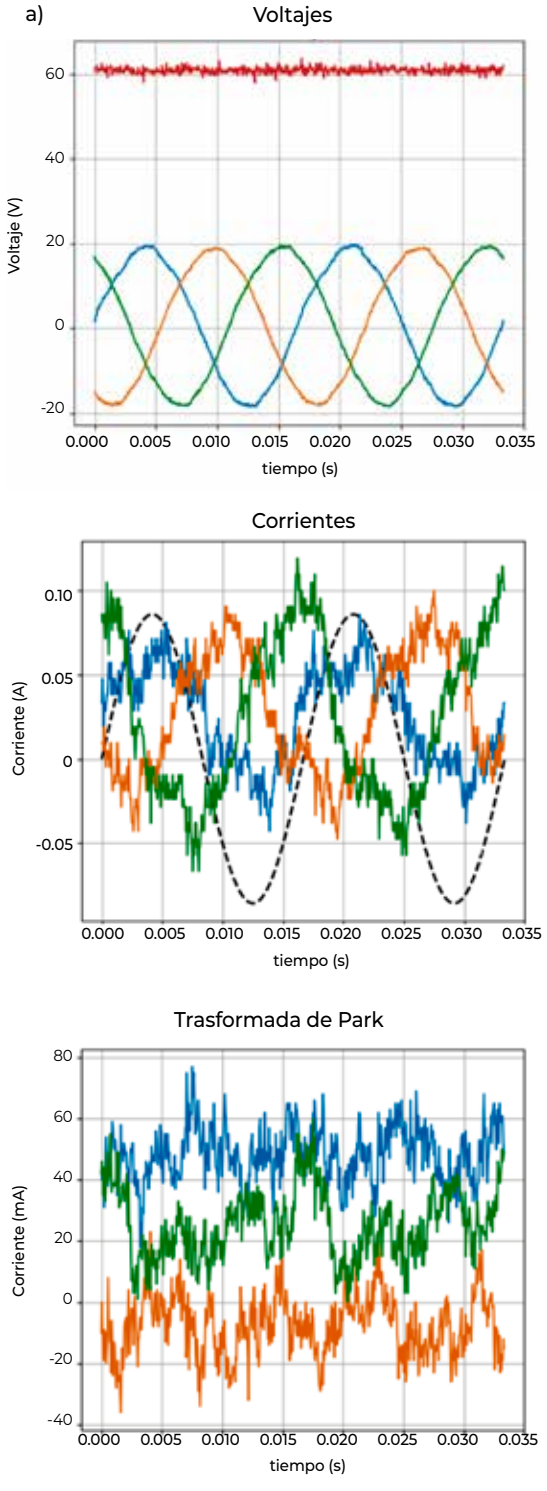

Figura 10. Resultados gráficos de la fila 13 de la Tabla 1.

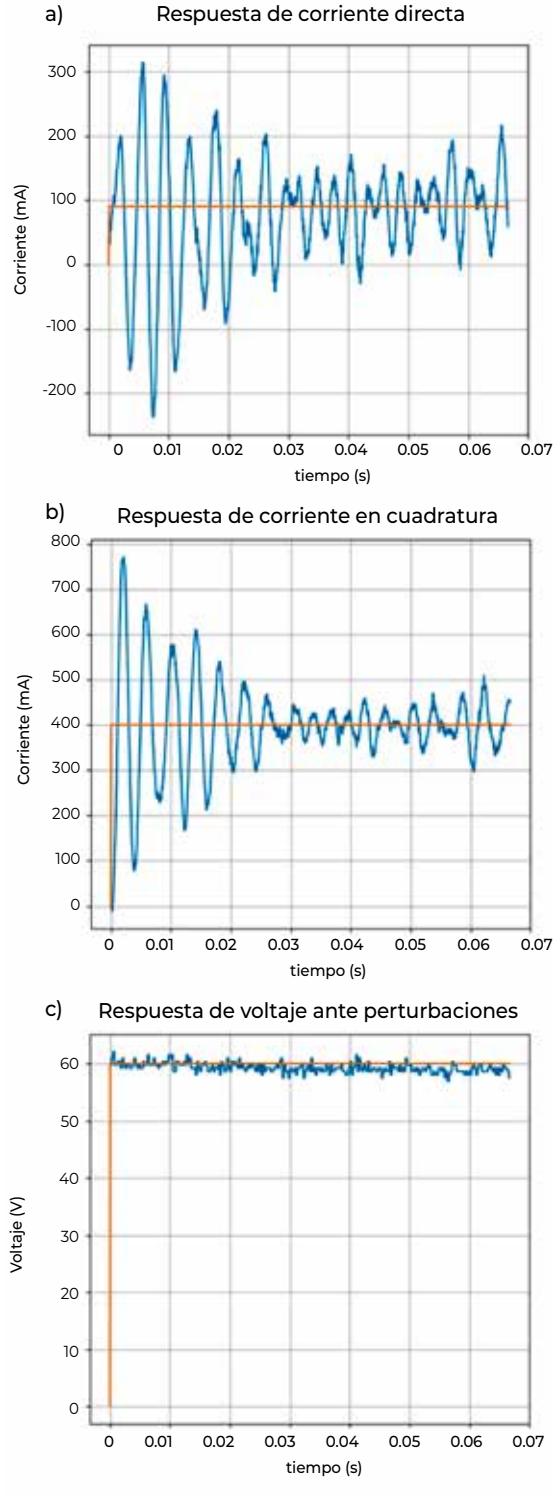

Figura 11. Respuesta ante el escalón con los valores PI teóricos y simulados.

La Figura 11 muestra las respuestas ante el cambio en la corriente de carga que se compensa utilizando los controladores teóricos simulados y la Figura 12 muestra las respuestas ante el mismo cambio utilizando los controladores obtenidos en este trabajo a partir de los controladores teóricos simulados. El cambio en la corriente que se implementa es de 0 a 400 mili amperios reactivos (se cambia en ese rango porque el primer controlador se desestabiliza cuando se le piden condiciones nominales por la sintonización)

La Figura 11 a) y 12 a) muestran la respuesta de I_d ante el cambio de carga. La Figura 11 a) tiene un sobre pico de 300 mA, mientras que la Figura 12 a) tiene un sobre pico de 200 mA. La Figura 11 a) tiene un tiempo de estabilización de 0.03 segundos, mientras que la Figura 12 a) tiene un tiempo de estabilización de 0.025 segundos.

La Figura 11 b) y 12 b) muestran la respuesta de ante el cambio de carga. La Figura 12 a) tiene un sobre pico de 750 mA, mientras que la Figura 12 b) tiene sobre pico de 500 mA. La Figura 11 b) tiene tiempo de estabilización de 0.03 segundos, mientras que la Figura 12 b) tiene tiempo de estabilización de 0.013 segundos. Y a la vista se percibe que la Figura 11 b) es más oscilante que la Figura 12 b)

La Figura 11 c y la Figura 12 c muestran la respuesta del bus DC. La respuesta del bus DC ante cambios de carga no es significativo porque él se mantiene igual, incluso es necesaria la precarga del bus DC para evitar inestabilidades.

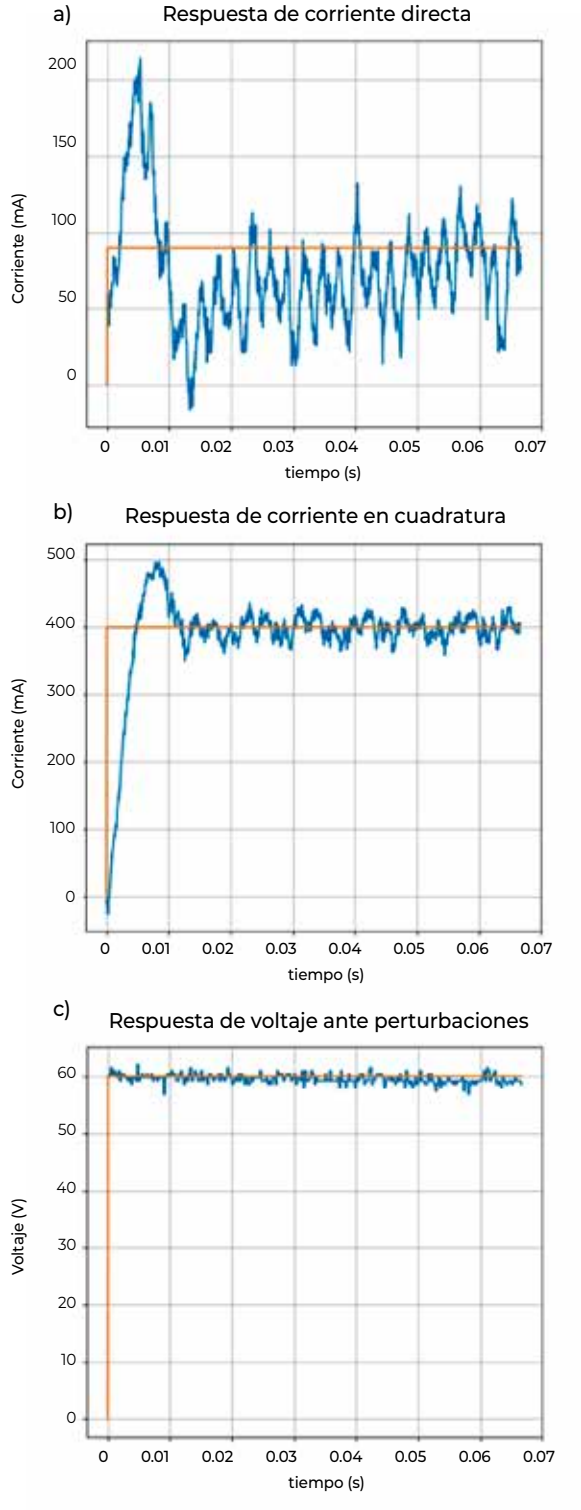

Figura 12. Respuesta ante el escalón con los valores PI obtenidos en esta propuesta.

4. Conclusiones

En este artículo se propuso una interpretación del D-STATCOM explicado a partir del principio del intercambio de energía entre dos fuentes. En este caso, una fuente simulaba el D-STATCOM y la otra fuente simulaba el comportamiento de la red eléctrica a la cual estaba conectado el D-STATCOM. Esta interpretación permite el funcionamiento del D-STATCOM en lazo abierto usada para caracterizar el dispositivo y sintonizar los controladores.

En este artículo se aborda el problema de la carga inicial de los capacitores del bus DC en un D-STATCOM real dado que en la literatura actual se asume que está resuelto. Por lo tanto, se propuso un algoritmo para reconocer el D-STATCOM y un método para realizar la primera carga de los capacitores para la inicialización de los controladores.

Después de realizada la carga del bus DC se desarrolla el algoritmo propuesto para la sintonización de los controladores del D-STATCOM real a partir de la modulación SPWM. Este proceso se realiza mediante el principio de intercambio de energía entre dos fuentes modificando M_d y M_q para analizar el intercambio de energía activa y reactiva entre el D-STATCOM y la red eléctrica.

Los resultados obtenidos de la sintonización del control en cascada del D-STATCOM real fueron comparados con los resultados del controlador obtenido por simulación. Los resultados muestran un mejor desempeño del D-STATCOM con el control diseñado bajo el algoritmo

propuesto en cuanto a tiempo de estabilización, respuesta del control y valores de damping que mejoran la respuesta inicial del D-STATCOM reduciendo el sobre pico máximo.

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Banda de Histéresis Adaptativa para un Convertidor AC-DC Elevador sin Puente, con Correccion del Factor de Potencia y Control por Modos Deslizantes

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Resumen

Se propone aplicar una banda de histéresis adaptativa que permite reducir la distorsión armónica total, el rizado y la deformación en el cruce por cero de la corriente de entrada de un convertidor AC-DC elevador sin puente con corrección del factor de potencia (PFC, Power Factor Correction). Se presenta un procedimiento para calcular la banda de histéresis con base en los estados dinámicos del convertidor electrónico de potencia, de tal forma que es posible fijar la frecuencia de conmutación. La banda es aplicable al control por modos deslizantes que permite mejorar el desempeño dinámico de los convertidores ante perturbaciones acotadas y cambios significativos de la región de operación. Se presentan los resultados de la simulación de un convertidor de 1 kW. Se muestra que es posible elevar el factor de potencia hasta 0.996, disminuir la deformación del cruce por cero, y reducir la distorsión armónica total en la corriente de entrada hasta 2.8 %, manteniéndola por debajo de los límites máximos permisibles del estándar EN/IEC 61000-3-2 (1000-3-2).

Palabras clave: banda de histéresis adaptativa; corrector del factor de potencia; rectificador controlado; modos de deslizamiento; frecuencia constante

Adaptive Hysteresis Band for a Bridgeless Boost Converter with Power Factor Correction and Sliding Mode Control

Abstract

It is proposed to apply an adaptive hysteresis band that allows to reduce the total harmonic distortion, the ripple and the deformation in the zero crossing of the input current of a bridgeless boost AC-DC converter with power factor correction (PFC). A procedure for calculating the hysteresis band based on the dynamic states of the converter is presented, in such a way that it is possible to keep fixed the switching frequency. The band is applicable to the sliding mode control that allows to improve the dynamic performance of the power converter in the presence of bounded perturbations and significant changes in operating region. The results of the simulation of a 1 kW converter are presented. It is shown that it is possible to raise power factor up to 0.996, to decrease the deformation of the zero crossing and to reduce the total harmonic distortion in the input current down to 2.8%, keeping it below the maximum permissible limits of the standard EN / IEC 61000-3-2 (1000-3-2).

Keywords: adaptive hysteresis band; power factor corrector; controlled rectifier; sliding mode; constant frequency

INTRODUCCIÓN

El convertidor AC-DC elevador sin puente (SBLB PFC, Semi Bridgeless Boost Power Factor Correction) presenta oscilaciones de amplitud y frecuencia finita alrededor de la señal de referencia (Muñoz-Galeano et al., 2016); este fenómeno, llamado "rizado" en la literatura de electrónica de potencia o "chattering" en la teoría de control reduce la precisión del controlador, incrementa las pérdidas de potencia y aumenta la distorsión armónica total en la corriente de entrada (THD_i; Total Harmonic Distortion in input current) (Utkin et al., 2017; Young et al., 1999). El control lineal con modulación PWM puede: reducir el rizado y el THD_i, aumentar el factor de potencia (PF, Power Factor) (Mejía-Ruiz et al., 2017; Huang et al., 2017; Kim et al., 2014), reducir el ruido de modo común (Man et al., 2017), incrementar la eficiencia (Alam et al., 2017; Bin y Lu, 2015; Chih-Chiang et al., 2016) y reducir la cantidad de sensores necesarios para el control de los convertidores electrónicos de potencia (Chen et al., 2017; Musavi et al., 2013). No obstante, el diseño de este controlador se realiza con base en el modelo lineal del convertidor y parámetros constantes; además, el cambio en la región de operación del convertidor y la variación de los parámetros limita la regulación y la respuesta dinámica del control lineal, estando inhabilitado para compensar perturbaciones significativas en la fuente o en la carga (Mohanty y Panda, 2017). El sistema de control lineal también es incapaz de compensar el componente DC en la corriente cuando el SBLB PFC tiene de forma inherente inductores de características diferentes en sus terminales (Marcos-Pastor et al., 2015).

El control por modos deslizantes (SMC, Sliding Mode Control) es una técnica no lineal derivada de la teoría de los sistemas de estructura variable (VSS, Variable Structure Systems). El SMC consiste en una ley de control discontinua, variante en el tiempo y con realimentación. (Utkin, 1977; Utkin et al., 2009). El SMC permite mejorar el desempeño dinámico de los convertidores en presencia de perturbaciones acotadas, cambios de operación y variación de los parámetros. El SMC también permite reducir el orden del sistema en lazo cerrado y suministrar la señal de activación y desactivación de los actuadores sin la intervención del sistema de modulación PWM, incrementando la velocidad de respuesta del controlador en lazo cerrado (Utkin, et al., 2017; Utkin, 1977; Utkin et al., 2009; Young et al., 1999). En (Marcos-Pastor et al., 2015) se desarrolla el SMC con circuitos analógicos para el SBLB PFC usando frecuencia de conmutación variable donde se evidencia el incremento del THD_i debido a la deformación de la corriente en el cruce por cero; una forma de reducir esto consiste en el uso de un controlador de corriente con banda de histéresis de ancho fijo que evita la introducción del componente DC en la corriente de la fuente, asegurando la simetría en cada semi-ciclo de la red. No obstante, el control con banda de histéresis de ancho fijo causa que la frecuencia de conmutación sea variable de tal forma que se hace necesario aumentar el tamaño y el costo de los filtros, los inductores y los disipadores de calor del sistema (Huber et al., 2008). La frecuencia variable también puede producir ruido audible e incrementar las pérdidas de potencia cuando el voltaje de la fuente tiene amplitud baja y la frecuencia de conmutación es alta (Ye et al., 2014; Guzman et al., 2016; Chincholkar y Chan, 2017; Pichan y Rastegar, 2017; Repecho et al., 2017).

Varios autores reducen el rizado fijando la frecuencia de conmutación; sin embargo, las metodologías de control presentadas deterioran el desempeño dinámico y la robustez del sistema (Mohanty y Panda, 2017; Ye et al., 2014; Chincholkar y Chan, 2017; Guzman et al., 2016; Pichan y Rastegar, 2017; Ye et al., 2014; Ashita et al., 2014). Además, el sistema de control requiere alta capacidad de cómputo que usualmente incluye unidades de punto flotante y arquitecturas de memoria de acceso múltiple para realizar los cálculos necesarios para fijar la frecuencia, incrementando los costos de la implementación. En (Marcos-Pastor et al., 2016) desarrollan un controlador de corriente valle para fijar la frecuencia de conmutación (f_{sw}) del rectificador con PFC; sin embargo, este método causa el incremento del tercer armónico en la corriente de entrada. El SMC también puede usar modulación PWM para fijar la frecuencia de conmutación; pero en la práctica, esta implementación es similar al control clásico PWM basado en la ley de control lineal y requiere que la función del control equivalente sea continua, de tal forma que no es posible la reducción del orden ni mejorar la robustez del sistema (Chincholkar y Chan, 2017; Mohanty y Panda, 2017). Este artículo propone una banda de histéresis adaptativa para un convertidor AC-DC elevador sin puente con corrección automática del factor de potencia que permite fijar la frecuencia de conmutación, disminuir el rizado, reducir la deformación de la corriente en el cruce por cero y el THD_i. Este artículo presenta el procedimiento de cálculo y la simulación de la banda de histéresis adaptativa mediante las siguientes secciones: el modelo dinámico de convertidor, la selección del sistema de control y el diseño detallado de la banda de histéresis propuesta. Finalmente, se presentan los resultados de la simulación y las conclusiones.

DESCRIPCIÓN DEL MÉTODO DE CONTROL

Los objetivos de control del SBLB PFC son: 1) controlar la forma de onda de la corriente de entrada (i_{in}), manteniéndola sinusoidal y en fase con el voltaje de entrada (v_{in}) para aumentar el PF; 2) controlar la amplitud del rizado de i_m cerca del cruce por cero para reducir el THD_i; y 3) regular el voltaje de salida (v_0) según los requerimientos de la carga. Además, el sistema de control deberá compensar las variaciones de la amplitud

en v_{in} y las variaciones de la potencia en la salida (P_0). Para lograr esto, primero se obtiene el modelo dinámico del sistema a controlar, luego se selecciona el método de control y finalmente, se diseña el modulador por banda de histéresis adaptativa.

Modelo dinámico del sistema a controlar con banda de histéresis adaptativa

El circuito del SBLB PFC y el sistema de control con la banda de histéresis adaptativa propuesta en este artículo se muestran en la Fig. 1. El SBLB PFC puede descomponerse en dos convertidores elevadores operativos según el semi-ciclo de la red (Mejía-Ruiz et al., 2017), por lo que se modela el sistema para cada semiciclo. El SBLB PFC posee dos interruptores Q_1 y Q_2, cuatro diodos D_1, D_2, D_3, y D_4, dos inductores L_1 y L_2, un condensador C y la resistencia de carga R_L (Alam et al., 2017; Jovanovic y Jang, 2005; Xu et al., 2014). Los interruptores Q_1 y Q_2 son accionados por la misma señal de control (u) (Franceschini et al., 2012; Marcos-Pastor et al., 2015) operando en la región de corte y saturación; en consecuencia, los convertidores exhiben un comportamiento dinámico no lineal y discontinuo. La obtención del modelo matemático considera las siguientes suposiciones: 1) los interruptores de potencia tienen resistencia cero en el estado de encendido y resistencia infinita en el estado de apagado, 2) el tiempo de conmutación es infinitamente corto, 3) las fuentes pueden suministrar potencia infinita en corto circuito, 4) la frecuencia de conmutación (f_{sw}) es mucho mayor que la frecuencia de la fuente de corriente alterna (f_0) ($f_{sw} \gg f_0$) y 5) los inductores L_1 y L_2 tiene igual valor (L_1=L_2 =L).

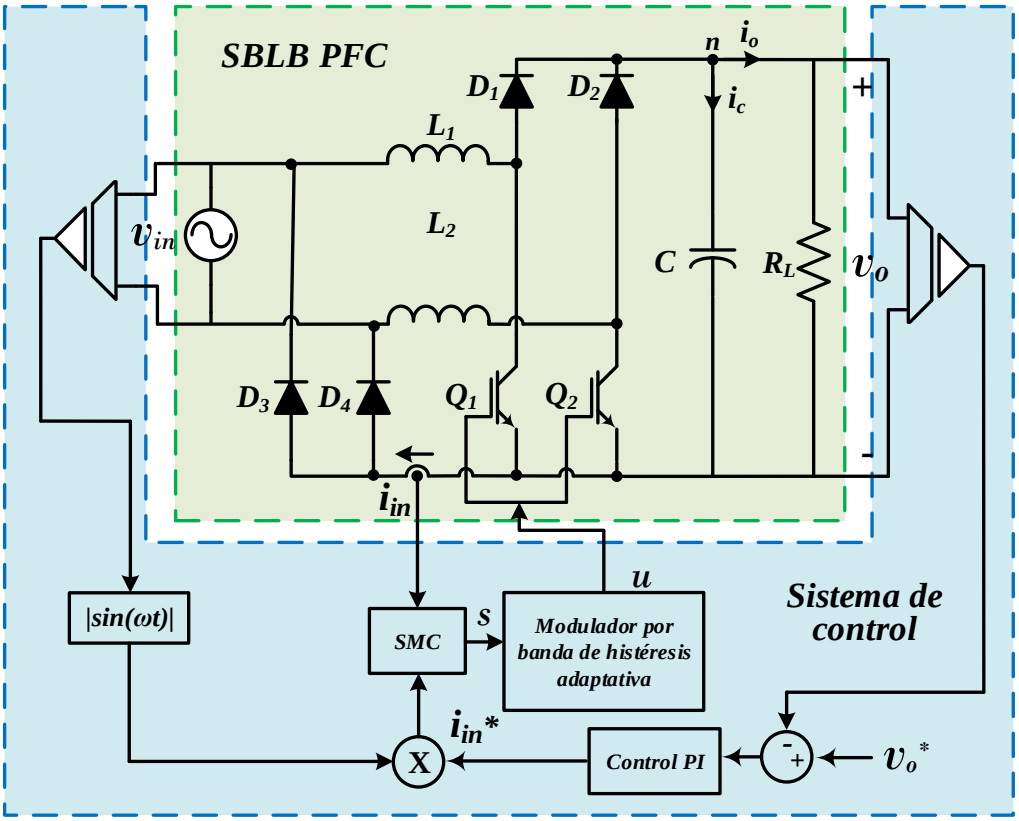

Fig. 1: Convertidor AC-DC elevador sin puente con PFC (SBLB PFC).

La banda de histéresis adaptativa se calcula con base en los estados dinámicos del SBLB PFC; razón por la cual, se encuentra el modelo del convertidor. Las ecuaciones (1) y (2) representan el modelo del sistema que es obtenido con base en las leyes de Kirchhoff y los estados de conmutación de Q_1 y Q_2. u=1se establece cuando los interruptores están cerrados, mientras que u=0 se establece cuando los interruptores están abiertos (Mejía-Ruiz et al., 2017).

$$\frac{di_{in}}{dt} = \frac{v_{in}}{L} - \frac{v_o}{L}(1-u) \tag{1}$$

$$\frac{dv_o}{dt} = -\frac{v_o}{R_L C} + \frac{i_{in}}{C}(1-u) \tag{2}$$

Selección del sistema de control

Las dinámicas del SBLB PFC son inestables cuando se emplea solo el controlador de voltaje (Utkin, 2016). Sin embargo, esta inestabilidad se puede eliminar mediante la implementación de un sistema con dos lazos de control en cascada como se muestra en la Fig. 1 (Alsmadi et al., 2017; y Yonglu et al, 2017). Este sistema requiere que el ancho de banda del controlador interno sea al menos 10 veces mayor que el ancho de banda del controlador externo (Mejía-Ruiz et al., 2017). El lazo externo (bloque de control PI, Fig. 1) permite regular v_0 y es implementado con un controlador Proporcional Integral (PI); los valores de la ganancia (K=0.5) y el tiempo de acción integral (T_i=0.3) del controlador se obtienen con base en la ubicación de los polos del sistema en lazo cerrado, teniendo como base un tiempo de establecimiento menor a 1s en v_0. La salida del controlador PI proporciona la amplitud de la señal de referencia para i_{in}; esta salida es multiplicada por la señal sinusoidal rectificada con la misma fase y frecuencia de v_{in} y el resultado es la señal de referencia (i_{in}*) para el controlador interno.

El control por modos deslizantes (Sliding Mode Control, SMC) corresponde al lazo interno (bloque SMC, Fig. 1) y permite controlar la i_{in}. El diseño del SMC comienza con la selección de la superficie de deslizamiento (S) (ecuación (3)) sobre la cual ocurre el modo de deslizamiento en el espacio de estados. El sistema en lazo cerrado se encuentra en régimen o dinámica deslizante cuando las trayectorias del sistema impuestas por la función de conmutación se dirigen hacia S=0. En la ecuación (3), $i_{in}=I\cdot sen(\omega t)$ es la corriente de entrada en estado estable. El valor de $I=2(v_0^*)^2/R_LV$ puede ser obtenido mediante un balance de potencia instantánea en la entrada y en la salida del convertidor ($P_{in}= P_0$), donde $<P_{in}>=VI/2$, $<P_0>=(v_0^*)^2/R_L$, v_0^* es el valor de referencia de v_0 y V es la magnitud de v_{in}. las condiciones de alcanzabilidad, existencia, transversalidad y control equivalente también deben ser consideradas en el diseño del SMC. La condición de transversalidad evalúa la capacidad del controlador para modificar las dinámicas del sistema con la superficie de conmutación propuesta (Utkin, 1977; Utkin et al., 2009; Young et al., 1999). La ecuación (4) muestra el cumplimiento de la condición de transversalidad cuando se aplica a la superficie de conmutación definida en la ecuación (3).

La condición necesaria y suficiente para que el sistema cumpla la condición de alcanzabilidad es $S(dS/dt)<0$ para todo $t>0$ y que $|S|\leq BH$; es decir que, la amplitud del rizado está acotada por BH y los estados del sistema convergen hacia S (Alsmadi et al., 2017; Utkin, 1977; Utkin et al., 2009; y Young et al., 1999). Cuando la transversalidad es positiva, la condición de existencia puede ser determinada por la inspección local de la condición de alcanzabilidad; tal que, en el dominio de $0<|S|<BH$ se satisfacen las ecuaciones (5) y (6) (Alsmadi et al., 2017; Utkin, 1977; Utkin et al., 2009; Young et al., 1999) para $v_{in}>0$ y $v_0>v_{in}$. El control equivalente (u_{eq}) es una ley de control que lleva al sistema a deslizarse sobre la superficie en forma ideal, obteniendo un valor continuo que representa el valor medio del control discontinuo; esto elimina la discontinuidad en el lado derecho de la ecuación diferencial (1) (Alsmadi et al., 2017). u_{eq} puede ser hallado con (dS/dt=0) como se muestra en la ecuación (7) (Alsmadi et al., 2017; Utkin, 1977; Utkin et al., 2009; Young et al., 1999). La región donde el modo de deslizamiento se produce esta dada por $0<u_{eq}<1$; es decir, el modo de deslizamiento puede producirse siempre que v_0 sea mayor que v_{in} ($0<v_{in}<v_0$). La ecuación (8) representa el movimiento de los lazos de i_{in} y v_0 durante el modo de deslizamiento que es obtenida al sustituir u_{eq} (ecuación (10)) en las ecuaciones (1) y (2); la ecuación (8) evidencia la reducción del orden del sistema al usar SMC, ya que este permite desacoplar las dinámicas de i_{in} y v_0.

$$S = i_{in} - i_{in}^{*} \tag{3}$$

$$\frac{d}{du}\left(\frac{dS}{dt}\right) = \frac{d}{du}\left(\frac{di_{in}}{dt} - \frac{di_{in}^{*}}{dt}\right) = \frac{d}{du}\left(\frac{v_{in}}{L} - \frac{v_o}{L}(1-u)\right) = \frac{v_o}{L} \neq 0 \tag{4}$$

$$\lim_{S=0^-}\frac{dS}{dt}|_{u=1} > 0, para\ el\ SBLB\ PFC\ \lim_{S=0^-}\frac{dS}{dt}|_{u=1} = \lim_{S=0^-}\frac{v_{in}}{L} > 0 \tag{5}$$

$$\lim_{S=0^+}\frac{dS}{dt}|_{u=0} < 0, para\ el\ SBLB\ PFC\ \lim_{S=0^+}\frac{dS}{dt}|_{u=0} = \lim_{S=0^+}\left(\frac{v_{in}}{L} - \frac{v_o}{L}\right) < 0 \tag{6}$$

$$\left.\frac{dS}{dt}\right|_{u=u_{eq}} = \frac{v_{in}}{L} - \frac{v_o}{L}(1-u_{eq}) = 0, \qquad donde\ u_{eq} = 1 - \frac{v_{in}}{v_o} \tag{7}$$

$$\frac{dv_o}{dt} = -\frac{v_o}{R_LC} + \frac{2(v_o^{*})^2}{R_LC\ v_o}\ y\ \frac{di_{in}}{dt} = 0 \tag{8}$$

Modulador por banda de histéresis adaptativa

Este artículo propone el siguiente procedimiento de cálculo de la función del modulador por banda de histéresis adaptativa mostrado en la Fig. 1. El modulador es usado para generar la señal u que acciona a Q_1 y Q_2. La Fig. 2 muestra la representación geométrica de la Banda de Histéresis ($HB=\Delta i_{in}/2$) adaptativa propuesta en términos de la amplitud del rizado (Δi_{in}) de i_{in}. La banda adaptativa permite la operación con $f_{sw}=1/T_{sw}=1/(T_{on}+T_{off})$ constante, donde T_{sw} es el periodo de conmutación, T_{on} y T_{off} son el tiempo de apertura y de cierre de los interruptores respectivamente.

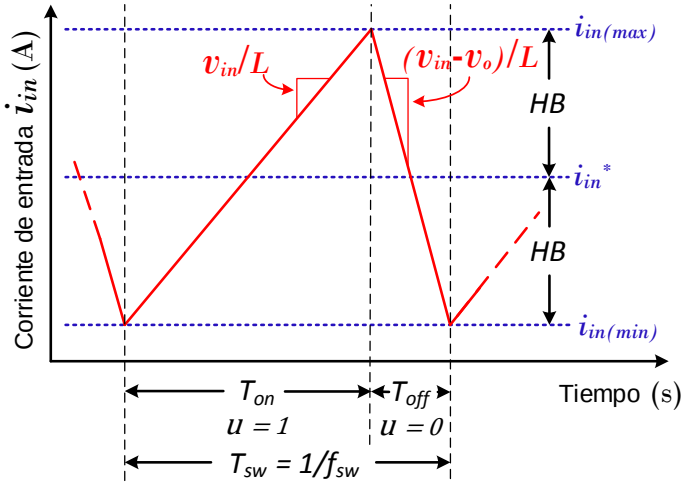

Fig. 2: Representación geométrica de la banda de histéresis adaptativa.

En el cálculo de HB, se asume que los cambios de i_{in} respecto al tiempo son lineales ($di_{in}/dt=\Delta i_{in}/\Delta t$). Durante la operación del SBLB PFC, Q_1 y Q_2 están cerrados incrementando la magnitud de i_{in} hasta alcanzar el límite superior ($i_{in(max)}$) de HB; por otro lado, i_{in} está decreciendo cuando Q_1 y Q_2 están abiertos mientras se alcanza el límite inferior ($i_{in(min)}$) de HB. La ecuación (9) se obtiene al reemplazar u=1 en la ecuación (1), donde $v_{in}=V|\sin(\omega t)|$ debido a la acción rectificadora del convertidor, v_0 es el voltaje regulado en la salida y V es la amplitud de v_{in}. La ecuación (10) se obtiene al reemplazar u=0 (interruptores abiertos) en la ecuación (1).

$$\frac{\Delta i_{in}}{\Delta t} \cong \frac{v_{in}}{L} = \frac{\Delta i_{in}}{T_{on}} \ , donde\ T_{on} = L\frac{\Delta i_{in}}{v_{in}} \tag{9}$$

$$\frac{\Delta i_{in}}{\Delta t} \cong \frac{v_0 - v_{in}}{L} = \frac{\Delta i_{in}}{T_{off}} \ , donde\ T_{off} = L\frac{\Delta i_{in}}{v_0 - v_{in}} \tag{10}$$

La ecuación (11) se obtiene al sustituir T_{on} (ecuación 9) y T_{off} (ecuación (10)) en $f_{sw}=1/(T_{on}+T_{off})$.

$$\Delta i_{in} = \frac{v_{in}\,(v_o - v_{in})}{L f_{sw} v_o} \tag{11}$$

La ecuación (12) presenta la banda de histéresis adaptativa propuesta en este artículo que puede ser obtenida reemplazando la ecuación (11) en $HB=\Delta i_{in}/2$.

$$HB = \frac{\Delta i_{in}}{2} = \frac{v_{in}\,(v_o - v_{in})}{2L f_{sw} v_o} = \frac{E|sin(\omega t)|\,(v_o - E|sin(\omega t)|)}{2L f_{sw} v_o} \tag{12}$$

El diagrama de bloques del modulador por histéresis con f_{sw} constante se muestra en la Fig. 3. La amplitud de HB se calcula con base en la ecuación (12) y los valores de v_0, v_{in}, f_{sw} y L. La señal resultante del cálculo es comparada con S y el resultado de la comparación es aplicado a las entradas de un flip-flop RS. Q_1 y Q_2 se abren cuando S es mayor que HB y se cierran cuando S es menor que HB, limitando la amplitud del rizado de i_{in} con la banda de histéresis adaptativa. La implementación de la banda de histéresis propuesta puede ser extendida a sistemas trifásicos; esto, debido a que la corriente de cada fase puede ser controlada siguiendo su propia banda de histéresis, teniendo en cuenta que la referencia a seguir por el control se construye con base en la señal de voltaje de su propia fase.

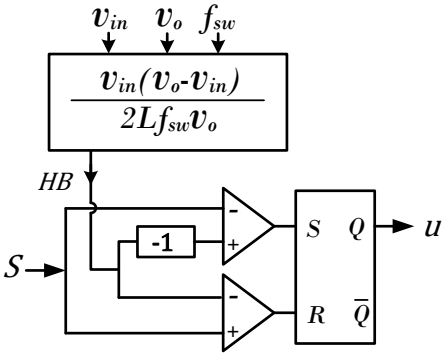

Fig. 3: Diagrama de bloques del modulador con banda de histéresis adaptativa.

RESULTADOS

El circuito SBLB PFC fue simulado en el software PSIM. La topología y el esquema de control se muestran en la Fig. 4. Los valores de los componentes y las especificaciones funcionales usados en la simulación del SBLB PFC se presentan en la Tabla 1. El objetivo de la simulación consiste en evaluar el desempeño de la banda de histéresis adaptativa propuesta en este artículo; por lo tanto, se presenta un análisis de las formas de onda de la corriente y el THD_i obtenido.

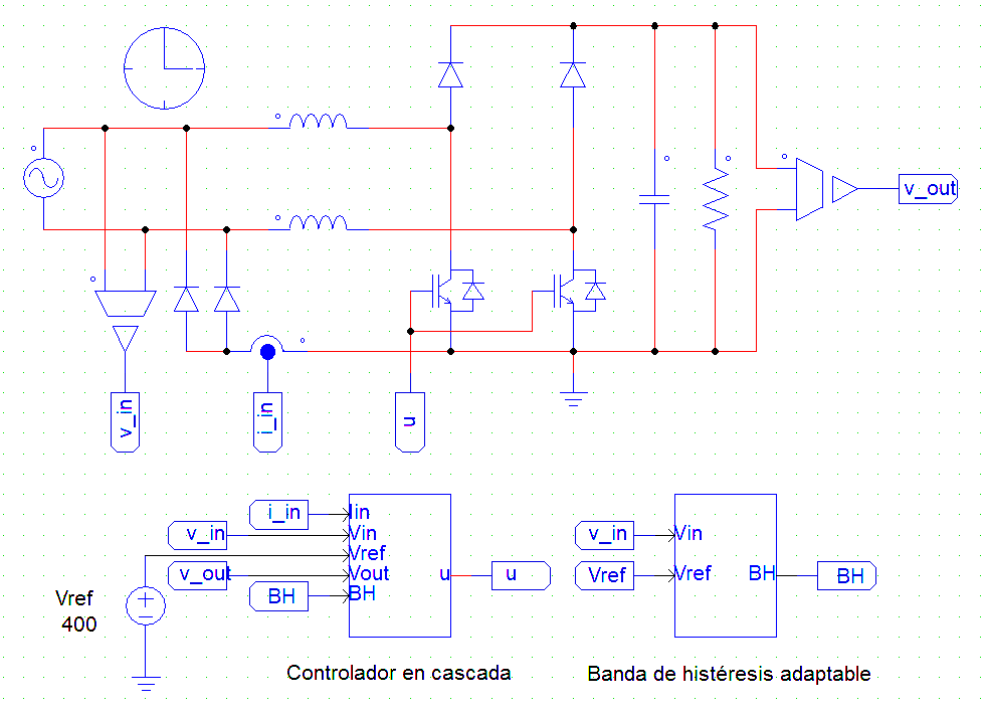

Fig. 4: Circuito del SBLB PFC simulado en PSIM.

Tabla 1: Especificaciones funcionales del SBLB PFC.

Símbolo	*Descripción*	*Valor*
v_{in}	Voltaje de entrada	84 V_{rms} hasta 120 V_{rms}
f_L	Frecuencia de la línea	60 Hz
V_0	Voltaje regulado en la salida	200 V_{dc} hasta 400 V_{dc}
$P_{out(max)}$	Potencia máxima de salida	1 Kw hasta 2 Kw
L_1- L_2	Inductores	2 mH
C	Condensador	2.5 mF
f_{sw}	Frecuencia de conmutación	40 KHz

Los resultados de simulación con v_{in}=169.7 V_{pico}, I=11.8 A_{pico}, V_0=400 v_{dc} y R_L=160 Ω demuestran el cumplimiento del balance de potencia (P_{in}=P_0= 1 kW) en estado estable, manteniendo el voltaje de salida alrededor de v_0*=400 Vdc con un rizado menor al 0.5%; sin embargo, el análisis presentado hace énfasis en los resultados obtenidos en la entrada del convertidor donde se evidencian las ventajas de la banda de histéresis adaptativa propuesta. Las formas de onda simuladas de i_{in} y v_{in} se comparan en la Fig. 5 donde i_{in} exhibe una forma de onda sinusoidal y en fase con v_{in}, alcanzando un PF=0.996.

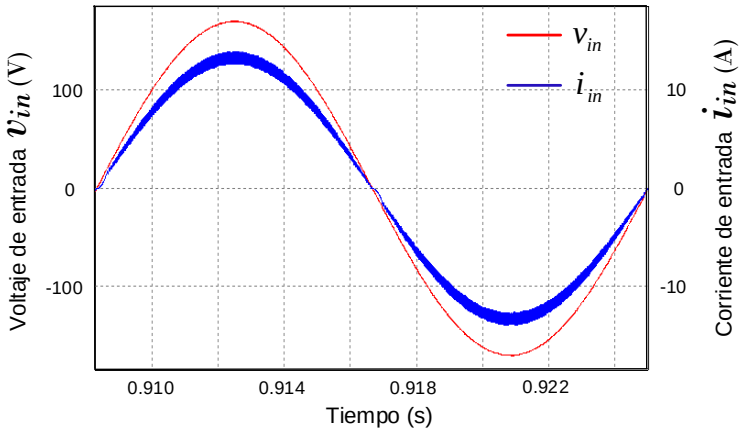

Fig. 5: Formas de onda de i_{in} y v_{in}.

La Fig. 6 muestra la forma de onda de i_{in} durante el cruce por cero. La simulación se realiza con P_0=1 kW, v_{in}=169.7 V_{pico} y v_{in}=120 V_{rms}. La Fig. 6a presenta a i_{in} cuando el control se realiza con banda de histéresis fija, i_{in} se deforma antes y después del cruce por cero, incrementando la THD_i hasta 13.3%. En contraste, la Fig. 6b presenta i_{in} cuando el control se realiza con banda de histéresis adaptativa propuesta. Esta banda de histéresis reduce la amplitud del rizado cerca del cruce por cero y el tiempo de estabilización de i_{in}; además, la banda de histéresis adaptativa reduce la deformación en i_{in} en el cruce por cero, haciendo que i_{in} alcance la señal de referencia por medio de una curva exponencial después del cruce por cero. Esta curva se produce debido a que la tasa de incremento de la corriente rectificada de la fuente es menor que la tasa de incremento de la señal de referencia i_{in}* en los primeros 12 µs. El SMC dirige a los estados del sistema para que se muevan hacía S después del cruce por cero, manteniendo cerrados Q_1 y Q_2. La amplitud y la duración de la curvatura tienen relación directa con el valor de L_1 y L_2.

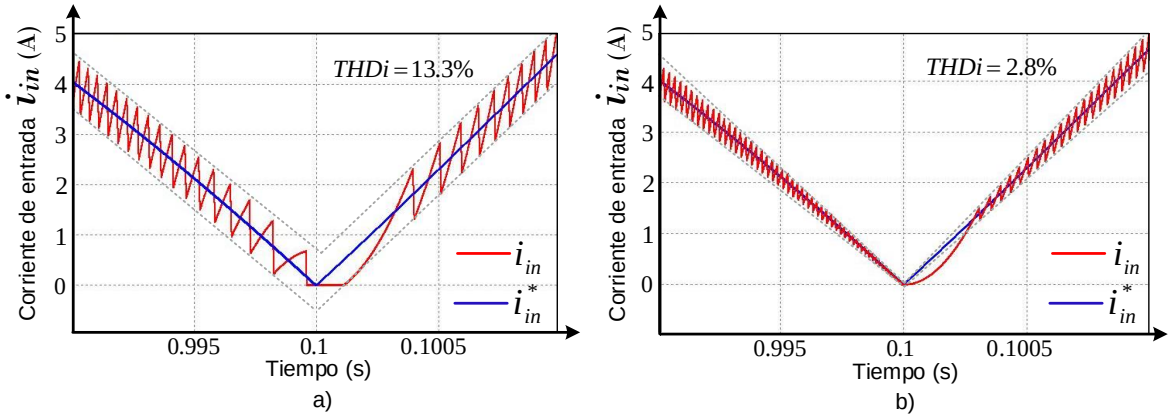

Fig. 6. Forma de onda de i_{in} durante el cruce por cero, usando: (a) banda de histéresis fija, y (b) banda de histéresis adaptativa.

La Fig. 7 muestra los resultados de la simulación del espectro en frecuencia de i_{in}. La Fig. 7a muestra el espectro con la amplitud de la banda de histéresis fija donde se puede observar una dispersión de la energía entre 60 Hz y 48 kHz con THD_i=13.3%. La Fig. 7b muestra el espectro con la banda de histéresis adaptativa propuesta donde se observa una concentración de la energía alrededor de la frecuencia fundamental de la red (60 Hz) y de la frecuencia de conmutación constante (40 kHz); razón por la cual, el THD_i se reduce hasta 2.8% manteniéndolo por debajo de los límites máximos permisibles del estándar EN/ IEC 61000-3-2 (1000-3-2).

El convertidor SBLB PFC es simulado con un incremento de carga del 200 % Para ilustrar la efectividad del SMC con la banda de histéresis propuesta para controlar la dinámica del sistema. La Fig. 8 muestra los resultados de la simulación cuando P_0 se incrementa desde 1 kW hasta 2 kW, manteniendo la amplitud de, v_{in} constante.

i_{in} se mantiene sinusoidal y en fase con v_{in}, garantizando la corrección del PF. El THD_i se mantiene constante en 2.8 % durante el tiempo de simulación. El controlador con la banda de histéresis adaptativa propuesta requiere ~ 87 ms (aproximadamente 5 ciclos de la red) para alcanzar la corriente de referencia necesaria para suministrar los 2 kW en la carga. El voltaje en la salida se estabiliza en ~ 345 ms (aproximadamente 21 ciclos de la red). La simulación muestra que el controlador con la banda de histéresis adaptativa propuesta permite reducir el THD_i, la deformación de la corriente en el cruce por cero y corregir el PF en presencia de cambios significativos de la región de operación.

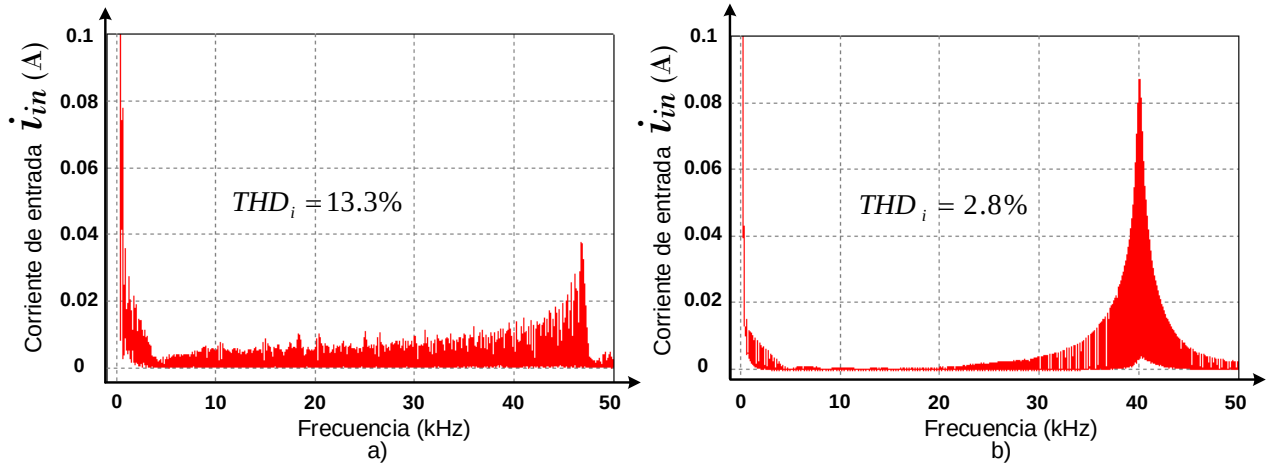

Fig. 7: Espectro de frecuencias de la corriente i_{in}: (a) banda de histéresis fija y (b) banda de histéresis adaptativa.

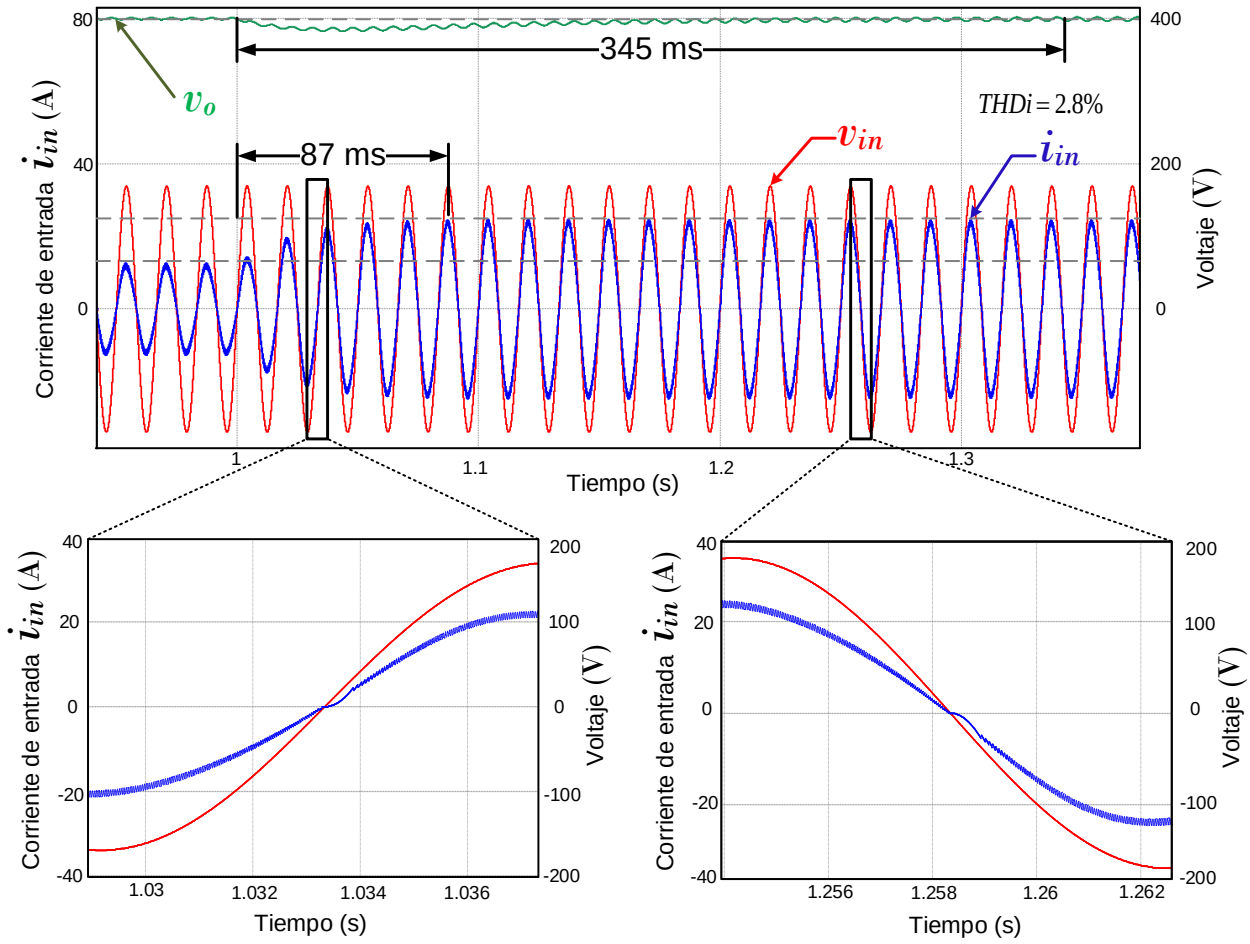

Fig. 8: Respuesta transitoria cuando la carga se incrementa desde 1 kW hasta 2 kW. La corriente se estabiliza aproximadamente en 5 ciclos de la red.

CONCLUSIONES

La banda de histéresis adaptativa propuesta en este artículo permite reducir el rizado, el THD_i y fijar la frecuencia de conmutación del SBLB PFC. Los resultados muestran que la señal de corriente en la entrada se mantiene en fase con el voltaje, garantizando un factor de potencia de 0.994. Además, la deformación de la corriente durante el cruce por cero de la señal es reducida en comparación con la deformación producida por la banda de histéresis de amplitud constante. El espectro en frecuencia de la señal de la corriente de entrada muestra la concentración de la energía alrededor de la frecuencia fundamental de la red y de la frecuencia de conmutación de 40 kHz del SBLB PFC cuando se usa la banda de histéresis adaptativa; en consecuencia, el THD_i es reducido de acuerdo al estándar EN/ IEC 61000-3-2 (1000-3-2).

La banda de histéresis adaptativa propuesta permite alcanzar los objetivos de control, evitando afectar la robustez, la regulación y la respuesta dinámica del SMC para todas las condiciones simuladas. El THD_i es reducido y el PF aumenta en presencia de cambios de carga de hasta el 200%, manteniendo la frecuencia de conmutación constante y la deformación de la señal baja en el cruce por cero.

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Article

A Sliding Surface for Controlling a Semi-Bridgeless Boost Converter with Power Factor Correction and Adaptive Hysteresis Band

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Abstract: This paper proposes a new sliding surface for controlling a Semi-Bridgeless Boost Converter (SBBC) which simultaneously includes Power Factor Correction (PFC) and DC bus regulation. The proposed sliding surface is composed of three terms: First, a normalized DC voltage error term for controlling DC bus and rejecting DC voltage disturbances, normalization was performed for increasing system robustness during start-up and large disturbances. Second, an AC current error term for implementing a PFC scheme and guarantying fast current stabilization during disturbances. Third, an integral of AC current error term for increasing the stability of the overall system. Also, an Adaptive Hysteresis Band (AHB) is implemented for keeping constant the switching frequency and reducing the THD_i. The proposed sliding surface was validated by means of sliding mode conditions and Lyapunov stability criteria. Simulations for comparing performance were performed between: a cascade PI control, a hybrid PI-Sliding Mode Control (PI-SMC), and Sliding Mode Control (SMC) with the proposed surface; additionally, it is presented an stability analysis for the proposed surface in start-up and under large perturbations. It is also presented experimental results for PI-SMC and SMC implemented in a SBBC prototype. The proposed surface implemented in the SMC presents the best dynamic behavior removing DC over voltages and responding faster under DC voltage changes or DC load current perturbations.

Keywords: sliding surface; Sliding Mode Control; Semi-Bridgeless Boost Converter; Adaptive Hysteresis Band; Power Factor Correction; non-linear control

1. Introduction

Many electrical devices as motors, computers and household appliances use passive rectifiers for supplying energy to DC loads. The rectifying action usually injects lower order harmonics which increases the Total Harmonic Current Distortion (THD_i), reduces the Power Factor (PF) and worsens energy quality of electrical grids [1–3]. For overcoming the problems related to passive rectifiers, active rectifiers are a good alternative [4,5], they are current-controlled rectifiers used to control the current in the AC side and provide a regulated DC voltage to load, their controllers are usually designed for keeping PF and THD_i into the admissible ranges (PF>0.9 and $THD_i < 5\%$) according to IEEE Std. 519 and IEC/EN 61000-3-2 [6,7].

Several active rectifiers with PFC-based on boost converter have been proposed to replace passive rectifiers [8–10]. Within these, SBBC is one of the promising topology due to stands out by reducing

the number of diodes in current path from source to load, decreasing the conduction power losses and improving efficiency. In addition, SBBC topology has two clamped diodes that connect the source to circuit ground which decreases common mode noise and electromagnetic interference [8,11,12]. Reasons why, SBBC topology was selected as the case of study of this paper.

SBCC controllers are usually based on classic cascade PI or linear controllers which has an external voltage loop and an inner current loop that uses Pulse Width Modulation (PWM) for generating the required control signals and activating power switches. However, this kind of controllers present over voltages at start-up which causes instability that affects sensitive loads [13] [10,14–17]. Particularly, [17] made a comparative analysis for PFC of several high efficiency AD/DC boost topologies. They showed that linear controllers allow obtaining high PFs and low THD_is; however, there are three issues to highlight: 1) DC voltage response has over peaks, 2) AC current stabilization time has a delay of several cycles in face of disturbances and load changes, and 3) AC current waveform near to zero crossing has distortion [9,11,14]. In general terms, linear PI controllers are designed around of an operating point which reduces the dynamic response in presence of large disturbances; besides, the dynamic performance of the controller is degraded when the region of operation of the converter moves away from the equilibrium point used in the design [8,11,13]. Large disturbances and extensive changes in the operation points are inherent to electric power systems, so sensitive loads are supremely affected [18]. For improving the response of power systems, it is desirable the use of non-linear controllers which fast response under disturbances and with high working range.

Sliding Mode Control (SMC) is a non-linear control strategy and it is a good alternative for controlling variable structure systems, as SBBCs. SMC improves the robustness against large and fast disturbances and it also reduces the sensitivity of the system to the variation of the parameters. also deals with uncertainty in modeling parameters. Moreover, SMC can directly provide the switching signals of power switches by means of hysteresis modulation; consequently, the dynamic response in closed loop is the fastest possible [19–24].

Following paragraphs have the purpose of showing the most relevant and recently papers related to SMC aplied to AC/DC converters, their contributions and some drawbacks are summarized.

In [12], authors proposed a SMC for a SBBC that allows reducing the injection of DC current into the power network, they used a hysteresis modulation; however, the hysteresis band amplitude is constant, obtaining a variable switching frequency which increases THD_i. Their sliding surface function consists on reducing the error between voltage and current waveforms, guarantying AC current and voltage in phase. SMC ensures current control for PFC when load is increasing up to 140%; however, DC voltage has variations up to 13% around of equilibrium point and it is observed a delay of several grid cycles for voltage stabilization. Basically, DC voltage was not considered in sliding surface design, hence, controller response is slow for DC bus regulation.

In [25], the authors made an analysis between integral and double integral SMC for the AC current error was done. Their sliding surface with an integral component presents low steady state error and high PF; however, the AC current has high THD_i. The sliding surface with double integral reduces steady state error and THD_i. Nonetheless, a DC current component appears. For this sliding surface, DC voltage dynamic was not considered.

In [26], it was implemented a hybrid PI-SMC for current error reduction. DC voltage is controlled by the external PI loop and DC voltage does not present over peak when load or source are disturbed or reference voltage is changed. Nevertheless, it is observed a slow response with delay of seconds for both AC current and DC voltage.

In [15], an AC/DC with hybrid PI-SMC for PFC was implemented, a genetic algorithm for obtaining sliding coefficients was presented. AC current and DC voltage errors were considered in the sliding surface design; nevertheless, DC voltage response has oscillations and high over voltages in presence of load disturbances due to the SMC response was limited by the linear controller. Otherwise, THD_i increases due to the significant distortion produced in the AC current near to the zero crossing.

In [23], an AC/DC converter based on totem-pole topology with an hybrid controller PI-SMC was implemented. In the sliding surface design, AC current and DC voltage errors were considered. An integral surface of AC current and DC voltage errors were also included, which reduces the steady state errors. They reached fast responses when AC current changes were incorporated; nevertheless, it was necessary an external limiter for protection of power switches; also, DC voltage presented over peaks due to the linear component of the controller.

In [18], an AC/DC converter with an hybrid PI-SMC controller and a PWM modulation for fixing switching frequency was presented. AC current and DC voltage with their corresponding integrative errors were considered. DC voltage presented oscillations with over peak up to 11% which was mitigated in several cycles of the source when load is changed, so that linear controller response is slow.

Main contribution of this paper is a new sliding surface for simultaneously DC voltage regulation and PFC, the proposed surface is composed of three terms which improves different aspects of the controller. The first one corresponds to a normalized DC voltage error term for removing DC voltage instability in start-up and in the presence of large disturbances due to the fact that the controller gives the priority to the current controller component which increases the robustness [27]. The second one corresponds to an AC current error term for implementing a PFC scheme and guarantying fast current stabilization during disturbances. The third one corresponds to an integral sliding term for the AC current error which increases the overall system stability and reduces the stable-state error in presence of load or source disturbances. We highlight that the proposed surface does not need an external PI loop; in consequence, the proposed sliding surface gives a response without over peaks or oscillations and provides fast DC voltage stabilization.

Another contribution is the implementation of an adaptive hysteresis band to fix the switching frequency according to the system dynamic which improves current waveform in zero crossing and reduces THD_i. The proposed adaptive hysteresis band does not need PWM signals; hence, the SMC responds fast while robustness is not reduced.

This paper is organized as follows: Section 2 corresponds to the SMC design which includes transversality and existence conditions, equivalent control and Lyapunov stability criteria. Section 3 describes the controllers implemented in this paper: PI control, PI-SMC and SMC. Additionally, for PI-SMC and SMC, it is described the AHB. Section 4 are the simulation results which includes a comparative analysis of the control schemes and a detailed analysis of the proposed sliding surface illustrating its effectiveness. Section 5 are the experimental results that demonstrate the effectiveness of the proposed SMC. Section 6 are the conclusions.

2. Sliding Mode Control Design

In this section, the mathematical procedure for the SMC design is detailed step by step: 1) first step consists on obtaining the SBBC mathematical model, 2) second step corresponds to the description of the proposed sliding surface for DC voltage regulation and PFC. 3) third step is the validation of the transversality condition, 4) fourth step is the validation of existence condition. 5) fifth step is the validation of equivalent control condition to evaluate SBBC under ideal control conditions. 6) Sixth step is validation of hitting condition with Lyapunov stability criteria to ensure stability in start-up.

Control objectives are: 1) to control the waveform of AC current, keeping it sinusoidal and in phase with AC voltage for PFC; 2) to control the amplitude of the AC current ripple near to zero crossing in order to reduce the THD_i; and 3) to regulate DC voltage according to the load requirements.

2.1. First step: SBBC mathematical modelling

Figure 1 corresponds to the SBBC topology with clamped diodes. This topology has two inductors L_1 and L_2 (where it is assumed $L_1 = L_2 = L$), four diodes D_1, D_2, D_3 and D_4, two power switches Q_1 and Q_2, and a capacitor C. The AC source is denoted by $(v_s = V_s sin(wt))$ while DC load is the resistor R. L_1, Q_1 and D_1 operate in the positive semi-cycle while L_2, Q_2 and D_2 operate in the negative

semi-cycle. SBBC can be modelled as a boost converter for each semi-cycle and switches actuates with the control signal $(u)(u = 1$ for switches closed and $u = 0$ for switches open). Mathematical model (Equations (1) and (2)) is obtained using Kirchhoff laws for both switching states. Equation (1) represents output voltage (v_o) dynamic (DC voltage) and Equation (2) describes the dynamic behavior of AC current (i_s) (AC current). For more details concerning to operation principle and deduction of equations please consult [28].

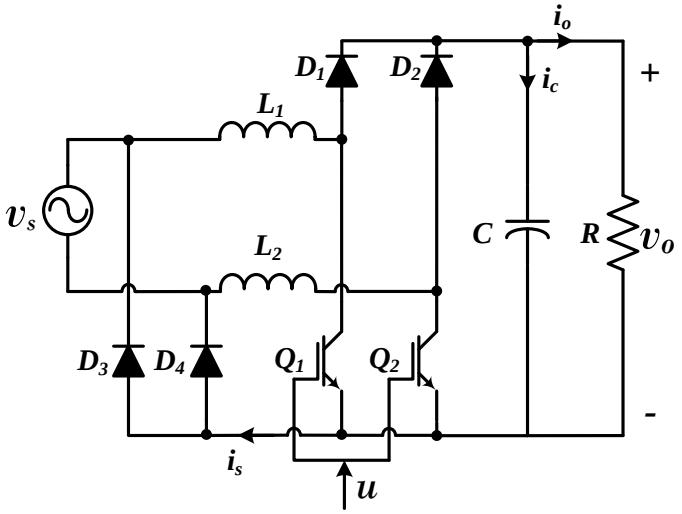


Figure 1. Topology SBBC with clamped diodes.

$$\frac{dv_o}{dt} = -\frac{v_o}{RC} + (1-u)\frac{i_s}{C} \tag{1}$$

$$\frac{di_s}{dt} = \frac{v_s}{L} - (1-u)\frac{v_o}{L} \tag{2}$$

2.2. Second step: sliding surface proposal

The sliding surface (S) proposed in this paper (Equation (3)) is composed by S_1, S_2 and S_3 terms. S_1 corresponds to the normalized DC voltage error [27] where V_{ref} is the desired DC voltage and α_1 is the sliding coefficient, which allows to adjust DC voltage dynamics response. S_2 corresponds to AC current error where reference current i_{ref} (Equation (4)) is a rectified sinusoidal signal and I_{ref} is its amplitude. I_{ref} is deduced by using a power balance $(P = v_s i_{ref} = V_{ref} i_o)$. S_3 corresponds to the integral of AC current error used to increase system stability. Sliding coefficients corresponding to current α_2 and α_3 are set in 1 $(\alpha_2 = \alpha_3 = 1)$ due to the fact that DC voltage was normalized and α_1 value is set to handle the priority between AC current and DC voltage terms in S.

$$S = \underbrace{-\alpha_1 \left(\frac{v_o}{V_{ref}} - 1\right)}_{S_1} + \underbrace{\alpha_2 (i_{ref} - i_s)}_{S_2} + \underbrace{\alpha_3 \int (i_s - i_{ref}) dt}_{S_3} \tag{3}$$

$$i_{ref} = \underbrace{\left(\frac{V_{ref} v_o}{R V_s sin^2(wt)}\right)}_{I_{ref}} |sin(wt)| \tag{4}$$

Equation (3) can be expressed as (5), using $x_1 = (v_o/V_{ref} - 1)$ as the normalized DC voltage error and $x_2 = i_s - i_{ref}$ as the AC current error. In the same way, Equations (1) and (2) are rewritten in function of errors, being Equations (6) and (7) representation of DC voltage error and AC current

error dynamics, respectively. Equation 8 represents the reference current time variation (di_{ref}/dt). Equations (7) and (8) can be combined for deducing the dynamics of current error in (9).

$$S = -\alpha x_1 - x_2 + \int x_2 dt \tag{5}$$

$$\frac{dx_1}{dt} = \frac{(1-u)(x_2 + i_{ref})}{CV_{ref}} - \frac{(x_1+1)}{RC} \tag{6}$$

$$\frac{dx_2}{dt} = \frac{v_s}{L} - \frac{V_{ref}(1-u)(x_1+1)}{L} - \frac{di_{ref}}{dt} \tag{7}$$

$$\frac{di_{ref}}{dt} = \underbrace{\left(\frac{V_{ref}|sin(wt)|}{RV_s sin^2(wt)}\right)}_{\gamma_1}\frac{dx_1}{dt} - \underbrace{\left(\frac{V_{ref} w cos(wt)}{RV_s sin(wt)|sin(wt)|}\right)}_{\gamma_2} V_{ref}(x_1+1) \tag{8}$$

$$\frac{dx_2}{dt} = \frac{v_s}{L} + \left(\frac{\gamma_1}{RCV_{ref}} + \gamma_2 - \frac{(1-u)}{L}\right) V_{ref}(x_1+1) - \frac{\gamma_1(1-u)(x_2+i_{ref})}{CV_{ref}} \tag{9}$$

2.3. Third step: validation of transversality condition

Transversality condition is evaluated according to Equation (10). Equation (11) represents $\dot{S}$ obtained by deriving Equation (5), while the solution for the transversality condition is expressed in Equation (12). Equation (12) gives the first restriction for α (Equation (13)) such that α range is limited by x_1 and x_2. Equation (14) must be fulfilled for ensuring that the SBBC can be controlled; this second restriction is obtained by evaluating (13) in the system boundaries and in steady state ($x_1 = x_2 = 0$ and $0 < i_{ref} < I_{ref}$).

$$\frac{d}{du}\left(\frac{dS}{dt}\right) \neq 0 \tag{10}$$

$$\frac{dS}{dt} = \dot{S} = -\alpha\frac{dx_1}{dt} - \frac{dx_2}{dt} + x_2 \tag{11}$$

$$\frac{d}{du}\left(\frac{dS}{dt}\right) = \left(\frac{\alpha}{V_{ref}} - \gamma_1\right)\frac{(x_2 + i_{ref})}{C} - \frac{(V_{ref}(x_1+1)}{L} \neq 0 \tag{12}$$

$$\alpha \neq \frac{CV_{ref}^2(x_1+1)}{L(x_2+i_{ref})} + \gamma_1 V_{ref} \tag{13}$$

$$\alpha < \left(\frac{C}{LI_{ref}} + \frac{1}{RV_s}\right) V_{ref}^2 \tag{14}$$

2.4. Fourth step: validation of existence condition

Existence condition $(S\dot{S} < 0)$ guarantees the existence of a sliding mode, the SBBC must remain into the sliding surface when $S \to 0$ (Equation (15)). Equation (16) presents the first existence condition when the system operates over the sliding surface and closed control signal ($u = 1$) is applied in order to follow the dynamic trajectories toward $S = 0$. Equation (17) gives the third restriction for α and it is obtained by evaluating Equation (16) in system boundaries and in steady state. Similarly, Equation (18) presents the second existence condition when system operates under the sliding surface and open control signal ($u = 0$) is applied in order to follow the dynamic trajectories toward $S = 0$. Equation (19) presents the load restriction obtained from Equation (18). Finally, Equation (20) corresponds to the control function defined ($u(S) = (1/2)(1 + sign(S))$) for guarantying the existence conditions .

$$\lim_{S=0^+} \frac{dS}{dt}|_{u=1} < 0 \quad \text{and} \quad \lim_{S=0^-} \frac{dS}{dt}|_{u=0} > 0 \tag{15}$$

$$\lim_{S=0^+} \frac{dS}{dt}|_{u=1} = (x_1+1)\left[\frac{\alpha}{RC} - \left(\frac{\gamma_1}{(RCV_{ref}} + \gamma_2 V_{ref}\right)\right] + x_2 - \frac{v_s}{L} < 0 \tag{16}$$

$$\alpha < \left(\frac{\gamma_1}{RCV_{ref}} + \gamma_2\right) V_{ref} + \frac{v_s}{L} \tag{17}$$

$$\lim_{S=0^-} \frac{dS}{dt}|_{u=0} = \frac{(\alpha-\gamma_1)}{C}\left(\frac{(x_1+1)}{R} - \frac{(x_2+i_{ref})}{V_{ref}}\right) + V_{ref}(x_1+1)\left(\frac{1}{L} - \gamma_2\right) > 0 \tag{18}$$

$$R > \frac{V_{ref}}{I_{ref}} \tag{19}$$

$$u(S) = \left\{ \begin{array}{lll} 1 & when & S > 0 \\ 0 & when & S < 0 \end{array} \right\} \tag{20}$$

Existence conditions ensure sliding mode, guarantying not only $S = 0$ but also $x_1 = x_2 = 0$; under these conditions the system remain controlled around of the equilibrium point.

2.5. Fifth step: validation of equivalent control

Equivalent control evaluates the system dynamics under ideal operation conditions, assuming infinite switching frequency and not taking into account time variation of the sliding surface ($\dot{S} = 0$). Equation (21) presents the equivalent control condition (u_{eq}) obtained from Equations (6), (9) and (11). Condition for ensuring equivalent control ($0 < u_{eq} < 1$) is presented in Equation (22) and corresponds to the fourth restriction for α ($\alpha < \gamma_1 V_{ref}$) evaluated in system boundaries. In this case, α is limited by the required power according to the desired set point of DC voltage ($\alpha < P_{ref}/V_s$). This restriction is more restrictive than transversality (14) and existence (17) restrictions, hence, this restriction contains the others.

$$u_{eq} = 1 - \underbrace{\frac{\left[\left(1 - \frac{1}{RC}\right)\gamma_1 + \frac{\alpha}{RCV_{ref}} + \gamma_2\right] V_{ref}(x_1+1) + (v_s/L) - (x_2+i_{ref})}{(V_{ref}/L)(x_1+1) + [(\alpha/V_{ref}) - \gamma_1](x_2+i_{ref})}}_{u'_{eq}} \tag{21}$$

$$\alpha < \frac{V_{ref}^2}{RV_s} \tag{22}$$

2.6. Sixth step: validation of hitting condition (Lyapunov stability criteria)

This condition evaluates the system convergence through Lyapunov stability criteria regardless of initial conditions. The energy Lyapunov function to evaluate is $V = (1/2)x_1^2$ [15], therefore, restriction to satisfies is $\dot{V} = x_1\dot{x}_1 < 0$. First condition for applying Lyapunov is $S = 0$ and it is obtained x_2 in function of x_1 (Equation 23) with γ_3 and γ_4 as auxiliary variables. γ_3 and γ_4 are associated with the integral term of S (S_3) taking into account i_s and i_{ref} dynamics. Also, please note that logarithm attenuates S_3 for high error values and introduces a dynamic sliding surface which depends on time.

$$x_2 = -\left(\alpha + \underbrace{\frac{V_{ref}^2}{wRV_s} \ln\left|tan\frac{wt}{2}\right|}_{\gamma_3}\right) x_1 - \left(\underbrace{\gamma_1 + \frac{I_s}{w} cos(wt)}_{\gamma_4}\right) \tag{23}$$

Equation (24) presents the Lyapunov restriction obtained after replacing Equations (21) and (23) into Equation (6). u'_{eq} in function of x_1 is defined in Equation (25). Condition to satisfy $\dot{V} = x_1\dot{x}_1 < 0$ is given in Equation (26) while α restriction is in Equation (27) ; please note that restriction of Equation (27) is the same that control equivalent restriction of Equation (22).

$$\dot{V} = -x_1\frac{[(\alpha+\gamma_3)x_1+\gamma_4-i_{ref}]u'_{eq}}{CV_{ref}} - x_1\frac{(x_1+1)}{RC} \tag{24}$$

$$u'_{eq} = \frac{A(x_1+1)+(v_s/L)+[(\alpha+\gamma_3)x_1+\gamma_4-i_{ref}]}{(V_{ref}/L)(x_1+1)-(\alpha/V_{ref}-\gamma_3)[(\alpha+\gamma_3)x_1+\gamma_4-i_{ref}]} \tag{25}$$

$$x_1 > \frac{(\alpha-\gamma_4V_{ref})(I_{ref}-\gamma_4)L+V_{ref}^2}{(\alpha-\gamma_3V_{ref})(\alpha+\gamma_3)L-V_{ref}^2} \tag{26}$$

$$\alpha < \frac{V_{ref}^2}{RV_s} \tag{27}$$

The system is asymptotically stable along the sliding surface (S_1, S_2 and S_3) according to existence condition and second Lyapunov stability theorem, considering the load restriction (Equation (19)) and sliding coefficient limits (Equation (28)).

$$0 < \alpha < \frac{V_{ref}^2)}{RV_s} \tag{28}$$

Finally, Equation (29) presents the x_1 open loop response in function of x_2 obtained for solving Equations (1) and (2) when $u = 1$ and the initial conditions ($t = 0$, $i_s = 0$, $v_o = V_{ini}$). This equation presents the limits for x_1 when $V_{ini} = 0$ ($x_1 = -1$) and $V_{ini} = V_{ref}$ ($x_1 \to 0$) (depending of SBBC parameters and x_2), so x_1 is bounded ($-1 < x_1 < 0$). Therefore, the sliding surface proposed in this paper presents stability for the SBBC DC voltage with or without Bus DC pre-charge.

$$x_1 = \frac{V_{ini}}{V_{ref}}e^{-\frac{1}{wRC}cos^{-1}[1-\frac{wL}{V_s}(x_2+i_{ref})]} - 1 \tag{29}$$

3. Control Schemes

Figure 2 presents the SBBC control system. Voltage waveform for obtaining the reference waveform of AC current is taken from the feeding source (electrical grid) by means of phase locked loop (PLL). Control system takes measured of v_s, i_s, v_o and i_o signals from SBBC. v_o and i_o are filtered to remove high frequency noise. Finally, the controller calculates the control actions and generates the u signal to trigger the power switches Q_1 and Q_2.

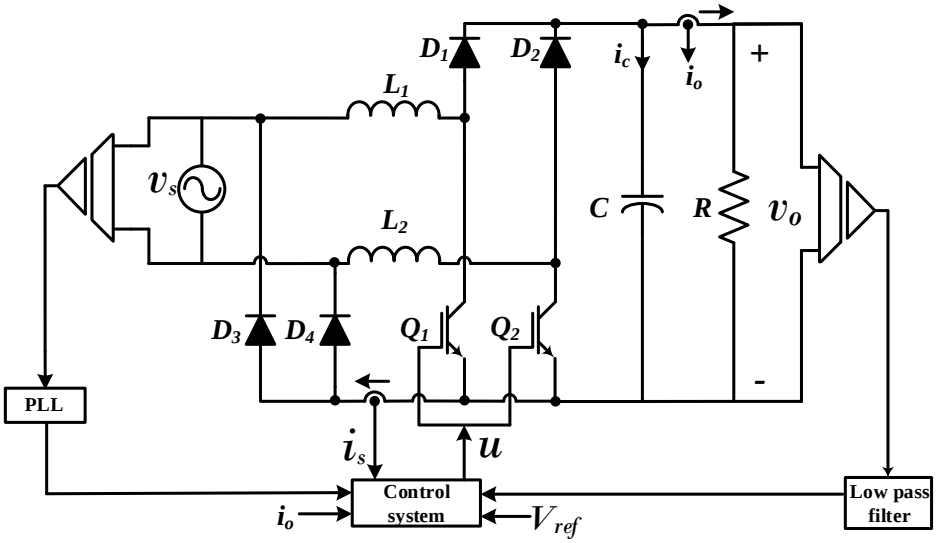


Figure 2. Control system for SBBC.

There were evaluated three control strategies: PI, hybrid PI-SMC and the proposed SMC; please see Figure 3. Classical cascade PI controller is shown in Figure 3a. The external voltage loop gives the AC current amplitude reference to internal current loop and current controller actuates by means of PWM generator. Control Scheme of hybrid PI-SMC is presented in Figure 3b; in this case, there is an external PI control loop for DC voltage regulation and gives the reference AC current amplitude for the internal SMC; voltage error is considered by the SMC and adaptive hysteresis band is used instead PWM generator. The proposed SBBC control with SMC is presented in Figure 3c; this system allows controlling both DC voltage and AC current; reference current is obtained from power balance and adaptive hysteresis band gives the control signal. The proposed sliding surface is used in both hybrid PI-SMC and SMC controllers in order to analyze their advantages and limitations.

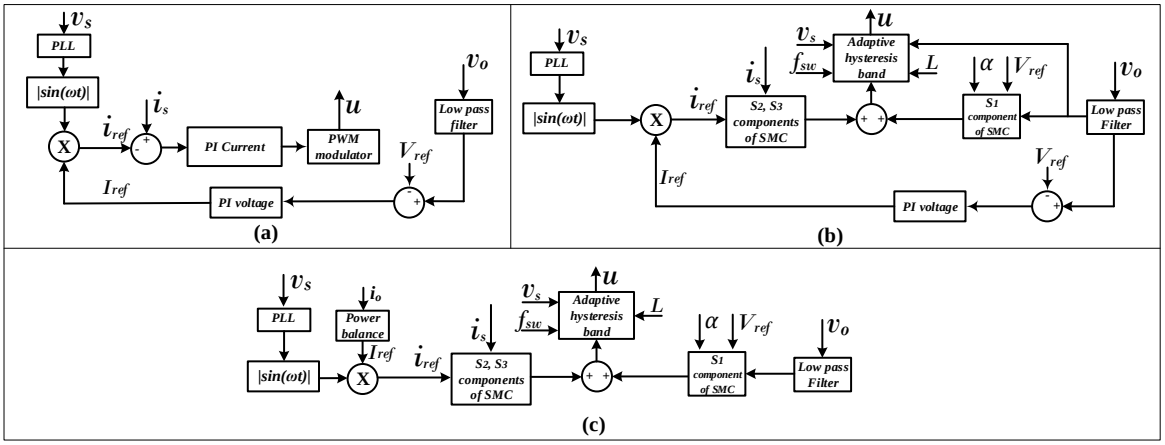


Figure 3. Block diagram of control system: a) classical cascade PI controller, b) hybrid PI-SMC and c) proposed SMC.

AHB is designed based on current ripple geometry according to [29]. AHB has two functions; first, to smooth the current zero crossing in order to decrease THD_i; second, to modify the switching time according to SBBC operation point in order to fix the switching frequency. Equation (30) presents the AHB in function of v_o, v_s, L and f_{sw}, while its implementation is in Figure 4. AHB calculated for each point is compared with the sliding surface. Finally, the control signal is given by a RS flip-flop.

The AHB does not require PWM signals for actuating over power switches; in consequence, sliding mode control does not have any delay in its AC current response.

$$AHB = \frac{v_s(v_o - v_s)}{2Lf_{sw}v_o} \tag{30}$$

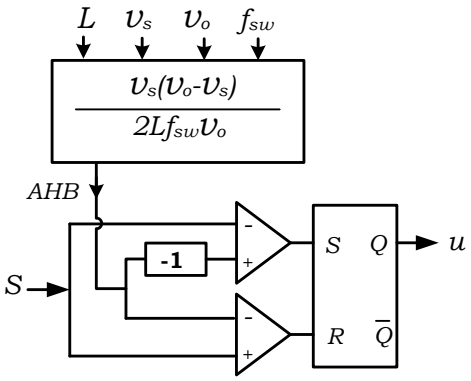


Figure 4. Adaptative hysteresis band modulator.

4. Simulation Results

The proposed surface and its control was performed in PSIM computer simulation software. The comparative analysis for PI, hybrid SMC-PI and the proposed SMC control strategies is presented in section 4.1 while the surface dynamic behavior at start-up is discussed in section 4.2. Values of the system parameters are given in table 1. Control parameters used in simulations are $K_p = 0.2, K_i = 0.8$ (for PI control) and $\alpha = 150$ (for SMC).

Table 1. Simulation parameters.

Parameter	Value
Grid voltage $(v_s = v_{in})$	120 $Vrms$
Grid frequency (f)	60 Hz
DC bus capacitor (C)	2.2 mF
DC bus voltage $(V_o = V_{ref})$	400 V
Inductors $(L_1 = L_2 = L)$	2.2 mH
Switching frequency (f_{sw})	40 kHz
Rated power (P_o)	500 W
Rated Load (R)	320 Ω

4.1. Comparative Analysis for PI, PI-SMC and SMC

Effect of load increasing on SBBC performance with PI, PI-SMC and the proposed SMC controllers are analyzed. In this simulation, DC power in load is incremented from 250W to 500kW. Figure 5 allows comparing the AC current stabilization time for the three controllers. AC current with PI controller exhibits a stabilization time of 32.4 ms, this control system has a delay between measurement and switching signal degrading significantly the waveform near to zero crossing and presenting a THD_i of 17.23% (Figure 5a). For PI-SMC, hysteresis modulation strategy improves the waveform near the zero crossing of current, reducing the THD_i to 3.85% (Figure 5b); nevertheless, current stabilization (amplitude) is reached two cycles later if it is compared with the PI controller. Finally, The proposed SMC allows regulating AC current, rapidly responding to operation changes in only 0.04 ms. In this case, it can be observed that the current response is the fastest possible (Figure 5c). If is possible to concluded that SMC and the use of an ABH allows decreasing the THD_i to 3.7% and rapidly responds under perturbations.

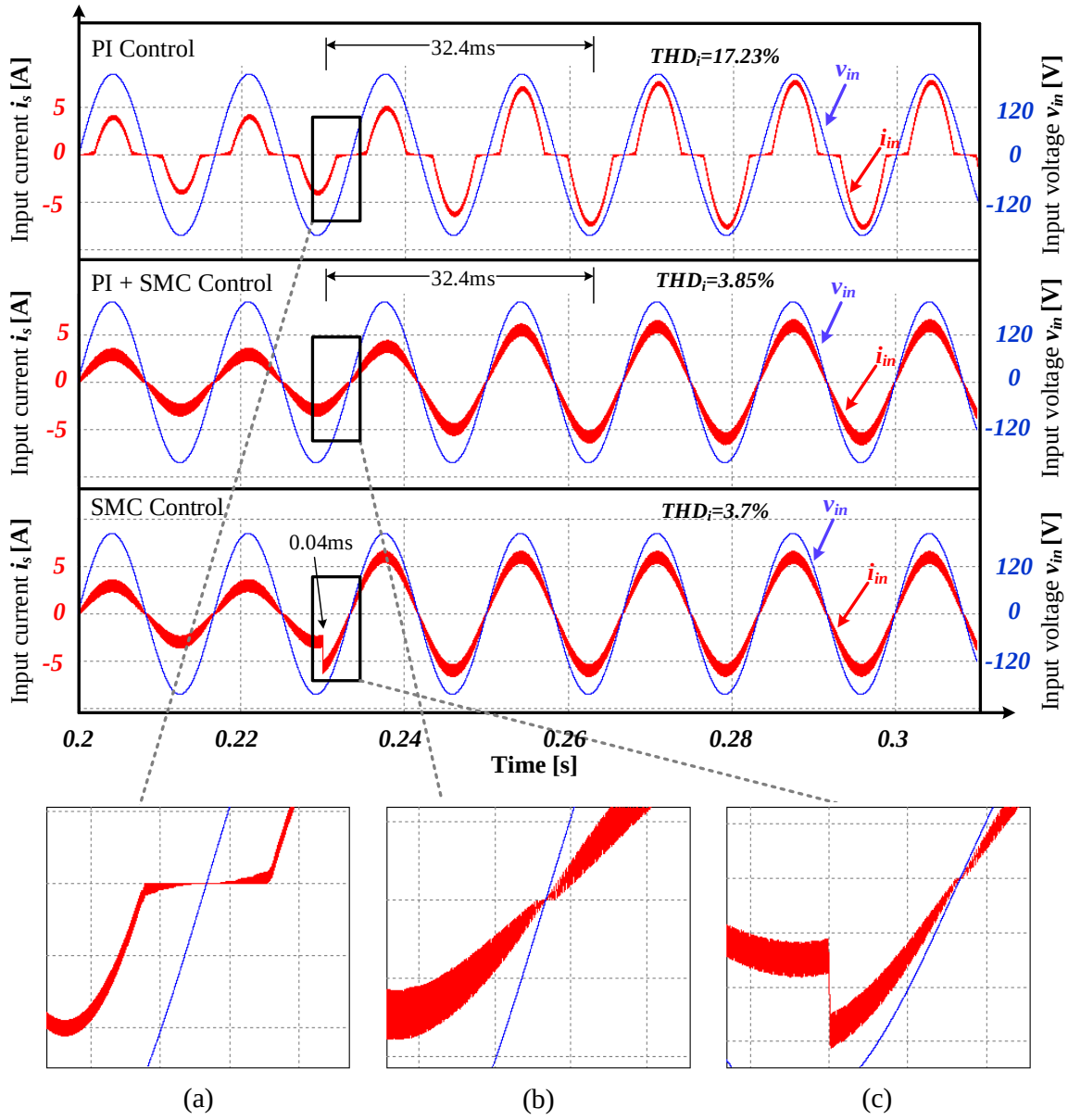


Figure 5. AC current performance of (a) PI control , (b) PI-SMC, and (c) the proposed SMC.

Figure 6 shows DC voltage response. The power converter with PI control (Figure 6a) takes 395.7 ms to regulate DC voltage and presents an over voltage of 12.75%. In comparison, PI-SMC allows reducing the over voltage to 3.75%, maintaining the same stabilization time than PI control (Figure 6b). This result evidences the delay caused by PI control when it is used as external loop, limiting the transient response of the closed loop system. On the other hand, DC voltage stabilizes in 30 ms, when the SMC strategy is used and the response exhibits a low over voltage of 0.1% (Figure 6c). This evidences that SMC rapid responses and protects sensitive DC loads against over voltages.

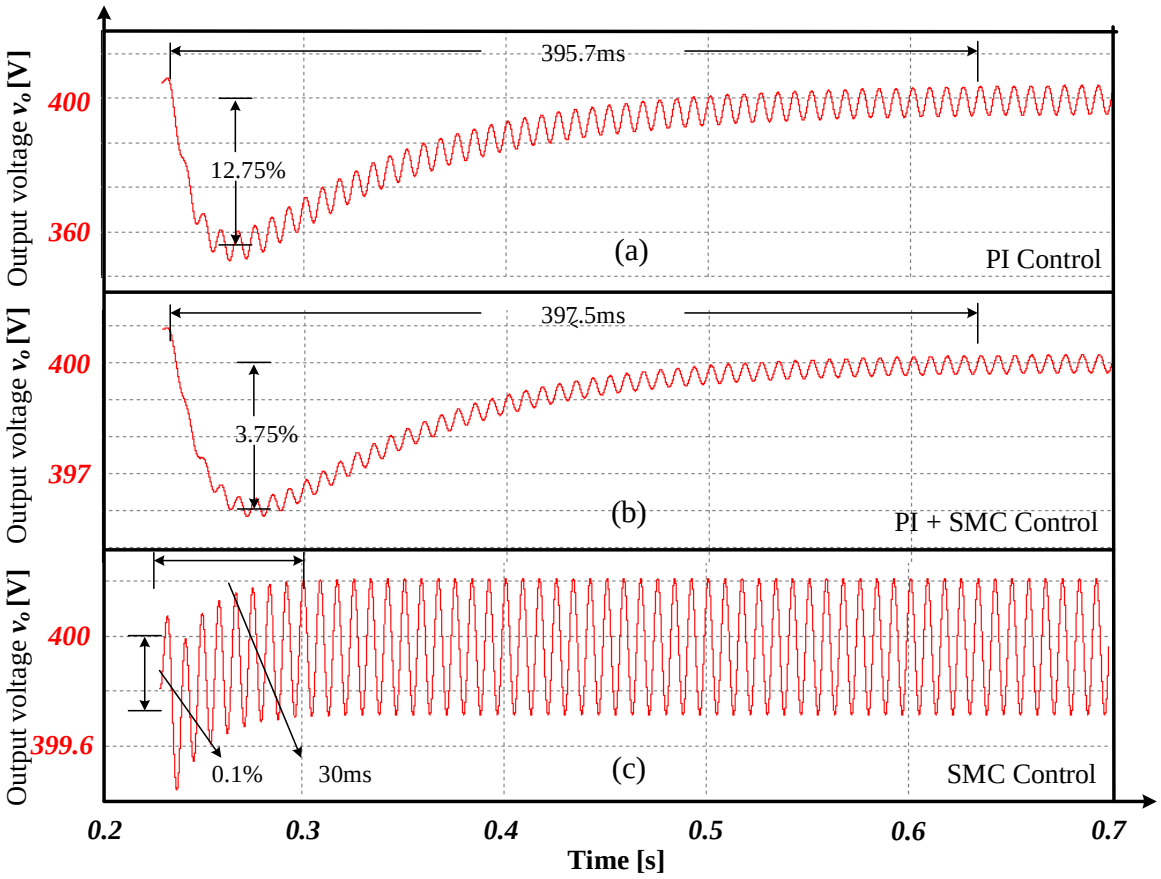


Figure 6. DC voltage transient response when the load increases from 250W to 500W, comparing the performance of (a) PI control , (b) PI-SMC , and (c) SMC .

Integrative Absolute-value Error (IAE) was obtained in order to quantify the dynamic behavior of controllers PI and SMC. Integral was calculated for 200000 points taken from PSIM since start-up until 0.2 sec; each value was normalized with $V_o = 400V$ due to the fact that in start-up error begin in 400 for each controller. IAE for SMC is $9.6217x10^3$ and IAE for PI control is $1.0924x10^4$. IAE index presents SMC behavior a 12% better than cascade PI controller.

4.2. Sliding Mode Control Behavior

This section has the purpose of showing the stability of SMC, forcing the system to work in adverse conditions that is the start-up without including a pre-charge of DC bus or under large perturbations.

Behavior of DC voltage in SBBC start-up is presented in Figure 7. Figure 7a shows DC voltage without DC-bus pre-charge. DC voltage does not present instability or over peaks and increases to remain around of the stabilization point $(400V)$ in 1.52 seconds. Stabilization time can be modified by means of the sliding coefficient depending on desired priority order, increasing or decreasing the response time for DC voltage or AC current. Figure 7b presents the behavior of normalized DC voltage error (S_1), at begin, voltage error is bounded by its minimum value (-1). Therefore; S_1, at start-up according to the sliding coefficient value, is $(S_1 = -150)$; then, S_1 rapidly reaches the convergence point (stabilization point) and keeps sliding around of $S_1 = 0$.

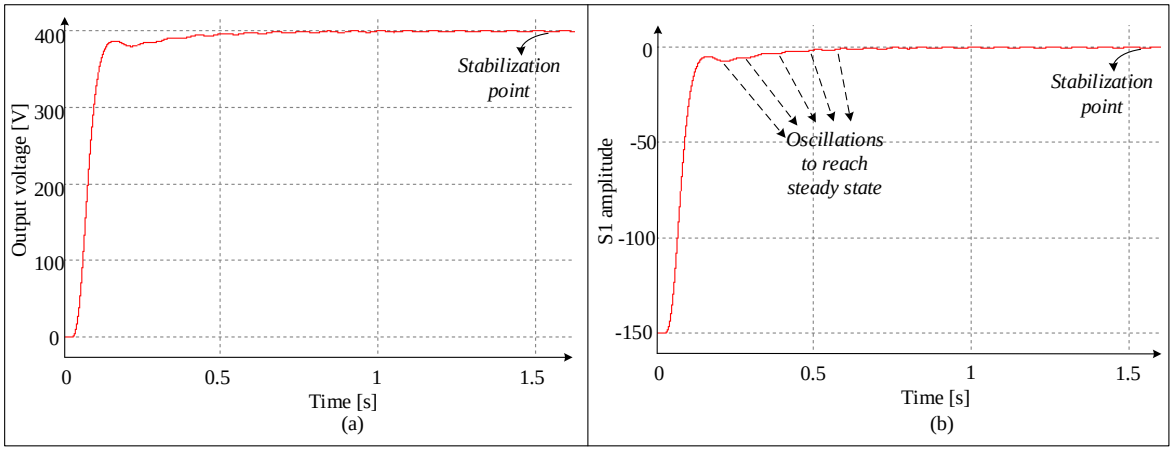


Figure 7. DC voltage behavior in start-up: (a) DC voltage and (b) DC voltage error S_1.

Behavior of AC current in SBBC in start-up is presented in Figure 8. It is observed in Figure 8a a transient with an over peak near to 15 times the desired value; nevertheless, the over peak is only presented for the first half cycle of the wave and AC current rapidly stabilizes in a sinusoidal wave in the second grid cycle while zero crossing deformation is gradually reduced in four cycles. Figure 8b presents the behavior of AC current error (S_2). At beginning, S_2 has also a couple of large transient oscillations, then magnitude of oscillations are significantly reduced being only evident for the first zero crossings. Finally, S_2 reaches the convergence zone oscillating near to the equilibrium point in the adaptive hysteresis band.

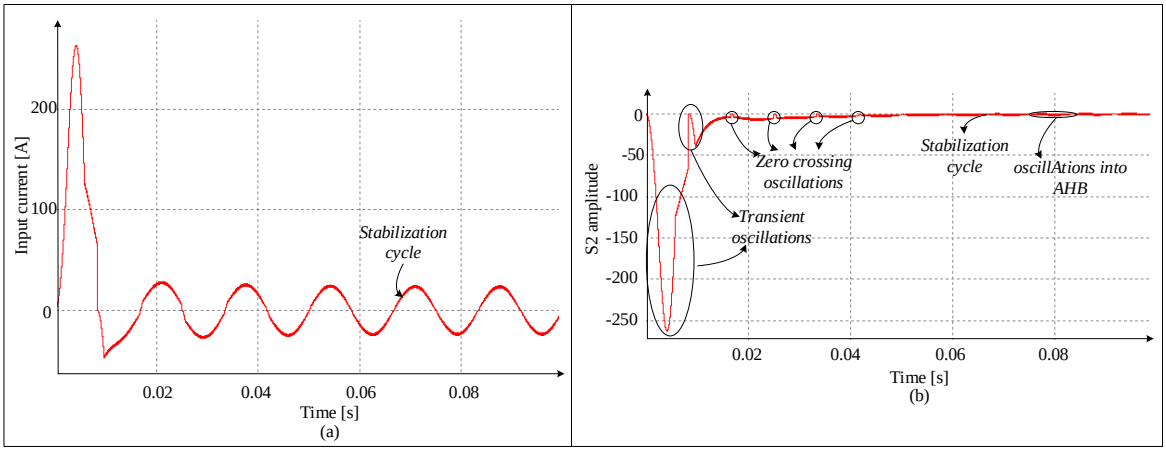


Figure 8. AC current behavior in start-up: (a) AC current and (b) AC current error S_2.

Behavior of S_3 is in start-up presented in Figure 9, being reset each period of the grid for setting in zero the accumulative error that is inherently produced in integral systems. S_3 begins in zero and immediately decreases near to -1.2 for the first peak, then it increases again and reaches the convergence zone around $S_3 = 0$. Stabilization of DC voltage and AC current as well as convergence to zero of its errors (including integral) in SBBC start-up demonstrate stability for the proposed sliding surface outside of operation zone (hitting condition and Lyapunov criteria).

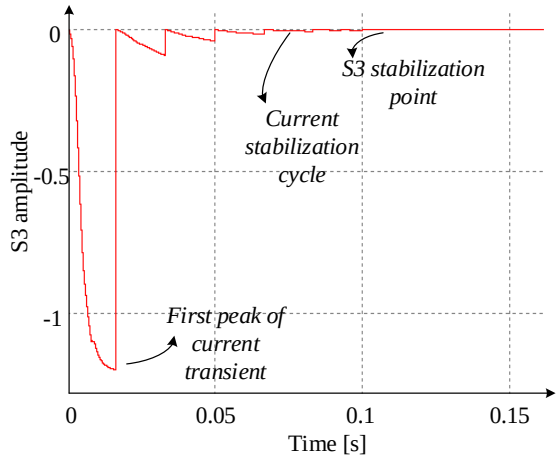


Figure 9. Integral of current error in start-up.

Sliding surface dynamic behavior when a disturbance appears is shown in Figure 10, the disturbance corresponds to an increasing to twice of DC load current. Figure 10 presents the sliding surface limited by the AHB in half-cycle of the AC voltage. In this case, the system is forced to be above of the upper AHB, it is observed that the SMC response immediately conducts the system into AHB which validates the hitting condition. Concerning to the existence condition, AHB limits speed in the response, fixing the switching frequency in $40kHz$ and forcing the system to be sliding around of $S = 0$.

In addition, note that at the beginning and end of each half-cycle during zero crossings, the system is also out of the AHB. This is due to polarity of AC current changes, putting the system out of the AHB. Under this situation, SMC reacts and rapidly brings the system back into the AHB which significantly reduce the THD_i produced in zero crossings.

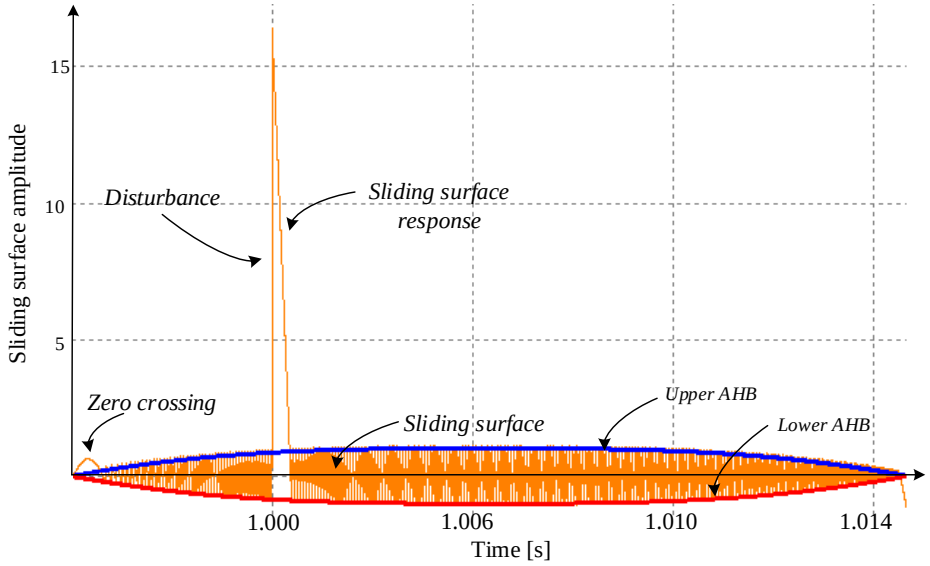


Figure 10. Sliding surface response for load increase.

Figure 11 shows the frequency spectrum of AC current, using the proposed SMC. The energy is concentrated near to the fundamental frequency (60Hz) and the switching frequency (40kHz); in this case, THD_i is 3.7%.

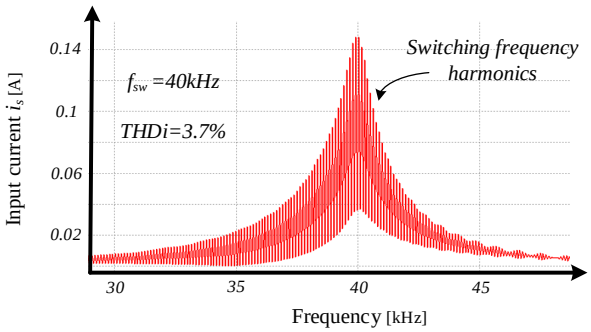


Figure 11. Frequency spectrum of the AC current using the adaptive hysteresis band.

5. Experimental Results

This section presents the experimental results when hybrid PI-SMC (Section 5.1) and the proposed SMC (Section 5.2) controllers are implemented in a SBBC. Cascade PI control was not considered due to this control was presented in numerous previous works and the simulations show that the this controller has the worst performance. Section 5.3 shows a zero crossing comparison between PI-SMC and SMC.

SBBC implementation is presented in Figure 12. This prototype is mainly composed of: 1) AC supply terminals and protection system. 2) Microcontroller Printed Circuit Board (PCB) used for signal processing and control. 3) Measurement PCBs for measuring AC voltage, AC current and DC voltage. 4) EMI filter for improving electromagnetic compatibility. 5) Inductors L_1 and L_2 for coupling AC and DC systems. 6) Power switching PCB with power switches (IGBTs) and diodes. 7) DC bus for regulating DC voltage. SBBC Requirements and characteristics are the same than used in the simulation result section (table 1). It was used a Digital scope GW Instek GDS-2204A (200MHz Bandwidth, 4 Input Channel, 2GSa/s Real-time Sampling Rate, 2Mp Record Length) for collecting the experimental results. For validating the dynamic behavior under the control strategies, there were implemented changes in the set point of DC voltage and in DC current (perturbation in the load).

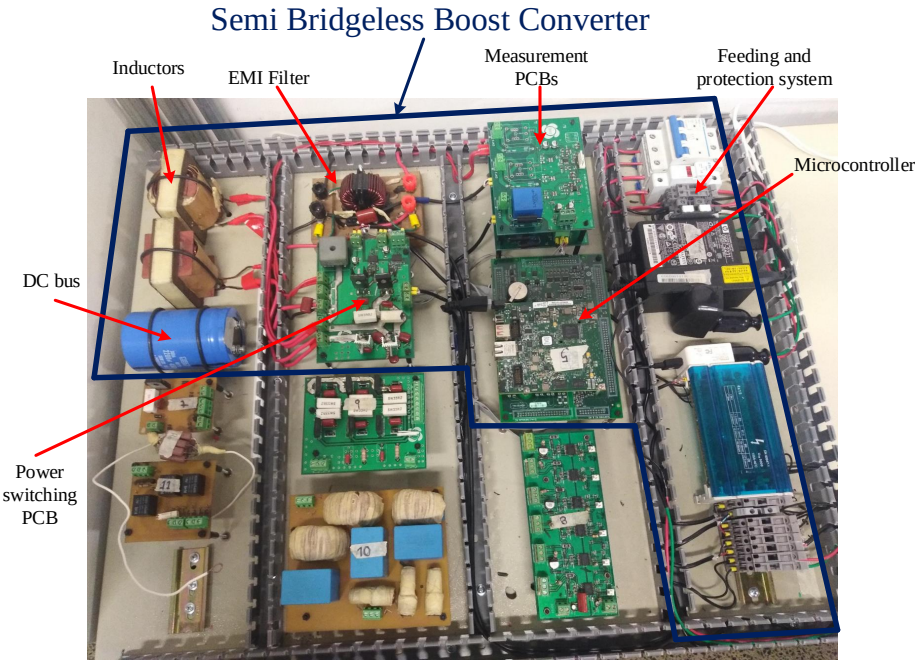


Figure 12. Semi Bridgeless Boost Converter for experimental test.

5.1. Results for PI-SMC controller

Figure 13 are the results when the set point of DC voltage is changed. Initially, set point of DC voltage was set in $400V$ and a change of $20V$ was made, reducing DC voltage from $400V$ to $380V$ as it can be seen in Figure 13a. Then, DC voltage set point was incremented, increasing DC voltage from $380V$ to $400V$ (Figure 13b). In both cases, DC voltage presents a stabilization time of 1.3 seconds with over voltage around of the stabilization point; also, current amplitude slightly changes; however, controller keeps AC current and voltage in phase, ensuring PF close to 1.

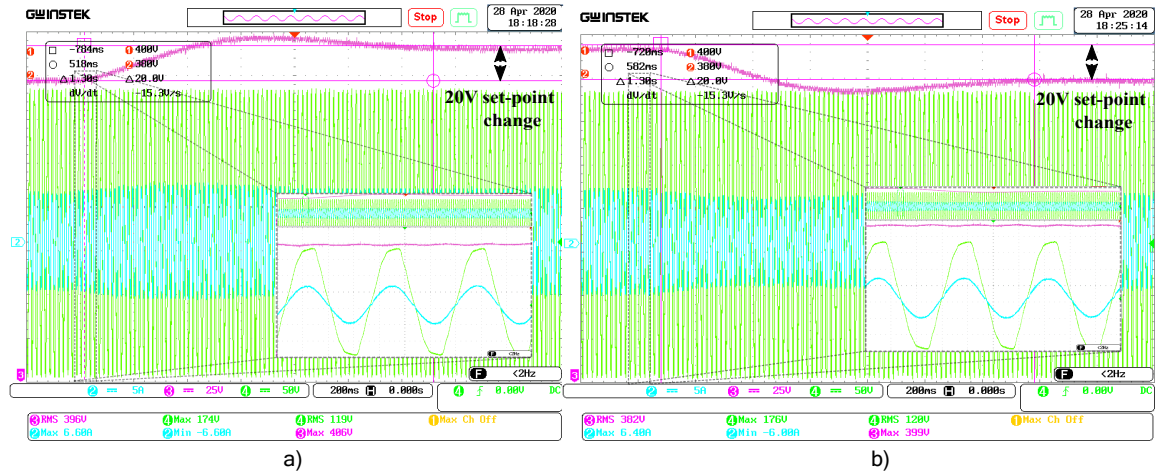


Figure 13. Experimental results with PI-SMC control for voltage set point changes: (a) DC voltage increases $20V$, (b) DC voltage decreases $20V$.

Figure 14 are the results when a load disturbance is caused. Figure 14a presents results when load decreases a 25%. In this case, an over voltage of $22V$ and a DC voltage stabilization time of 2.9 seconds are observed. Figure 14b presents results when load increases 25%; SBBC presents a maximum oscillation of $18V$ and DC bus stabilizes at 1.53 seconds. In both tests, AC current has delay of several grid cycles for reaching the stabilization point.

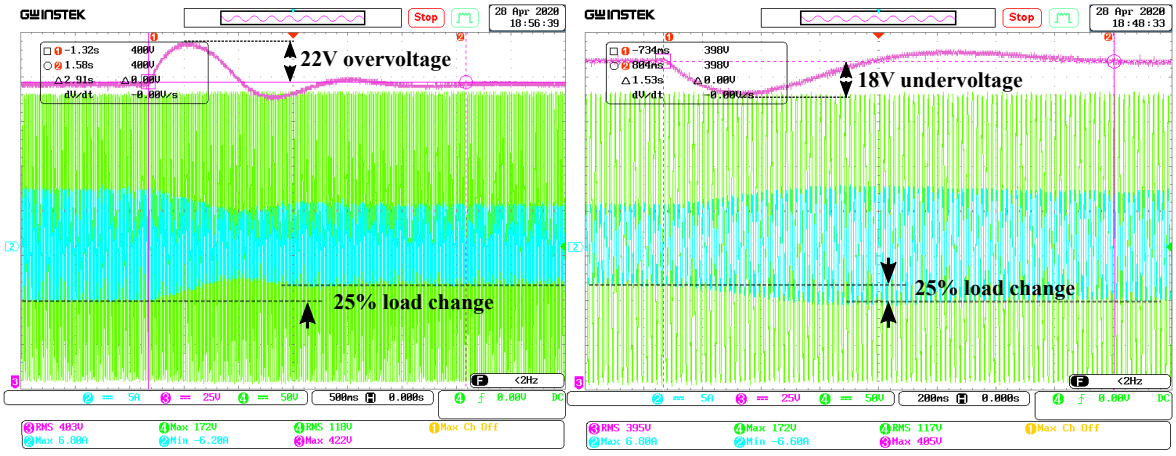


Figure 14. Experimental results with PI-SMC control for load changes: (a) load decreases 25%, (b) load increases 25%.

5.2. Results for the proposed SMC controller

Similarly to previous section, Figure 15 are the results when the set point of DC voltage is changed. Initially, set point of DC voltage was set in $400V$ and a change of $20V$ was made, reducing DC voltage from $400V$ to $380V$ as it can be seen in Figure 15a. Then, DC voltage set point was incremented, increasing DC voltage from $380V$ to $400V$ (Figure 15b). In both cases, DC voltage

presents a stabilization time of 1.55. In this case, DC voltage does not have any over voltage and PF is ensured close to 1. In addition, AC current amplitude is reached in only a half cycle after set point change; in contrast with PI-SMC control in which AC current amplitude is get after several cycles.

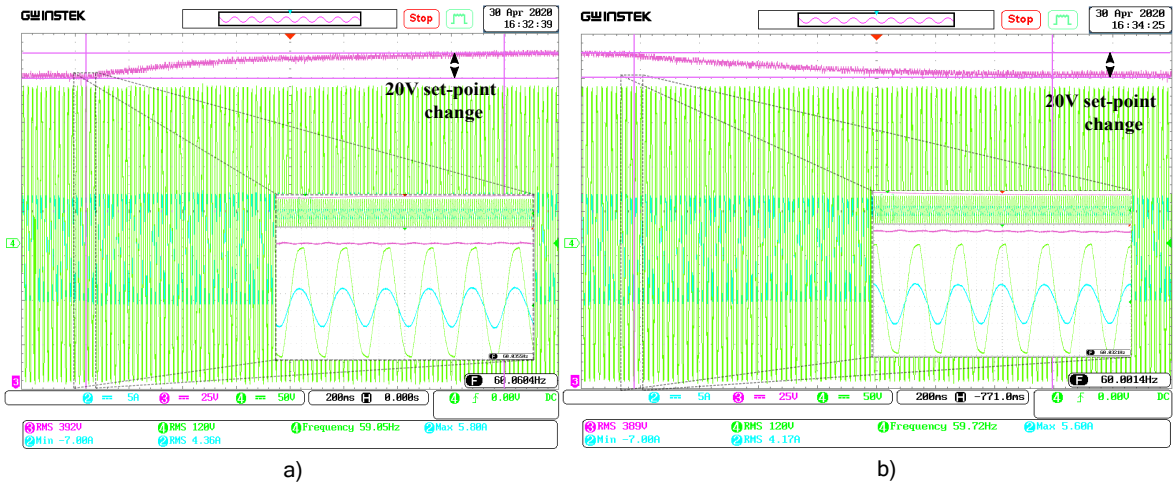


Figure 15. Experimental results with SMC for voltage set point changes: (a) DC voltage increases $20V$, (b) DC voltage decreases $20V$.

Figure 16 are the results when it is implemented perturbations in the load. Figure 16a presents results when load decreases a 50% while Figure 16b presents results when load increases 50%. In this case, DC voltage does not have any over voltage or oscillations around its set point. Also, SBBC instantaneously responds to load changes and current amplitude is reached in the next half-cycle. The proposed SMC control presents the fastest possible response, even when the load disturbance caused is twice as large as the load disturbance of PI-SMC control.

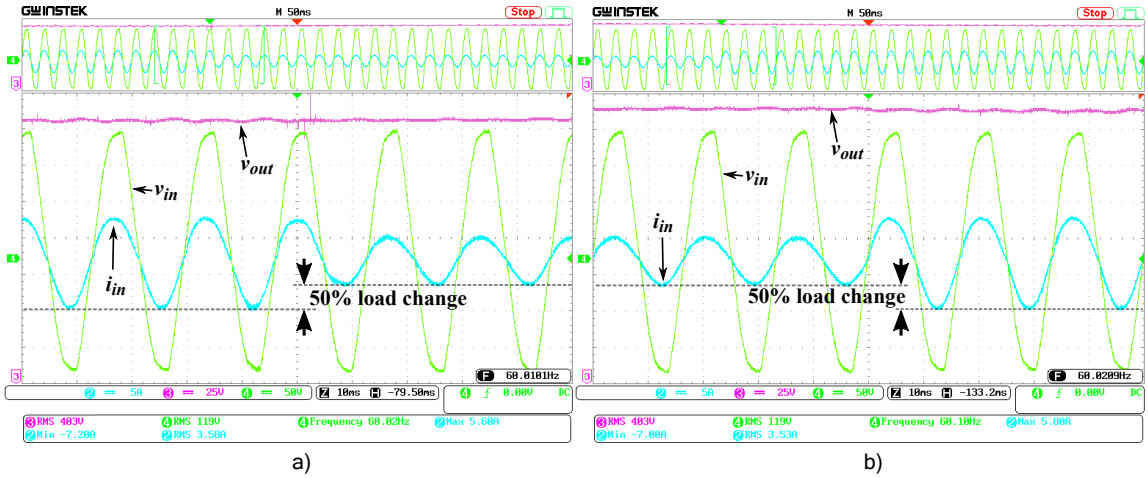
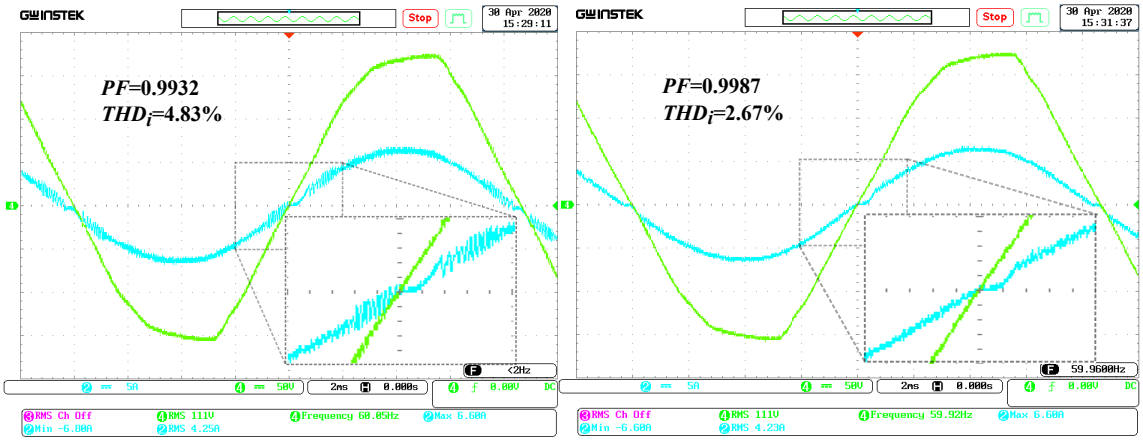


Figure 16. Experimental results with SMC for load changes: (a) load increases to 50%, (b) load decreases to 50%.

5.3. Zero crossing comparison

Finally, a zoom for AC current results was done in Figure 17 for the following two cases: (a) the PI-SMC with fixed hysteresis band, and (b) the SMC with the proposed adaptive hysteresis band. In Figure 17a, it is observed ripple increments just before and after the zero crossing obtaining a $THD_i = 4.83\%$. While in Figure 17b, zero crossing is softer than the zero crossing with fixed

hysteresis band, this approach represents a better performance during zero crossing and a reduction of $THD_i = 2.67\%$.



a) b)

Figure 17. Zero crossing of AC current: (a) PI-SMC control, (b) SMC control.

6. Conclusions

This paper proposed a new sliding surface for controlling a SBBC which simultaneously incorporates Power Factor Correction (PFC) and DC bus regulation. The proposed sliding surface is composed of 1) a normalized DC voltage error term, 2) an AC current error term, and 3) an integral of AC current error term. The surface was validated using sliding mode conditions, Lyapunov stability criteria and experimental tests. The surface was implemented for PI-SMC and SMC and AHB was used for fixing the switching frequency and reducing THD_i.

Simulations results were performed for comparing three controllers: Cascade PI, PI-SMC and SMC in terms of their dynamic behavior. When applied a DC power change of 250W (50%), it was found that SMC presented the best performance due DC voltage presents the lowest stabilization time ($30ms$) and practically does not present over voltage (0.1%) which guaranties the protection of sensitive loads. Also, AC current has the fastest time response ($0.04ms$) (almost instantaneous) and presents the best behavior in zero crossings which reduces THD_i (3.7%). IAE index was obtained for SMC and PI controllers, demonstrating that SMC is 12% better than PI control.

There were also made simulations concerning to the behaviour of the proposed sliding surface using SMC in start-up and without including a pre-charge of DC bus, forcing the system to work for adverse conditions. SMC control adequately responds without DC over voltages, stabilizing the AC current for the first half cycle of the wave despite the large over current in start-up. In these simulations, it was evidence the stability of SBBC when it is implemented SMC.

Experimental results were implemented for PI-SMC and SMC. It was implemented changes in the set-point of DC voltage and in DC load current. SBBC responds better under changes and perturbations despite of perturbations for SMC were more severe than perturbations for PI-SMC. Finally, zero crossing comparison shows a better behavior for SMC working with AHB which demonstrates the rapid response of SMC under instantaneous sign changes of the sliding surface.

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Conflicts of Interest: The authors declare that they have no conflict of interest.

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Other paper related with this master research are: 1) Unified method for teaching how to solve the equivalent circuit of transformers; this paper is published in journal “Revista espacios”. Power electronics devices need an electrical grid coupling, this link generally is done with transformers. Also, AC/DC converters can be modeled as transformers and this paper presents a procedure to obtain transformer variables in steady state. Main variables to considered for AC/DC converters and transformers are voltages, currents, powers, losses, efficiency and sequence group. 2) Power Loss Minimization for Transformers Connected in Parallel with Taps Based on Power Chargeability Balance; this paper is published in journal “energies” (category Q1). This paper uses an optimization method to set taps of transformers in parallel connection. In this master research work, the sliding coefficients are were set according to behavior in simulation, nevertheless, an optimization method as genetic algorithm can be used for a future research work.

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Unified method for teaching how to solve the equivalent circuit of transformers

Método unificado para enseñar a resolver el circuito equivalente de transformadores

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Contents

ABSTRACT:
In this paper, a unified method for calculating variables and parameters of transformers considering power losses in their windings is proposed. This method presents an educational tool for teaching how to obtain the steady-state operating conditions of transformers used to make technical and economic decisions. Five variants are considered in calculations using single-phase, three-phase or per-unit (p.u) equations. This method is validated by calculations and simulations (ATPDraw); also, an on-line PYTHON graphic interface was implemented.
Keywords: Transformers, solution method, simplified model, education

RESUMEN:
En este artículo se propone un método unificado para calcular las variables y parámetros de transformadores considerando pérdidas de potencia en sus devanados. Este método presenta una herramienta educativa para enseñar a obtener las condiciones operativas de transformadores en estado-estable usadas para tomar decisiones técnicas y económicas. Se consideran cinco variantes para los cálculos usando ecuaciones monofásicas, trifásicas y por-unidad (p.u). Este método se valida con cálculos y simulaciones (ATPDraw); además, se implementó una interfaz gráfica on-line en PYTHON.
Palabras clave: Transformadores, método de solución, modelo simplificado, educación

1. Introduction

Transformers in electrical systems are used as a link between generation and transmission, as well as transmission and distribution, and distribution and final users. The main function of transformers in transmission systems consist on increasing the voltage magnitude for reducing electric losses in the lines. In distribution systems, transformers are commonly used for decreasing voltage magnitude up to operation levels and feeding electric devices minimizing security risks for people. In addition, transformers have windings with galvanic

isolation and power transference is given by means of electromagnetic induction, providing isolation between electrical systems; in consequence, the transformer protection is essential for electrical grids (Vahidi & Esmaeeli, 2013), (Varan & Yurtsever, 2017). Transformers are also used for improving power quality, controlling angle-phase (Thompson, Miller, & Burger, 2008), starting motors (Huan, Xiangrui, & Guangzhe, 2012), and filtering third order and zero sequence harmonics (Ionescu, Paltanea, & Paltanea, 2013), (Hurng-Liahng, Kuen-Der, Jinn-Chang, & Wen-Jung, 2008).

Network operators need to know transformers operating conditions due to technical and economic reasons (Xiao-pin, Yi-yi, Yue, & Bin, 2014), (Georgilakis & Amoiralis, 2010). Transformer variables such as feeding voltage, output voltage, currents and load data are used in reliability studies, overload voltage regulation, disconnections and circuit transferences (Yazdani-Asrami, Mirzaie, & Shayegani Akmal, 2010). Hence, electrical engineers and students of electrical engineering need a methodology for learning how to find the transformer variables and parameters.

Generally, the conventional model is used for studying the transformer behavior in steady state (Jiale, Jiao, Song, & Kang, 2009). The conventional model is based on the transformer equivalent circuit where its windings are represented as inductors with resistances connected in series and the transformer core is represented as an inductor with a resistance connected in parallel. Nevertheless, the conventional model is modified according to the study to be done, for example: the high frequency model is formed adding to the conventional model the capacitive couplings between its windings. This model is used for designing transformers for isolation and voltage impulse tests (Nagy & Osama, 2010). The conventional model is combined with the transformer magnetic model for analyzing inrush currents in the magnetization branch (Abdulsalam, Xu, & Dinavahi, 2005). On the other hand, the conventional model is adapted to the RLC model when it is necessary to study transformer responses due to transient states (Hassan Hosseini, Vakilian, & Gharehpetian, 2008), (Yang, Wang, Cai, & Wang, 2011), (Celis-Montero, Castro-Aranda, & Martinez-Velasco, 2012), (Vahidi, Agheli, & Jazebi, 2012).

In this paper, the transformer solution method is deduced in steady state from a simplified model based on the conventional model. The main contribution of this paper consists on providing an educational tool for students of electrical engineering and electrical engineers regarding the solution of the transformer simplified model. The proposed solution allows obtaining voltages, currents, powers, power losses, efficiency, voltage regulation and power factor by means of nominal characteristics (transformer identification plate), test results (Ayasun & Nwankpa, 2006) and load connected. The proposed method has five variants: 1) single-phase solved from transformer primary side, 2) single-phase solved from transformer secondary side, 3) three-phase solved from transformer primary side, 4) three-phase solved from transformer secondary side and 5) per unit solution. Each variant can be applied according to the windings connection (wye or delta).

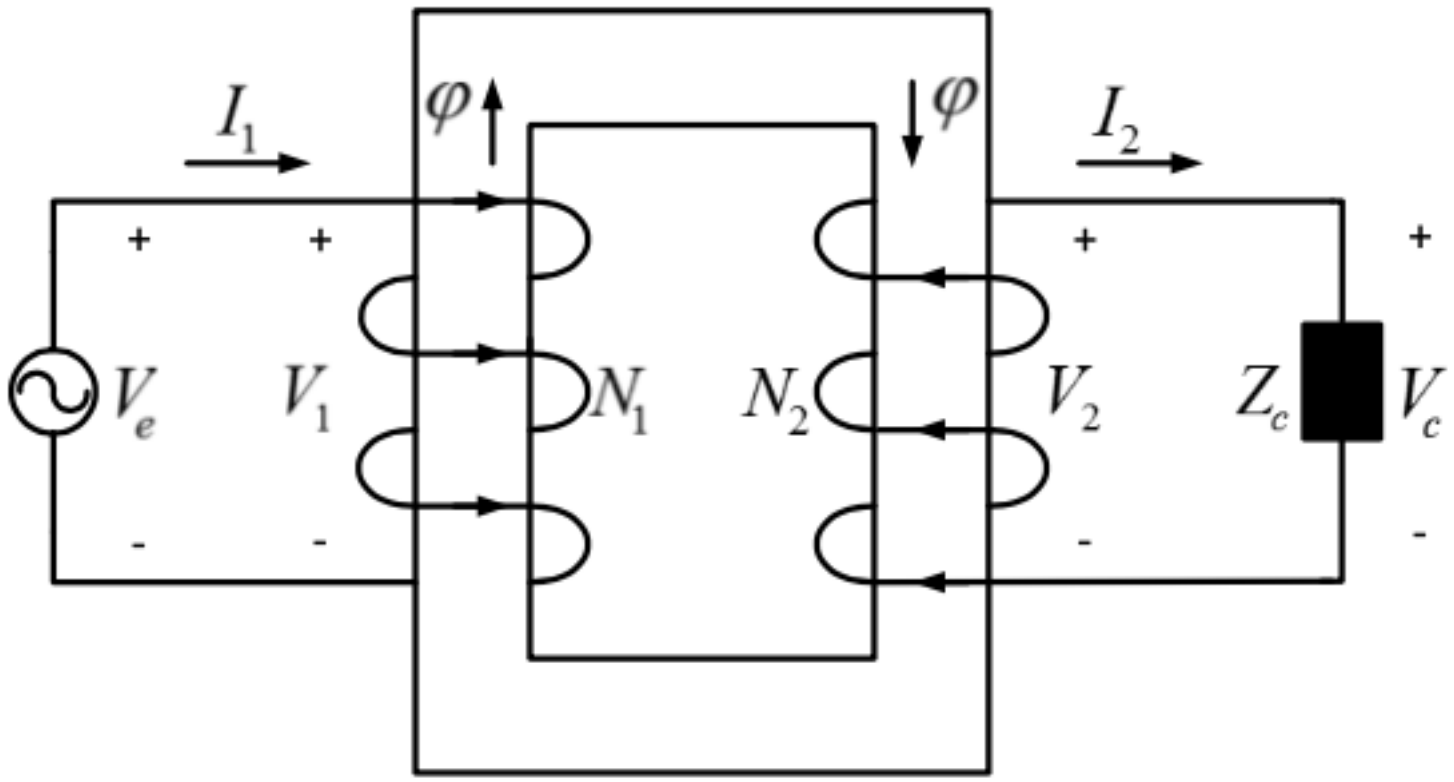
This paper is organized as follows: Section 1 presents the transformer conventional model based on power losses and the use of the simplified model is justified; in section 2, the solution method with its five variants is described; Section 3 presents the method validation through mathematical calculations and simulation in ATPDraw; in Section 4, the graphic interface for solving three-phase transformers is shown; finally, in section, 5 the most relevant conclusions and discussions are presented.

2. Methodology

2.1. Transformer ideal model

Figure 1 shows the transformer's ideal model where V_e is the feeding voltage while V_1 and N_1 are the induced voltage and the number of turns in the primary winding, respectively. Current I_1 circulates in the primary winding generating the flow (φ) in the transformer core. This flow induces a voltage V_2 in the secondary winding with N_2 number of turns. Current I_2 circulates in the secondary winding when the load Z_c is connected in its terminals and V_c is the voltage applied in the load. In the ideal model $V_e = V_1$ and $V_2 = V_c$; that is because power losses are not considered in the transformer windings.

Figure 1
Transformer's
ideal model

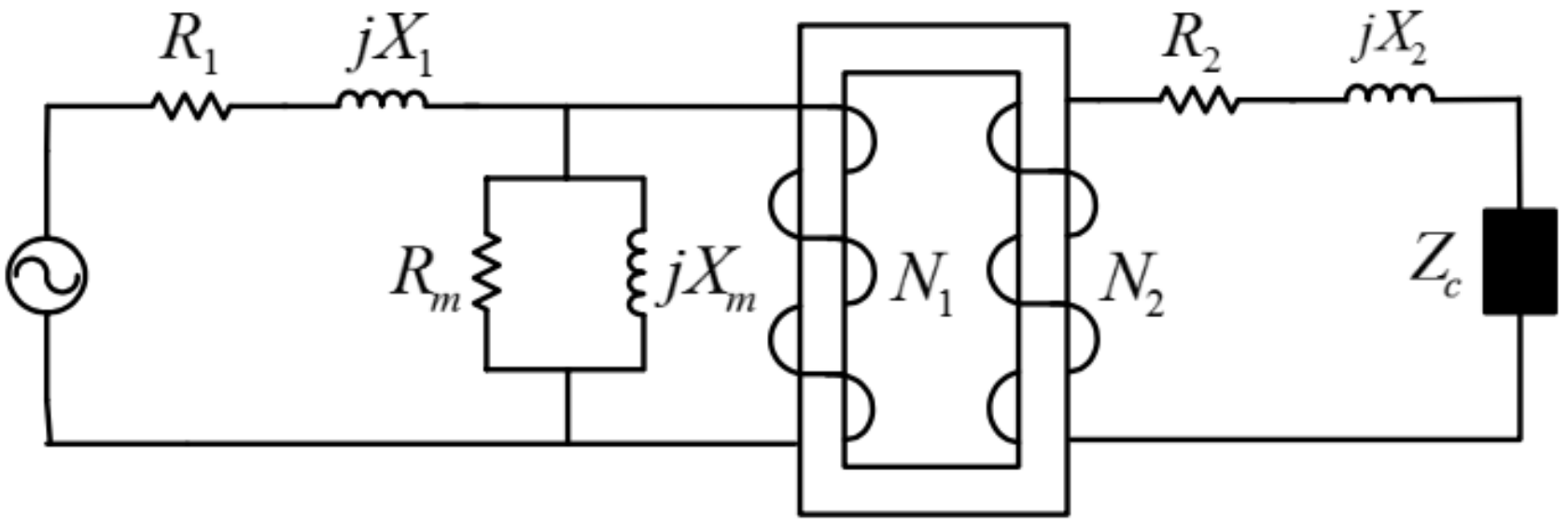


The ideal model is not suitable for studying transformers operation in steady state; in this model, it is considered that all power from the feeding source is given to the load; in consequence, the dispersion flows as well as power losses are not considered. This model does not take into account the power dissipated by the transformer as heat (power losses by Joule effect), parasite currents (power losses by Foucault effect) and core magnetization (power losses by hysteresis effect).

2.2. Transformer model based on losses

Figure 2 shows the transformer equivalent circuit that models power losses as resistances (Martínez-Velasco & de León, 2011). The primary winding impedance is represented as the inductor X_1 and the conductor losses as R_1. The magnetization branch is represented as the inductor X_m and core losses as R_m. The secondary winding impedance is represented as the inductor X_2 and the conductor losses as R_2. Inductors X_1, X_2 also model the dispersion flows in the primary and secondary windings, respectively. The inductor X_m models excitation current effects in the transformer core.

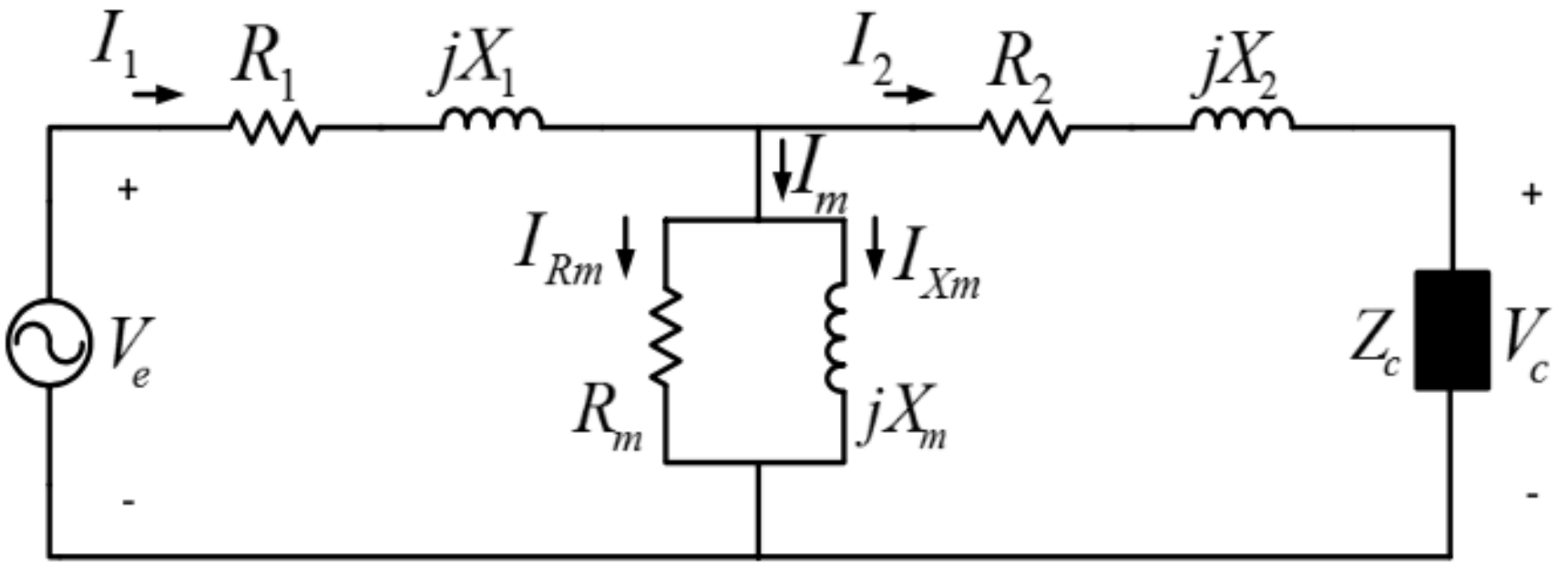
Figure 2
Transformer model
based on losses



The transformer model depicted in figure 2 can be simplified as follows: the impedances of the secondary side are transferred to the primary side (model referred to primary side); or conversely, the impedances of the primary side are transferred to the secondary side (model referred to secondary side). Figure 3 shows the transformer equivalent circuit based on losses or transformer conventional model which is used when calculations are referred to one transformer side.

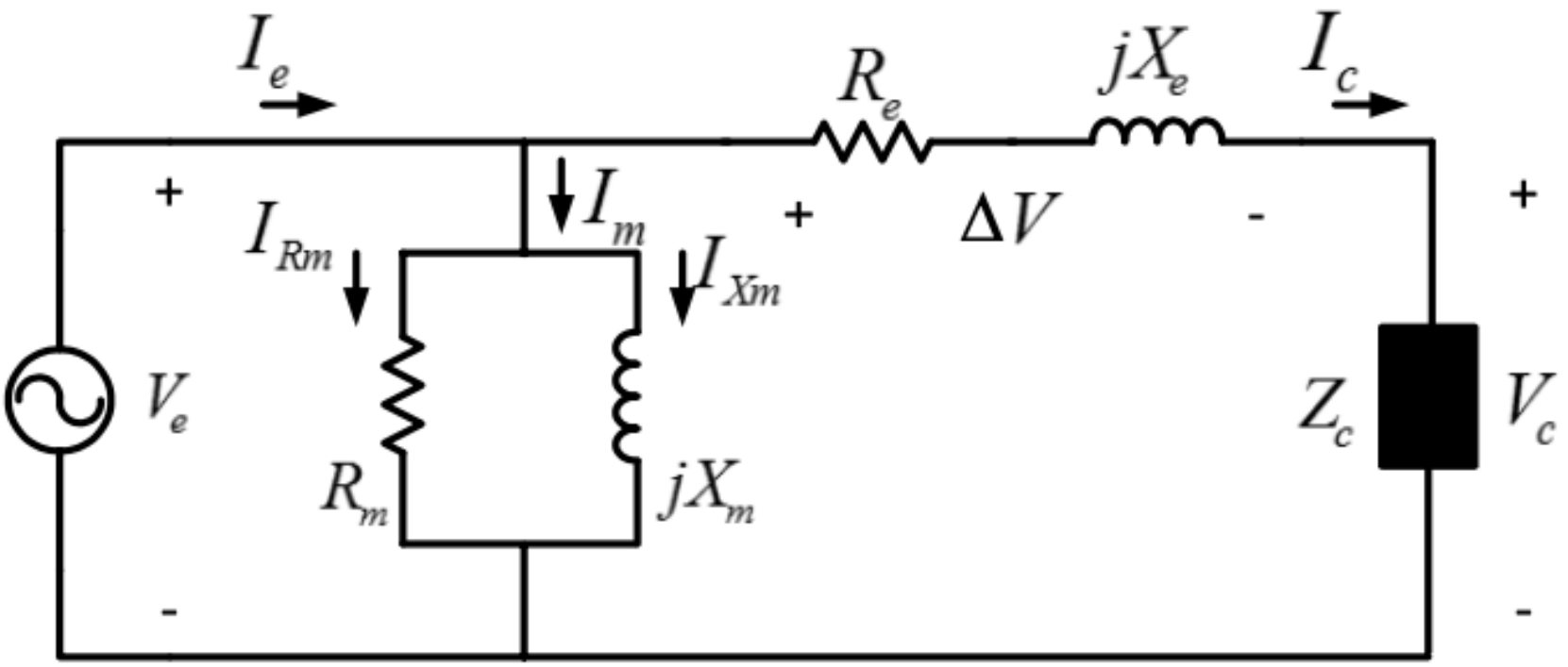
Figure 3
Transformer conventional

model.



In figure 3, the magnetization impedance formed by the parallel between R_m and jX_m ($Z_m = R_m || jX_m$) can be moved to the primary winding terminals. Thus, windings impedances are in series and they can be added to obtain the transformer simplified model depicted in figure 4.

Figure 4
Transformer
simplified model



The transformer's simplified model can be used without introducing significant mistakes in calculations because core losses depend on the feeding voltage magnitude. The voltage magnitude does not significantly change because voltage drop in windings is usually small compared with the feeding voltage. In the transformer simplified model, the primary and secondary windings are represented with their series equivalent circuit formed by $R_e + jX_e$ where: $R_e = R_1 + R_2'$ and $X_e = X_1 + X_2'$, this when it is necessary to solve the transformer referred to the primary side. $R_e = R_1' + R_2$ y $X_e = X_1' + X_2$ are used when it is necessary to solve the transformer referred to the secondary side. Primed variables correspond to resistance and inductance of primary and secondary sides referred to the secondary and primary sides, respectively.

In this paper, the simplified model of figure 4 is used for analyzing the equivalent circuit solution. This model is used due to the fact that transformers can be adequately modeled without introducing significant mistakes in the calculations. Additionally, the equivalent circuit solution of the simplified model is simpler than the solution by means of the models illustrated in figures 2 and 3.2.3. Unified solution method

In this section, the proposed method for solving transformer equations is explained. The method has 5 variants according to transformer vector group and reference side for solving the equivalent circuit. The method variants are: 1) single-phase referred to secondary side (SS), 2) three-phase referred to secondary side (TS), 3) single-phase referred to primary side (SP), 4) three-phase referred to primary side (TP) and 5) the per unit (p.u) system.

In variants SS and SP voltages, currents and powers per phase are used, and results are given in per phase values. In variants TS and TP three-phase powers with line-line voltages and line currents are used; results are also given in three-phase values. In variant 5 (per unit) all variables and parameters are changed to p.u system and results are also in p.u system.

The solution method allows solving the transformer equivalent circuit independently of the selected variant. Coefficients (k_i, $i = 1,2,\ldots.8$) are used to simplify the solution of equations since they are similar for all variants. Coefficients are selected according to the chosen variant and transformer vector group. Coefficients are explained at end of this section.

2.4. General definitions for transformer variables and parameters

In this section, the nomenclature is explained. Parameters and variables in bold style refer to a phasor quantity. Parameters and variables with no bold style correspond to magnitudes. Parameters and variables with only one sub-index correspond to per unit system or test data.

Transformer parameters are: $\boldsymbol{Z}_{*\_\#}$: impedance, $R_{*\_\#}$: resistance and $X_{*\_\#}$: inductance. transformer variables are: $\boldsymbol{S}_{*\_\#}$: apparent power, $P_{*\_\#}$: active power, $V_{*\_\#}$: voltage, $\Delta\boldsymbol{V}_{*\_\#}$: voltage drop, $Vreg$: voltage regulation, $I_{*\_\#}$: current, a: voltage ratio, fp: power factor, and η: efficiency.

Sub-indexes " $*$ " and "#" are used for simplifying the parameters and variables writing. Sub-index " $*$ " indicates the parameter or variable type ($*= 1, 3, b, eq, m, pu, ll, ln, i, fe, cu, fd$), where 1: single-phase, 3: three-phase, b: base, eq: equivalent, m: magnetization, pu: per unit, ll: line-line, ln: line-neutral, i: input, cu: copper losses, fe: iron losses, fd: magnetization. Sub-index "#" indicates the reference side of parameter or variable ($\# = t, p, s, n, c$) where t: transformer, p: primary, s: secondary, n: nominal and c: load. Thus, table 1 shows nomenclature of parameters and variables according to method variant. For example, the variant TS has the base impedance $Z_{b\_\#} = Z_{b\_s}$, being the sub index s to indicate that the impedance is in transformer secondary side.

Table 1
Parameters and variables according to variant selected

Parameter or variable \ variant	SS	TS	SP	TP	p.u
$Z_{b\_\#}$	Z_{b_s}	Z_{b_s}	Z_{b_p}	Z_{b_p}	Z_b
$\boldsymbol{Z}_{eq\_\#}$	$\boldsymbol{Z}_{eq\_s}$	$\boldsymbol{Z}_{eq\_s}$	$\boldsymbol{Z}_{eq\_p}$	$\boldsymbol{Z}_{eq\_p}$	$\boldsymbol{Z}_{eq}$
V_{*_c}	V_{ln_c}	V_{ll_c}	V_{ln_c}	V_{ll_c}	V_c
S_{*_c}	S_{1_c}	S_{3_c}	S_{1_c}	S_{3_c}	S_c
$\boldsymbol{I}_{*\_c}$	$\boldsymbol{I}_{f\_c}$	$\boldsymbol{I}_{l\_c}$	$\boldsymbol{I}_{f\_c}$	$\boldsymbol{I}_{l\_c}$	$\boldsymbol{I}_c$
$\Delta\boldsymbol{V}_{*\_\#}$	$\Delta\boldsymbol{V}_{ln\_t}$	$\Delta\boldsymbol{V}_{ll\_t}$	$\Delta\boldsymbol{V}_{ln\_t}$	$\Delta\boldsymbol{V}_{ll\_t}$	$\Delta\boldsymbol{V}_t$
$\boldsymbol{V}_{*\_e}$	$\boldsymbol{V}_{ln\_e}$	$\boldsymbol{V}_{ll\_e}$	$\boldsymbol{V}_{ln\_e}$	$\boldsymbol{V}_{ll\_e}$	$\boldsymbol{V}_e$
$R_{m\_\#}$	R_{m_s}	R_{m_s}	R_{m_p}	R_{m_p}	R_m
$\boldsymbol{X}_{m\_\#}$	$\boldsymbol{X}_{m\_s}$	$\boldsymbol{X}_{m\_s}$	$\boldsymbol{X}_{m\_p}$	$\boldsymbol{X}_{m\_p}$	$\boldsymbol{X}_m$
$\boldsymbol{Z}_{m\_\#}$	$\boldsymbol{Z}_{m\_s}$	$\boldsymbol{Z}_{m\_s}$	$\boldsymbol{Z}_{m\_p}$	$\boldsymbol{Z}_{m\_p}$	$\boldsymbol{Z}_m$
$\boldsymbol{I}_{m\_\#}$	$\boldsymbol{I}_{m\_s}$	$\boldsymbol{I}_{m\_s}$	$\boldsymbol{I}_{m\_p}$	$\boldsymbol{I}_{m\_p}$	$\boldsymbol{I}_m$
$\boldsymbol{I}_{*\_e}$	$\boldsymbol{I}_{f\_e}$	$\boldsymbol{I}_{l\_e}$	$\boldsymbol{I}_{f\_e}$	$\boldsymbol{I}_{l\_e}$	$\boldsymbol{I}_e$

2.5. Input data

It is considered that in the transformer secondary side a load is connected with the following characteristics: S_{3_c} is three-phase power, V_{ll_c} is line-line voltage and power factor fp in lagging (↓) if load is resistive-inductive or leading (↑) if load is resistive-capacitive. Transformer nominal conditions (from the identification plate) are: three-phase power (S_{3_n}); line-line primary voltage (V_{ll_p}); line-line secondary voltage (V_{ll_s}); short-circuit impedance or equivalent impedance in p.u ($\boldsymbol{Z}_{cc} = Z_{cc}\angle\theta_{cc}$, where θ_{cc} is the impedance angle); iron power losses in p.u (P_{fe}); excitation power in p.u (Q_{fd}) and finally transformer windings connection (YY=wye-wye, ΔY=delta-wye, $\Delta\Delta$=delta-delta, $Y\Delta$=wye-delta). On the other hand, the transformer test data can also be used to calculate the transformer impedances. 1) Short-circuit test: V_{sh}, I_{sh} and P_{sh} are short-circuit voltage, short-circuit current and short-circuit power, respectively. 2) Open-circuit test: V_{oc}, I_{oc} and P_{oc} are open-circuit voltage, open-circuit current and open-circuit power, respectively.

2.6. Proposed solution method

The general solution, step by step is explained as follows:

1) Nominal voltage ratio a_n is calculated according to equation 1.

$$a_n = \frac{V_{ll\_p}}{V_{ll\_s}} \tag{1}$$

Then, the method variant is chosen (SS, TS, SP, TP or p.u). Voltage ratio a is selected in table 2 according to the method variant and windings connection. This voltage ratio is used to change the voltages at the reference side when it is necessary.

Table 2
Voltage ratio *a*

Variant / Windings connection	MS	TS	MP	TP	p.u
YY	1	1	a_n	a_n	1
ΔY	1	1	$\sqrt{3} \cdot a_n$	a_n	1
$\Delta\Delta$	1	1	a_n	a_n	1
$Y\Delta$	1	1	$\frac{1}{\sqrt{3}} \cdot a_n$	a_n	1

In variants SS and TS, $a = 1$ for all winding connections. That is because the load is connected in the secondary side (parameters and variables are in their reference side). In variant p.u, $a = 1$ for all winding connections. In variant TP, $a = a_n$ for all winding connections since it is necessary to change the load reference to primary side from secondary side. In variant SP, $a = a_n$ for YY and $\Delta\Delta$. That is because it is necessary to change the reference from the secondary side to the primary side. In connection ΔY, a_n is multiplied by $\sqrt{3}$ because it is necessary to change V_{ll_s} of equation 1 to voltage per phase (V_{ln_s}) (corresponding to wye connection). In connection $Y\Delta$, a_n is divided by $\sqrt{3}$ because it is necessary to change V_{ll_p} of equation (1) to voltage per phase (V_{ln_p}) (corresponding to wye connection).

2) The base impedance is calculated according to equation (2).

3) The equivalent impedance phasor is obtained as follows: equation (3a) is used when $\boldsymbol{Z}_{eq\_\#}$ is calculated with the nominal short-circuit impedance in p.u (identification plate data) and base impedance; equation 3b is used when $\boldsymbol{Z}_{eq\_\#}$ is calculated with transformer test data.

4) The load voltage is calculated according to the winding connection and reference side.

5) The apparent power magnitude in the load is calculated (equation 5) according to the selected variant.

6) The load current phasor is calculated (equation 6). The current angle θ_{Ic} is obtained from the load power factor; θ_{Ic} is positive if the load is resistive-capacitive or negative if it is inductive-resistive.

7) The voltage drop due to the transformer windings is calculated (equation 7).

8) The input voltage is calculated (equation 8) as the sum of the load voltage and transformer voltage drop.

9) The magnetization resistance is calculated as follows: equation 9*a* is used to calculate $R_{m\_\#}$ with transformer nominal values; equation 9*b* is used when $R_{m\_\#}$ is calculated using the open-circuit test data and θ_m is the magnetization impedance angle.

10) The magnetization inductance is calculated as follows: equation 10*a* is used to calculate $\boldsymbol{X}_{m\_\#}$ with transformer nominal values; equation 10*b* is used when $\boldsymbol{X}_{m\_\#}$ is calculated using the open-circuit test data.

11) The magnetization impedance is calculated (equation 11) as the parallel between the magnetization resistance and the magnetization inductance.

12) The magnetization current is calculated (equation 12) as the relation between the input voltage and the magnetization impedance.

13) The input current is calculated (equation 13) adding the load current and the magnetization current.

14) The transformer iron losses are calculated (equation 14) using the input voltage and the magnetization resistance.

15) The transformer copper losses are calculated (equation 15) with the load current and the real part (resistance) of the equivalent impedance.

16) The transformer efficiency is calculated (equation 16) as the relation between output power and input power. In this step, the load power factor and transformer losses are considered.

17) Voltage regulation percentage is calculated (equation 17) using load voltage and transformer input voltage.

18) Input power factor is calculated (equation 18) with the input voltage angle θ_{Ve} and the input current angle θ_{Ie} of the transformer.

$$Z_{b\_\#} = \frac{(V_{ll\_s})^2}{S_{3\_n}} \tag{2}$$

$$\boldsymbol{Z}_{eq\_\#} = k_1 \cdot Z_{b\_\#} \cdot \boldsymbol{Z}_{eq} \tag{3a}$$

$$\boldsymbol{Z}_{eq_\#} = k_1 \cdot \frac{V_{sh}}{I_{sh}} \measuredangle \theta_{eq} \;\; \therefore \;\; \theta_{eq} = \cos^{-1}\left(\frac{P_{sh}}{V_{sh} \cdot I_{sh}}\right) \tag{3b}$$

$$V_{*\_c} = k_2 \cdot V_{ll\_c} \tag{4}$$

$$S_{*\_c} = k_2 \cdot S_{3\_c} \tag{5}$$

$$\boldsymbol{I}_{*\_c} = k_4 \cdot \frac{S_{*\_c}}{V_{*\_c}} \angle \theta_{Ic} \;\; \therefore \;\; \theta_{Ic} = \pm \cos^{-1}(fp) \tag{6}$$

$$\Delta \boldsymbol{V}_{*\_\#} = k_5 \cdot \boldsymbol{Z}_{eq\_\#} \cdot \boldsymbol{I}_{*\_c} \tag{7}$$

$$\boldsymbol{V}_{e\_\#} = \Delta \boldsymbol{V}_{*\_\#} + \boldsymbol{V}_{*\_c} \tag{8}$$

$$R_{m\_\#} = k_1 \cdot \frac{V_{ll\_s}^2}{P_{fe\_n} \cdot S_{3\_n}} \tag{9a}$$

$$R_{m\_\#} = k_1 \cdot \frac{V_{oc}}{I_{oc} \cdot \cos(\theta_m)} \;\; \therefore \;\; \theta_m = \cos^{-1}\left(\frac{P_{oc}}{V_{oc} \cdot I_{oc}}\right) \tag{9b}$$

$$\boldsymbol{X}_{m\_\#} = k_1 \cdot \frac{V_{ll\_s}^2}{Q_{fd\_n} \cdot S_{3\_n}} \angle 90^o \tag{10a}$$

$$\boldsymbol{X}_{m\_\#} = k_1 \cdot \frac{V_{oc}}{I_{oc} \cdot \sin(\theta_m)} \angle 90^o \tag{10b}$$

$$\boldsymbol{Z}_{m\_\#} = \frac{R_{m\_\#} \cdot \boldsymbol{X}_{m\_\#}}{R_{m\_\#} + \boldsymbol{X}_{m\_\#}} \tag{11}$$

$$\boldsymbol{I}_{m\_\#} = k_6 \cdot \frac{\boldsymbol{V}_{e\_\#}}{\boldsymbol{Z}_{m\_\#}} \tag{12}$$

$$\boldsymbol{I}_{e\_\#} = \boldsymbol{I}_{m\_\#} + \boldsymbol{I}_{*\_c} \tag{13}$$

$$P_{fe\_t} = k_7 \cdot \frac{V_{e\_\#}^2}{R_{m\_\#}} \tag{14}$$

$$P_{cu\_t} = k_8 \cdot I_{*\_c}^2 \cdot Z_{eq\_\#} \cdot \cos(\theta_{eq}) \tag{15}$$

$$\eta = \frac{S_{*\_c} \cdot fp \cdot 100\%}{S_{*\_c} \cdot fp + P_{fe\_t} + P_{cu\_t}} \tag{16}$$

$$Vreg = \frac{V_{e\_\#} - V_{*\_c}}{V_{*\_c}} \cdot 100\% \tag{17}$$

$$fp_e = \cos(\theta_{Ve} \pm \theta_{Ie}) \tag{18}$$

Table 3 shows the values of k_i according to the variant selected and windings connection. For example, if a transformer with windings connection ΔY and variant SP is selected, then, the k_i constants of column Δ are used because the primary winding connection is Δ. Additionally, equations (2) (9) and (10) are not altered when $k_i = 1$.

Constant k_1 is used to multiply the impedances in variants SP and TP by a^2; this is done to transfer the impedances at the primary side. In delta connections, k_1 is used to multiply by 3 according to the theorem of Kennelly for wye-delta transformations (impedance in delta is equal to three times wye impedance). In the p.u variant, this constant is used to divide the impedances by the base impedance; on the other hand, equation 3a has $k_1 = 1$ in p.u variant because the short-circuit impedance is taken from the identification plate (equation 3a does not need a change in this case).

Constant k_2 is used to change the line-line voltage to phase voltage if variant are SP or SS; similarly, the constant is used to change line-neutral voltage to line-line voltage in three-phase variants (TP or TS). Also, constant uses voltage ratio a_n to change the reference side from secondary side to primary side for variants referred to transformer primary side.

Constant k_3 divides by 3 in single-phase variants to transform the three-phase power into power per phase.

Constant k_4 divides by $\sqrt{3}$ in three-phase variants for obtaining the line current.

Constant k_5 divides by $\sqrt{3}$ in delta connections for changing the line current into phase current; also, this constant multiplies by $\sqrt{3}$ in wye connections for changing the phase-neutral voltage into line-line voltage.

Constant k_6 divides by $\sqrt{3}$ in wye connections for changing line-line voltage into phase-neutral voltage; also, this constant multiplies by $\sqrt{3}$ in delta connections for changing phase current into line current.

Constant k_7 divides by $\sqrt{3}$ in wye connections for changing line-line voltage into line-neutral voltage; also, this constant multiplies by 3 in three-phase variants for changing the phase power into three-phase power.

Constant k_8 divides by $\sqrt{3}$ in delta connections for changing the line current into phase current; also, this constant multiplies by 3in three-phase variants for changing the phase power into three-phase power.

Table 3
Constants k_i according to method variant

Variant / Constant	Reference: secondary side				Reference: primary side				p.u
	SS		TS		SP		TP		
	Y	Δ	Y	Δ	Y	Δ	Y	Δ	
k_1	1	3	1	3	a_n^2	$3 \cdot a_n^2$	a_n^2	$3 \cdot a_n^2$	$\frac{1}{Z_{b\_\#}}$
k_2	$\frac{1}{\sqrt{3}}$	1	1	1	$\frac{a}{\sqrt{3}}$	a	a	a	$\frac{1}{V_b}$
k_3	$\frac{1}{3}$	$\frac{1}{3}$	1	1	$\frac{1}{3}$	$\frac{1}{3}$	1	1	$\frac{1}{S_b}$
k_4	1	1	$\frac{1}{\sqrt{3}}$	$\frac{1}{\sqrt{3}}$	1	1	$\frac{1}{\sqrt{3}}$	$\frac{1}{\sqrt{3}}$	1
k_5	1	1	$\sqrt{3}$	$\frac{1}{\sqrt{3}}$	1	1	$\sqrt{3}$	$\frac{1}{\sqrt{3}}$	1
k_6	1	1	$\frac{1}{\sqrt{3}}$	$\sqrt{3}$	1	1	$\frac{1}{\sqrt{3}}$	$\sqrt{3}$	1
k_7	1	1	$\frac{3}{(\sqrt{3})^2}$	3	1	1	$\frac{3}{(\sqrt{3})^2}$	3	1
k_8	1	1	3	$\frac{3}{(\sqrt{3})^2}$	1	1	3	$\frac{3}{(\sqrt{3})^2}$	1

3. Results

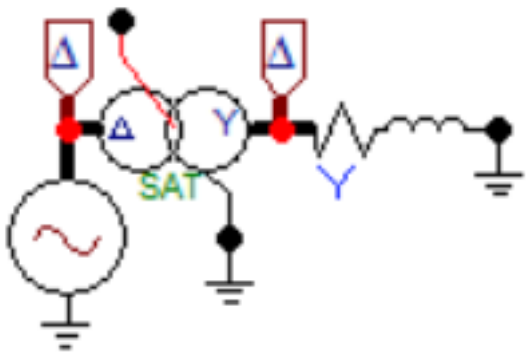
The proposed method is validated in ATPDraw software for a transformer with the following characteristics or identification plate:

$S_{3\_n} = 500\ kVA, V_{ll\_p} = 44\ kV, V_{ll\_s} = 13.2\ kV$
$\boldsymbol{Z_e} = 0.08\angle 80^o, P_{fe\_n} = 0.03, Q_{fd\_n} = 0.02$. Connection=$\Delta Y11$.

Load characteristics:
$S_{3\_c} = 400\ kVA, V_{ll\_c} = 13.1\ kV, fp = 0.9 \downarrow$.

The validation of the proposed approach was performed using theoretical calculations for all variants; the results are compared with ATPDraw results. In this case S_{3_n} and V_{ll_s} are used as base values in variant p.u.
Figure 5 illustrates the simulated circuit in ATPDraw where the transformer is supplied by a three-phase voltage source; the transformer has a load in wye connection. The resistance and inductor are used to model a load with lagging power factor.

Figure 5
Circuit to simulate
in ATPDraw



ATPDraw uses the transformer model of figure 2 for simulation; hence, it is necessary to change the model of the proposed method (figure 4) to the model depicted in figure 2 for simulation purposes. Figure 6 shows the transformer's input data where the primary and secondary rated voltages are rms magnitudes per phase. The resistance and inductance of the primary side correspond to $Z_1 = R_1 + jX_1$ of figure 2. Resistance and inductance of the secondary side correspond to $Z_2 = R_2 + jX_2$ of figure 2. Then, Z_1 and Z_2 correspond to the equivalent impedance of figure 4 ($Z_{eq\_p\_} = Z_1 + Z_2'$). Vector group $\Delta Y11$ causes a phase shift of 330 degrees. Magnetization resistance is calculated using equation 6 of the SP variant. Finally, magnetization current is calculated using equation 12 of the SP variant; ATPDraw calculates the magnetization inductance using the magnetization current in the simulation process.

Figure 6
Input data for
ATPDraw simulation

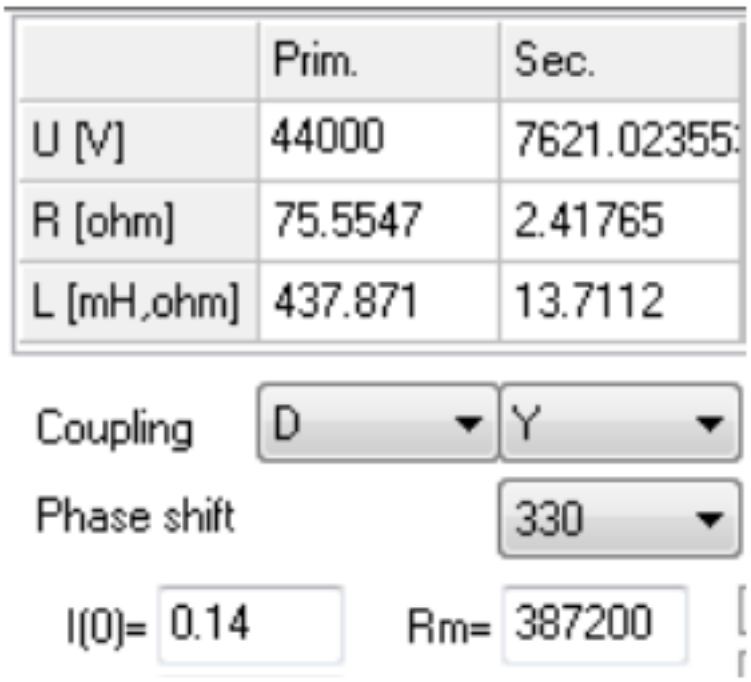


Table 4 shows the calculated results for each variant and ATPDraw simulations results. In this case, the label NA indicates that it is not possible to obtain the corresponding parameter or variable from the ATPDraw simulation.

Simulation results in ATPDraw are validated as follows: 1) the calculation results from variant SP are validating with the variables and parameters measured in transformer primary side from ATPDraw; 2) the variant SS calculations are validated by means of variables and parameters that are measured in the transformer secondary side from ATPDraw. Results are presented in table 4 where each row has two values in bold, the calculated value by the proposed method and its corresponding value from the ATPDraw simulation.

Table 4
Results of
proposed method

Variant / Step	SS	TS	SP	TP	p.u	ATPDraw
(1) a_n	3.33	3.33	3.33	3.33	1	3.33
(1) a	1	1	**5.77**	3.33	1	**5.77**
(2) $Z_{b\_\#}$ [Ω]	348.48	348.48	11616	11616	NA	NA
(3a) $\boldsymbol{Z}_{e\_\#}$ [Ω]	$27.88\angle 80^o$	$27.88\angle 80^o$	$929.28\angle 80^o$	$929.28\angle 80^o$	$0.08\angle 80^o$	NA
(4) V_{*_c} [V]	**7563.28**	13100	43666.66	43666.66	0.99	**7558.37**
(5) S_{*_c} [VA]	**133333.33**	400000	133333.33	400000	0.8	**133164.65**
(6) $\boldsymbol{I}_{*\_c}$ [A]	$\mathbf{17.63\angle -25.84^o}$	$17.62\angle -25.84^o$	$3.05\angle -25.84^o$	$5.28\angle -25.84^o$	$0.8061\angle -25.84^o$	$\mathbf{17.61\angle -25.83^o}$
(7) $\Delta\boldsymbol{V}_{*\_\#}$ [V]	$491.52\angle 54.16^o$	$851.34\angle 54.16^o$	$2834.30\angle 54.16^o$	$2832.82\angle 54.16^o$	$0.0644\angle -54.16^o$	NA
(8) $\boldsymbol{V}_{*\_e}$ [V]	$7861.18\angle 2.90^o$	$13615.98\angle 2.90^o$	$\mathbf{45384.40\angle 2.90^o}$	$45383.48\angle 2.90^o$	$1.029\angle -2.90^o$	$\mathbf{45384.39\angle 2.90^o}$
(9a) $R_{m\_\#}$ [Ω]	11616	11616	**387200**	387200	33.3333	**387200**
(10a) $\boldsymbol{X}_{m\_\#}$ [Ω]	$17424\angle 90^o$	$17424\angle 90^o$	$580800\angle 90^o$	$580800\angle 90^o$	$50\angle 90^o$	NA
(11) $\boldsymbol{Z}_{m\_\#}$ [Ω]	$9665.09\angle 33.69^o$	$9665.098\angle 33.69^o$	$322169.87\angle 33.69^o$	$322169.87\angle 33.69^o$	$27.7350\angle 33.69^o$	NA
(12) $\boldsymbol{I}_{m\_\#}$ [A]	$0.81\angle -30.79^o$	$0.81\angle -30.79^o$	$\mathbf{0.14\angle -30.79^o}$	$0.24\angle -30.79^o$	$0.0371\angle -30.79^o$	$\mathbf{0.14\angle -31.41^o}$
(13) $\boldsymbol{I}_{*\_e}$ [A]	$18.43\angle -26.05^o$	$18.43\angle -26.05^o$	$\mathbf{3.19\angle -26.05^o}$	$5.52\angle -26.05^o$	$0.8430\angle -26.05^o$	$\mathbf{3.21\angle -25.61^o}$
(14) P_{fe_t} [W]	5319.98	15959.94	**5319.58**	15958.75	0.0317	**5112.9**
(15) P_{cu_t} [W]	1504.76	4514.28	**1501.12**	4503.37	0.0090	**1562**
(16) η	94.61 %	94.61 %	94.61 %	94.61 %	94.64 %	94.46 %
(17) V_{Reg}	3.93 %	3.93 %	3.93 %	3.93 %	3.9393 %	4.01 %
(18) fp_e	0.87 ↓	0.87 ↓	0.87 ↓	0.87 ↓	0.87 ↓	0.87 ↓

It is worth to notice that certain values such as copper losses, efficiency, voltage regulation and input power factor are not directly obtained by means of the ATPDraw simulation. However, these values can be calculated by means of other results provided in the simulation. For example, copper losses (P_{cu_t}) can be obtained adding the power losses in each winding. Transformer efficiency is calculated with equation (16). Voltage regulation can be obtained using equation (17). Finally, input power factor is calculated using equation (18).

According to the results presented in Table 4 it can be verified that SS and TS (ΔY connections) have the following equivalences: first, in wye connections line current and phase current are the same; second, in wye connections the line-line voltage is the line-neutral voltage multiplied by $\sqrt{3}$; third, the three-phase power is three times the single-phase power. Also note that SP and TP (ΔY connections) have the following equivalences: first, in delta connections the line-line voltage is equal to the line-neutral voltage; second, in delta connections the line current is the phase current multiplied by $\sqrt{3}$; finally, the power calculated in TP can be obtained multiplying by 3 the power obtained in the SP variant.

Figure 7 shows the main window of the graphic interface implemented in Python to obtain the transformer parameters and variables with the proposed method. The five variants have been implemented in the graphic interface, this one presents the results in the transformer simplified model (see figure 4). The interface can be found in the follow web page:

https://github.com/IceMerman/TransformerSolution

In this interface the user can obtain the parameters and variables of three-phase transformers. In the main window the user indicates the load data and transformer data from the identification plate; also, the user can select method variant and transformer winding connection.

Figure 7
Graphic interface

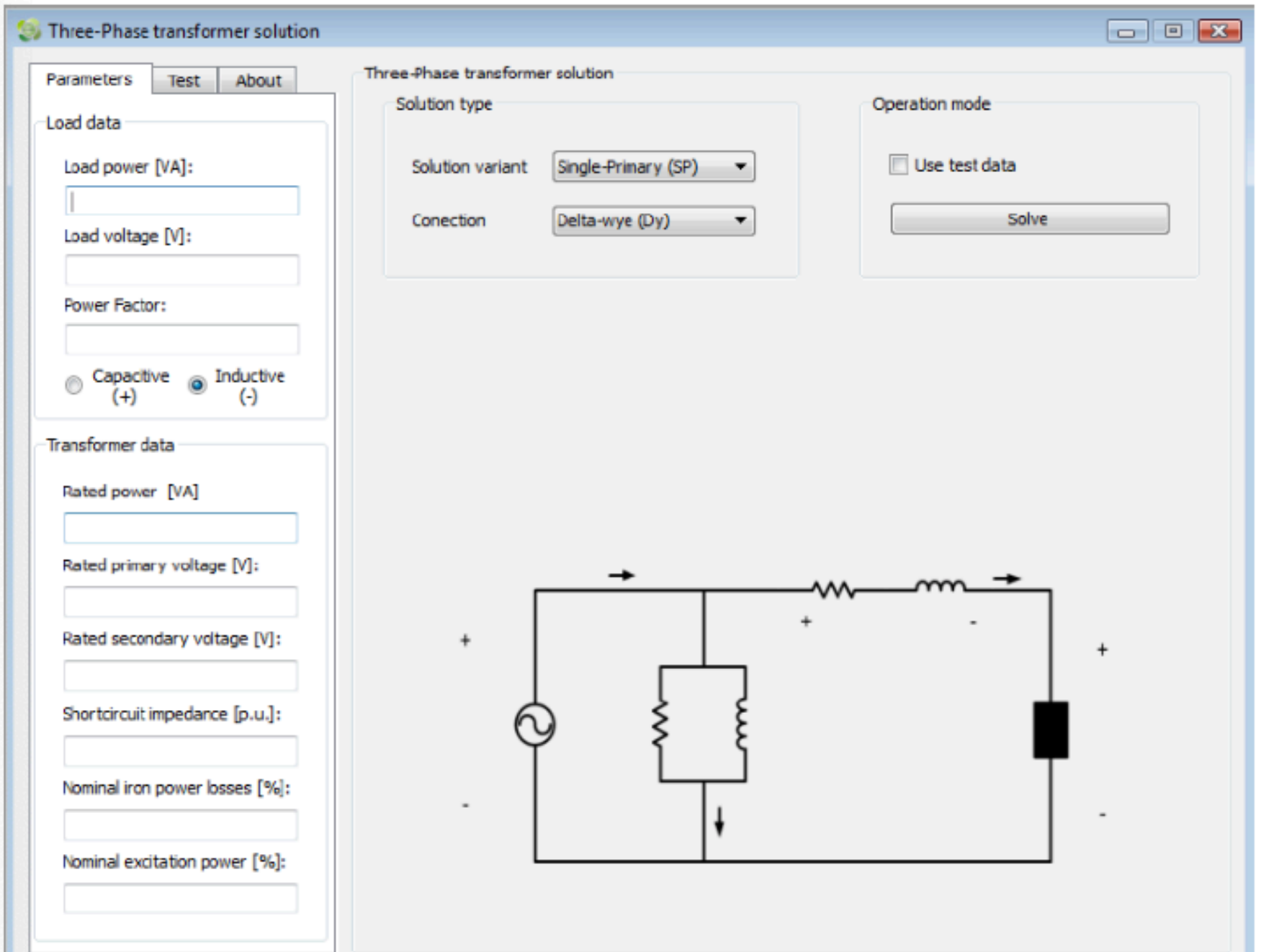
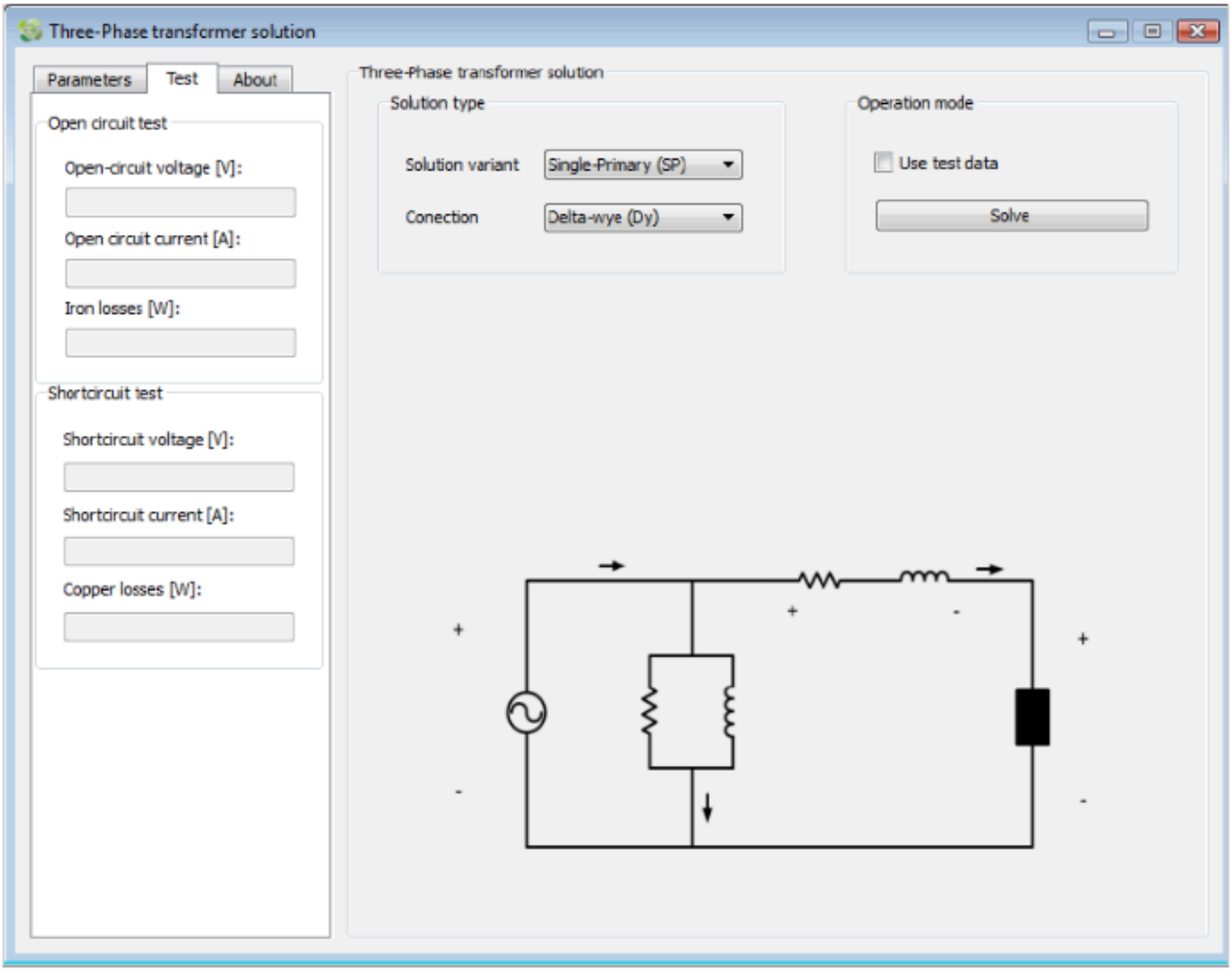


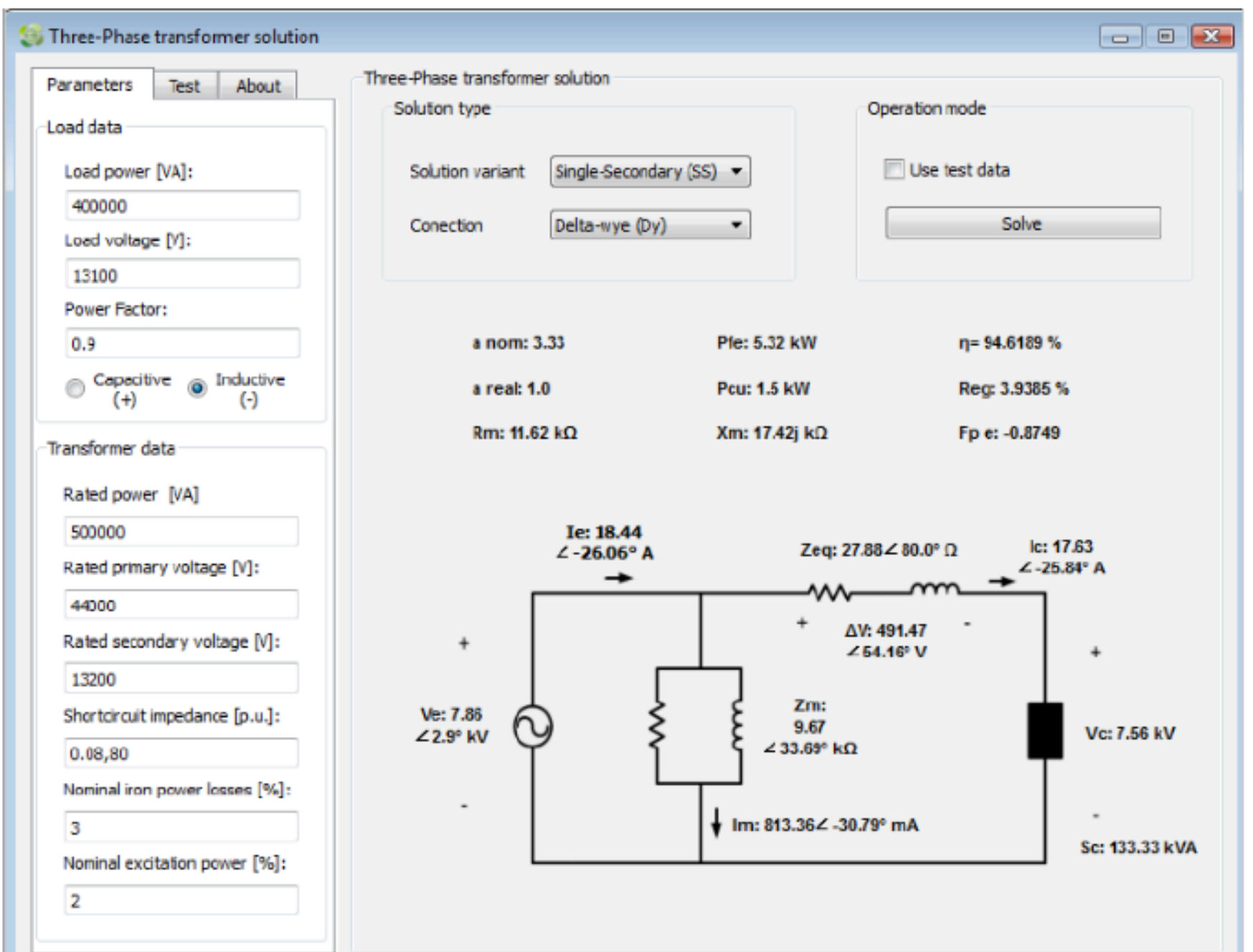
Figure 8 shows the test data panel of the graphic interface. This panel is activated when the option is marked in the "operation mode" section. In this panel, the user can enter the transformer short-circuit and open-circuit test data for the calculation of short-circuit and magnetization impedances.

Figure 8
Test data panel of
the graphic interface



Finally, the “solve” button is used for obtaining the calculation results. Figure 9 shows the results of the example solved in this paper for the SS variant.

Figure 9
Calculation results
for SS variant



4. Conclusions

In this paper, a method with five variations to solve the equivalent circuit of three-phase transformers was proposed and explained. This method allows calculating the electric variables (voltages, currents, powers, efficiency, power factors and voltage regulation) of transformer according to load condition, transformer parameters and transformer test data. The proposed method uses the simplified transformer model and was validated by means of simulations in ATPDraw. Despite of the fact that ATPDraw uses a different transformer model, simulation results were equivalent.

Mathematical results and simulations demonstrate the equivalence between the five method variants. Therefore, it is possible to present a general method to find the transformer variables. The application of the method is useful for engineers in making technical and economic decisions regarding transformer selection and its related variables; as well as for students for the understanding of transformers' performance.

The results obtained with the graphical interface implemented in PYTHON were consistent with the simulations performed in ATPDraw. In this interface, students as well as engineers can obtain the transformer parameters and variables entering the load characteristics, the transformer data from the identification plate and the results of short-circuit and open-circuit tests.

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Power Loss Minimization for Transformers Connected in Parallel with Taps Based on Power Chargeability Balance

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Abstract: In this paper, a model and solution approach for minimizing internal power losses in Transformers Connected in Parallel (TCP) with tap-changers is proposed. The model is based on power chargeability balance and seeks to keep the load voltage within an admissible range. For achieving this, tap positions are adjusted in such a way that all TCP are set in similar/same power chargeability. The main contribution of this paper is the inclusion of several construction features (rated voltage, rated power, voltage ratio, short-circuit impedance and tap steps) in the minimization of power losses in TCP that are not included in previous works. A Genetic Algorithm (GA) is used for solving the proposed model that is a system of nonlinear equations with discrete decision variables. The GA scans different sets for tap positions with the aim of balancing the power supplied by each transformer to the load. For this purpose, a fitness function is used for minimizing two conditions: The first condition consists on the mismatching between power chargeability for each transformer and a desired chargeability; and the second condition is the mismatching between the nominal load voltage and the load voltage obtained by changing the tap positions. The proposed method is generalized for any given number of TCP and was implemented for three TCP, demonstrating that the power losses are minimized and the load voltage remains within an admissible range.

Keywords: transformers connected in parallel (TCP); tap-changers; power chargeability; power loss minimization; genetic algorithms

1. Introduction

Power transformers represent vital equipment and their availability have a major impact on the reliability of a power system [1]. Being one of the key elements of a network, power transformers have been the focus of a great number of studies regarding several issues that include diagnostic methods [2], fault detection [3] and the effects of loads in their ageing [4]. In [3], the authors proposed an algorithm for fault detection as well as faulted phase and winding identification for power transformers based on the induced voltages in a power system. In [1], a reliability analysis and overload capacity assessment of power transformers is presented. The authors based their analysis on the hot-spot temperature of the winding as the most critical factor in measuring the overload capacity of power transformers. A review of the existing studies of the effect of loads and other factors on the ageing of power transformers is presented in [5]. However, a comprehensive review regarding the status and current trend of different diagnostic techniques for power transformers is presented in [2].

This current paper deals with the issue of power loss minimization for transformers operating in parallel. Parallel operation of transformers is a common practice in the electricity industry. This type of arrangement allows improving efficiency, availability, reliability and flexibility. Power transformers exhibit maximum efficiency when operating close to full load. Regarding availability, when transformers are connected in parallel one of them can be switched off for maintenance proposes without incurring in undesired loss of load (supposing that the remaining transformers have enough capability to supply the load). Similarly, as regards reliability a parallel connection facilitates the use of back up transformers in case of a fault. In addition, the parallel connection of transformers adds flexibility to attend the demand growth of an electrical system because new transformers can be incorporated in a modular fashion.

Transformers Connected in Parallel (TCP) with tap-changers are used for controlling power flows through voltage regulation in power grids and ensuring that the load voltage remains within an admissible range; therefore, most methods for coordinating TCP with taps are mainly designed to regulate voltage amplitude [6–12]. In [6,7], tap-changers of TCP are mainly used for reactive power control with the aim of minimizing power losses and therefore the construction features of transformers are neglected. In [8,9], TCP with tap-changers are used in the context of optimal power flow. In this case, the authors objective is to find the optimal tap positions with the aim of improving stability and minimizing generation fuel cost, respectively. In [10], the tap positions of power transformers are optimized for active and reactive power regulation, while in [11,12] the authors present a coordinated voltage control strategy for three-phase On-Load Tap Changer (OLTC) transformers with the aim of dealing with unbalanced networks and power loss minimization, respectively. A common feature of the aforementioned studies is the fact that they considered the TCP as being identical. However, this might not always be the case since given a set of power transformers operating in parallel, if a new one is to be added, it might not have exactly the same construction features. TCP with different construction features, without an adequate control, might exhibit internal circulating currents due to unbalanced voltages in their secondary sides. Circulating currents increase internal power losses since they are not used to supply loads. However, internal power losses of TCP can be reduced using taps and, at the same time, guarantying that the load voltage remains within an admissible range.

Generally, TCP with taps are synchronized using Automatic Voltage Control (AVC) in systems with OLTC for tracking a voltage reference [13,14]. Adaptive Voltage Reference Setting (AVRS) is the most used AVC technique for controlling TCP with taps [15]. This technique is based on tracking a voltage reference using a master-follower controller; the main controller (master) imposes a voltage reference while the secondary controller (follower) tracks the reference changing taps positions [16]. In a master-follower scheme, one OLTC transformer is designed as the master, and all the other OLTC transformers in parallel are the followers. The master transformer monitors the voltage level and alters the tap positions in order to keep it within allowed limits. The other OLTC transformers mimic the same actions keeping all TCP in the same tap positions. The disadvantage of this scheme is the fact that circulating currents will appear if all TCP do not have exactly the same construction features. Other schemes for TCP are the true circulating current and negative reactance compounding, both described in [13]. Furthermore, improved voltage control schemes such as enhanced transformer paralleling package and intelligent AVC relays are the topic of on-going research [14]. In [15,16], the AVRS is used for controlling TCP with OLTC systems being the main function the load voltage regulation. This is carried out keeping all transformers in the same tap position. In [17], the authors proposed an OLTC with solid-state tap-changer using power electronics. Results showed reduction in frictional losses, size of components and operation cost; nevertheless, solid-state tap changer components are more expensive in comparison with mechanical OLTC currently used. It is noteworthy that the aforementioned papers do not consider the AVRS issues regarding power losses, different voltage ratio and different tap steps.

Technical literature lacks of a general method to minimize internal power losses in TCP with different construction features such as rated voltages, rated powers, voltage ratios, short-circuit

impedances and tap steps. Hence, this paper proposes a novel mathematical model that allows finding the tap positions of TCP, that guarantee minimal power losses in TCP while keeping the load voltage within an admissible range. Furthermore, different construction features such as rated voltages, nominal powers, voltage ratios, short-circuit impedances and tap steps are taken into account. For this purpose, a non-linear system of equations with discrete variables (tap positions) obtained from the TCP equivalent circuit is solved. The following hypotheses were considered: (1) Transformers can be from different manufacturers. Then, all TCP have different short-circuit impedances; (2) transformers may have different voltage ratios or tap steps, this leads to current and voltage unbalances; (3) transformers have different percentage of tap steps, this causes internal voltages and current unbalances; (4) transformers have different rated powers, in this case, each transformer provides a different amount of power to the load.

The main features and contributions of this paper are as follows:

(1) A novel mathematical model for the optimal tap setting of TCP with the aim of minimizing power losses is provided, such model takes into account technical features that have not been considered in previous works.
(2) A fitness function that implicitly incorporates the nature of the apparent power without the use of phasors, and that also allows keeping voltages within a specified range is proposed.
(3) The TCP model is expressed as a non-linear discrete optimization problem, which is successfully solved through a meta-heuristic technique.

This paper is organized as follows. In Section 1, the introduction is presented. Section 2 presents the generalization of equivalent circuit and equations of TCP considering transformers with different construction features. In Section 3, power chargeability is defined and its applications to minimize power losses are explained. In Section 4, the proposed method is implemented in a set of three tap-changing TCP. Finally, the more relevant conclusions are presented in Section 5.

2. Tap-Changing TCP

Connection of transformers in parallel consists on connecting the primary windings of all transformers to the same power source and the secondary windings to the same load. Parallel operation of transformers is correct when: No transformer secondary current flows in the no-load state, transformers are loaded proportionally to their rated power and the respective currents of individual transformers are in phase with each other. These conditions are fulfilled if the following requirements are met:

(1) Rated voltages, both primary and secondary, should be the same (within an error of 0.5%).
(2) Transformers should have the same group of connections with the same hourly shift.
(3) Short-circuit voltages of the transformers should not differ by more than 10%.
(4) The operational power ratio should not be bigger than 1/3 of any transformer.

If some of these conditions are not complied, internal circulating currents appear due to voltage unbalances, which increase power losses in transformers. Therefore, TCP with different parameters produce an asymmetric distribution of currents between the windings of the TCP; each current depends on the voltage magnitude imposed in the secondary side of each transformer and the position of the taps.

Figure 1 represents the one-line diagram equivalent circuit for three-phase TCP with load. The subscript k is used to denote the position for each transformer (t_k). Then, $k = 1, 2, 3, \ldots, x$; being x the total number of TCP. V_p is the primary voltage, a_k is the voltage ratio according to tap position, $V_{s\_k} = V_p/a_k$ is the secondary voltage for each transformer, Z_{sh_k} is the short-circuit impedance, and I_k is the current provided for each transformer to the load. Finally, n_{m_k} is the tap number of each transformer, so $m = 1, 2, 3, \ldots, q$; being q the last tap position of transformer t_k.

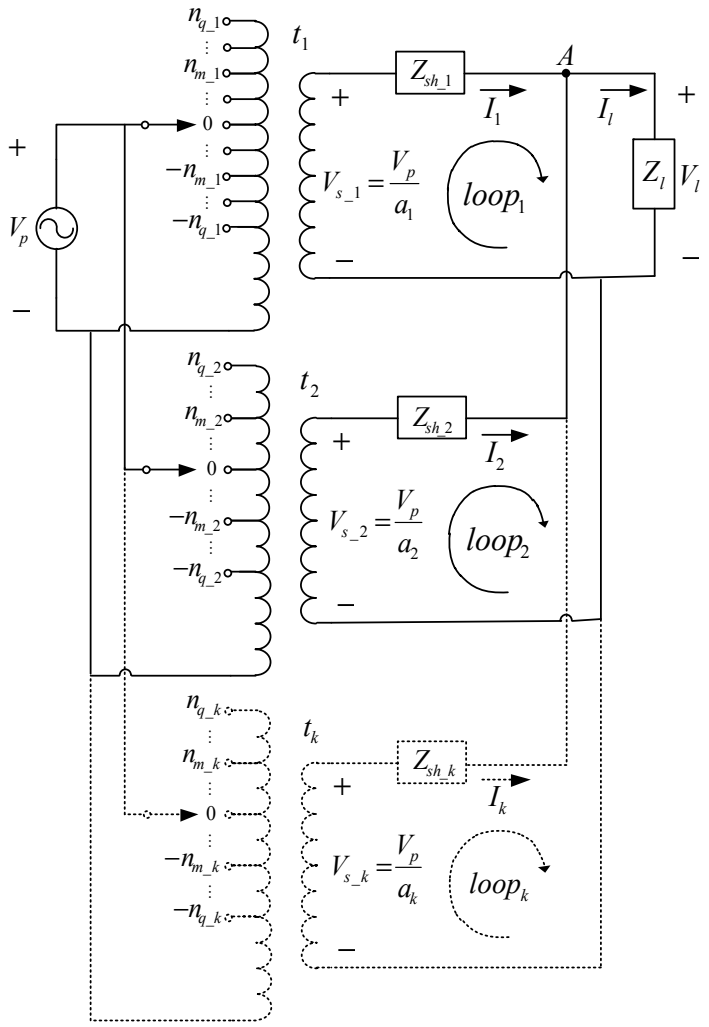

Figure 1. One-line diagram equivalent circuit of transformers connected in parallel (TCP) with load.

Equation (1) is obtained when Kirchhoff's voltage law is applied in the transformer secondary sides ($loop_1, loop_2, \ldots, loop_k$), the last row in Equation (1) is obtained by applying Kirchhoff's current law in node A.

$$\begin{bmatrix} V_p/a_1 \\ V_p/a_2 \\ \vdots \\ V_p/a_k \\ \vdots \\ V_p/a_x \\ 0 \end{bmatrix} = \sqrt{3} \cdot \begin{bmatrix} Z_{sh\_1} & 0 & \ldots & 0 & 0 & 0 & Z_l \\ 0 & Z_{sh\_2} & \ldots & 0 & 0 & 0 & Z_l \\ 0 & 0 & \ddots & 0 & 0 & 0 & \vdots \\ 0 & 0 & 0 & Z_{sh\_k} & 0 & 0 & Z_l \\ 0 & 0 & 0 & 0 & \ddots & 0 & \vdots \\ 0 & 0 & 0 & 0 & 0 & Z_{sh\_x} & Z_l \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \ldots & \frac{1}{\sqrt{3}} & \ldots & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_k \\ \vdots \\ I_x \\ I_l \end{bmatrix} \quad (1)$$

In Equation (1), voltage ratios ($a_1, a_2, \ldots a_k, \ldots a_x$) are represented by each nominal voltage ratio ($a_{N\_1}, a_{N\_2}, \ldots a_{N\_k}, \ldots a_{N\_x}$) and tap step percentage ($tsp_1, tsp_2, \ldots tsp_k, \ldots tsp_x$) of each transformer as follows.

$$a_k = a_{N\_k} \cdot \left(1 + n_{m\_k} \cdot \frac{tsp_k}{100}\right) \quad (2)$$

Equation (2) allows calculating voltage ratio according to the transformer tap position. As it is aforementioned, the main goal of this paper is to find n_{m_k} of each transformer such as power losses

in TCP are minimized. To achieve this, it is necessary to solve the system of equations formed by Equations (1) and (2). Equation (1) is nonlinear with discrete variables, because the discrete voltage ratios are considered according to Equation (2). The solution of the equation system allows obtaining the currents, which each transformer provides to the load.

3. Power Chargeability in TCP and Problem Description

3.1. Problem Description

Figure 2 shows the apparent power phasors for TCP $(S_1,\ S_2,\ \ldots,\ S_k,\ \ldots,\ S_x)$ and the power load phasor (S_l) demanded by the load. It is considered that the load demands a resistive-inductive power. Each S_k phasor can be decomposed in direct and quadrature components taking S_l as a reference. The direct components $(S_{l_1},\ S_{l_2},\ \ldots,\ S_{l_k},\ \ldots,\ S_{l_x})$ are in phase with S_l and are considered in this paper as efficient since they produce currents that directly flow from TCP to the load. The quadrature components $(S_{loss_1},\ S_{loss_2},\ \ldots,\ S_{loss_k},\ \ldots,\ S_{loss\_x})$ are in quadrature with S_l and are considered in this paper as inefficient since they produce recirculating currents between the TCP; in other words, the sum of all quadrature components is zero $(\sum_{k=1}^{x} S_{loss\_k})$ yielding to undesirable energy interchange between the TCP. Equation (3) can be used to quantify such undesirable energy interchange presented in Figure 2; it is observed that the load consumes less power than the one provided by the transformers due to the quadrature components of S_k.

$$S_l < \sum_{k=1}^{x} S_k \tag{3}$$

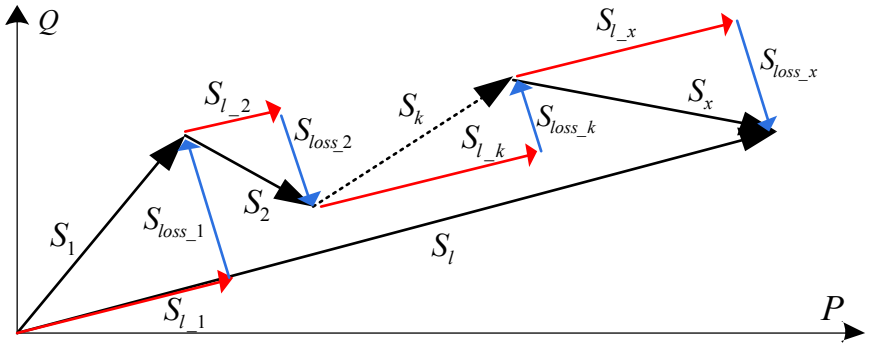

Figure 2. Load and TCP power phasors in the non ideal case. P (W), Q (VAr), S (VA).

3.2. Condition 1: Operation of Transformers in Similar Power Chargeability

The situation illustrated by Equation (3) and Figure 2 can be solved when there are not quadrature components of S_k, being all S_k phasors in phase with S_l. This is an ideal situation where $S_l = \sum_{k=1}^{x} S_k$, (see Figure 3); to approximate to this case, condition 1, operation of transformers in similar power chargeability, presented in Equation (4) is proposed to minimize quadrature components. Condition 1 allows carrying out all TCP to similar power chargeability minimizing the mismatching between the TCP chargeability and the desired chargeability ($S_{c\_l} = S_l / S_{N\_t}$); where S_{N_t} is the total nominal power available from all transformers (sum of all TCP nominal powers $S_{N\_t} = \sum_{k=1}^{x} S_{N\_k}$). The losses minimization is obtained when all transformer powers are delivered to the load, then power flows are not recirculating between transformers. This condition is fulfilled when all TCP are in equal power chargeability. Power chargeability S_{c_k} of a transformer is defined as the ratio

between the apparent power provided by the transformer (S_k) and its nominal power (S_{N_k}) where ($S_{c\_k} = S_k / S_{N\_k}$).

$$\underbrace{\min \sum_{k=1}^{x} (S_{c\_k} - S_{c\_l})^2}_{\text{condition 1}} \tag{4}$$

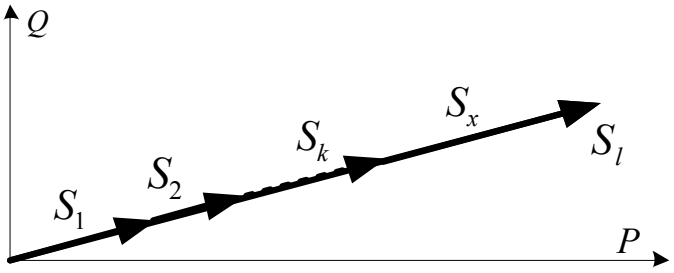

Figure 3. Load and TCP power phasors in the ideal case where $S_l = \sum_{k=1}^{x} S_k$.

3.3. Condition 2: Load Voltage into Admissible Range

Condition 2, load voltage into admissible range, given by Equation (5), is used to keep the load voltage within an allowed range. Note that in this case, condition 2 is zero when the deviation of the load voltage (V_l) with respect to the nominal load voltage (V_{N_l}) is less than 5%; otherwise, it is greater than zero. Figure 4 shows the condition 2 delimiting an admitted zone where the voltage is in the allowed range and a penalization zone where the voltage is not in the permitted range.

$$\underbrace{\max\left(\left|1 - \frac{V_l}{V_{N\_l}}\right| - 0.05, \quad 0\right)}_{\text{condition 2}} \tag{5}$$

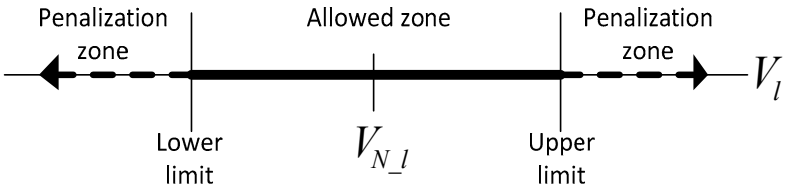

Figure 4. Load voltage constrain (condition 2), load voltage into admissible range.

3.4. Methodology

The objective consists on finding the tap positions of all TCP so that transformers operate with similar power chargeability and the load voltage is kept within the allowed range. To achieve this, the embedded Genetic Algorithm (GA) routine of Matlab [18] is used in order to obtain the best tap positions for the TCP. It is worth to mention that any other meta-heuristic technique can be applied for this purpose. The main aim of this paper is not the solution method but the model for power loss minimization in TCP. A GA is a meta-heuristic technique that mimics the process of natural selection. It starts with a set of randomly generated set with candidate solutions, then these solutions or individuals go through a process of selection, crossover and mutation in which the algorithm explores the search space and gradually improves the quality of the initial set of solutions [19]. GAs belong to the larger set of evolutionary algorithms which have been widely used in engineering applications [20,21]. The main advantage of GA lies in the fact that they are able to provide high-quality solutions for non-convex, non-linear optimization problems. In this case, the default parameters of the Matlab GA

were used, providing adequate results. The decision variables for the optimization process are the tap positions (n_{m_k}) of each transformer. A vector represents a candidate solution, as it is indicated in Figure 5. Every entry of such vector indicates the tap position of the corresponding transformer.

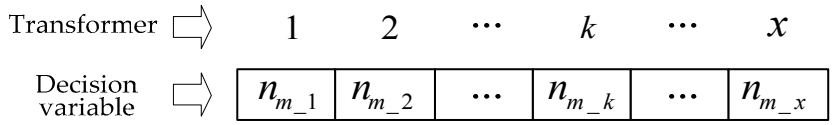

Figure 5. Codification of candidate solutions.

3.4.1. Fitness Function

The GA is used to minimize the fitness function given by Equation (6); subject to the constraints given by Equations (1) and (2). Constants C_1 and C_2 are used to weigh the contribution of each condition in the fitness function. In this way, it is possible to focus the optimization process to obtain a better result in power chargeability balance or load voltage regulation according to the constant magnitudes.

$$\text{minimize}\left\{\underbrace{C_1 \cdot \sum_{k=1}^{x}\left(S_{c\_k} - S_{c\_l}\right)^2}_{\text{condition 1}} + \underbrace{C_2 \cdot \max\left(\left|1 - \frac{V_l}{V_{N\_l}}\right| - 0.05,\quad 0\right)}_{\text{condition 2}}\right\} \tag{6}$$

Condition 1 implies that all TCP are in similar power chargeability guaranteeing the reduction of circulating currents and power losses minimization, while condition 2 is used to keep the load voltage within an admissible range. Condition 1 can be modified when it is necessary to select the best chargeability in a period divided in several load conditions. In this case, condition 1 is weighed with the load energy $(S_k \cdot \Delta T_k)$ for each load condition as illustrated in Equation (7), being ΔT_k the load duration time.

$$\text{minimize}\left\{\underbrace{C_1 \cdot \sum_{k=1}^{x}\left(S_{c_k} - S_{c_l}\right)^2 \cdot (S_k \cdot \Delta T_k)}_{\text{condition 1}} + \underbrace{C_2 \cdot \max\left(\left|1 - \frac{V_l}{V_{N\_l}}\right| - 0.05,\quad 0\right)}_{\text{condition 2}}\right\} \tag{7}$$

3.4.2. Input and Output Data of the Proposed Method

The input data to optimize TCP are: Primary voltage V_p, transformer short-circuit impedances Z_{sh_k}, load impedance Z_l, nominal voltage ratios a_{N_k}, maximum tap value of each transformer n_{q_k} and transformer tap step percentages tsp_k. The GA output data are: each tap step position n_{m_k}, each transformer chargeability S_k and the load voltage V_l.

4. Tests and Results

In this section, the proposed method is implemented with three TCP feeding a load with power variations in an operation period. The optimization was done in two common cases as follows: (1) The control is an OLTC system, such as, tap positions are automatically set according to the variation of the power demanded by the load; (2) the control is manual and taps are set in a fixed position for all operation during a time frame.

Figure 6 shows three load profiles with lagging power factor (pf), which are used to feed the three tap-changing TCP. In profile 1, the load demanded is $S_l = 100$ kVA with $pf = 0.92$ for three hours;

in profile 2, the load demanded is $S_l = 130$ kVA with $pf = 0.96$ for four hours; finally, in profile 3, the load demanded is $S_l = 150$ kVA with $pf = 0.91$ for three hours.

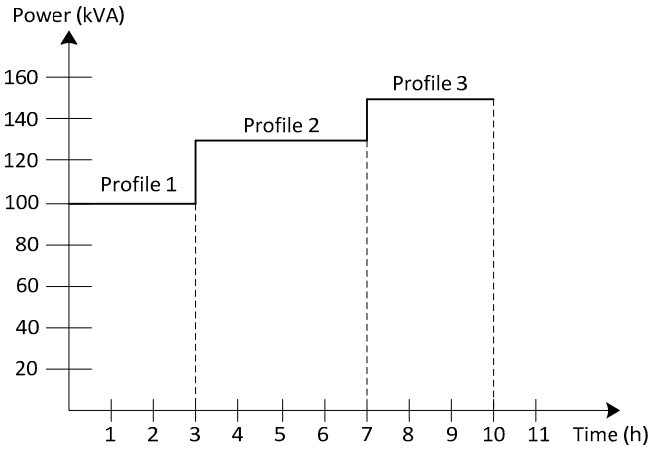

Figure 6. Load profiles in the operation period.

Table 1 shows the characteristics of the three tap-changing TCP. Note that transformers with different construction features (nominal power S_{N_k}, short-circuit impedance Z_{sh_k}, primary nominal voltage V_{Np_k}, secondary nominal voltage V_{Ns_k}, maximum tap position n_{q_k} and tap step percentage (tsp_k) were considered.

Table 1. Tap-changing transformers data.

t_k	S_{N_k} (kVA)	Z_{sh_k} (%)	V_{Np_k} (kV)	V_{Ns_k} (kV)	n_{q_k}	tsp_k (%)
t_1	30	3.0	13.2	240	6	1.5
t_2	45	3.0	13.2	240	6	1
t_3	75	3.5	13.2	240	7	3

4.1. Optimization with an OLTC System

An OLTC system is a controller used to changing tap positions automatically during load state changes without transformer disconnections. In this case, the OLTC system sets the tap positions for each load profile of Figure 6. Table 2 shows the results obtained for the three load profiles; so for each transformer is obtained: Tap position, power chargeability, mismatching voltage in the load and the wanted chargeability. Note that for load profile 1, there are different tap positions for all transformers ($n_{m\_1} = 2$, $n_{m\_2} = 3$ and $n_{m\_3} = 1$); however, transformers 1 and 2 have equal power chargeability ($S_{c\_1} = S_{c\_2} = 66.05\%$) being the chargeability of transformer 3 less than the ones of S_{c_1} and S_{c_2} ($S_{c\_3} = 56.62\%$). However, transformer 3 has the major tap step yielding a major chargeability mismatch between S_{c_l}; therefore, the optimization process sets the tap in position 1 of transformer 3 so that S_{c_3} does not surpass the wanted chargeability ($S_{c\_l} = 61.16\%$). The load voltage mismatch is 4.22%, fulfilling the load voltage constraint of 5% with respect to the nominal load voltage.

In load profile 2, all tap positions are different ($n_{m\_1} = 3$, $n_{m\_2} = 4$ and $n_{m\_3} = 1$); nevertheless, all transformers present similar chargeability ($S_{c\_1} = 72.82\%$, $S_{c\_2} = 78.34\%$ and $S_{c\_3} = 81.92\%$) close to $S_{c\_l} = 78.29\%$. In this case, transformer 2 has the closest chargeability to S_{c_l}, yielding minimum circulating currents in the system due to transformer 2. However, it is guaranteed the best operation point for transformers 1 and 2 (S_{c_1} and S_{c_3} are close to S_{c_l}) with the load voltage mismatch within the admissible range (4.95%) according to tap step restrictions.

In load profile 3, the effect of different tap steps in transformers 1 and 2 is observed, both transformers have the same tap position ($n_{m\_1} = n_{m\_2} = 1$) but different chargeability ($S_{c\_1} = 85.60\%$ and $S_{c\_2} = 94.14\%$).

In this case, transformer 2 has the closest chargeability to S_{c_l}. This minimizes the circulating currents in the system since transformer 3 is approximately charged at its maximum ($S_{c\_3} = 99.65\%$). The optimization process sets all transformers in an operation point where the chargeabilities are close to the desired chargeability ($S_{c\_l} = 94.67\%$) and the mismatching voltage is less than 5% in this profile (2.70%).

The transformers considered in this test exhibit different short circuit impedances, tap numbers, tap steps and rated powers; therefore their tap adjustments do not allow the chargeability to be equal to S_{c_l}. However, the tap setting obtained thorough the GA guarantees an operation point where power losses are minimal and the load voltage remains within an admissible range (0–5%).

Table 2. Optimization results for TCP with an OLTC system.

Load Profile	Transformer 1		Transformer 2		Transformer 3		Voltage Mismatch (%)	S_{c_l} (%)
	n_{m_1}	S_{c_1} (%)	n_{m_2}	S_{c_2} (%)	n_{m_3}	S_{c_3} (%)		
1	2	66.05	3	66.05	1	56.62	4.22	61.16
2	3	72.82	4	78.34	1	81.92	4.95	78.29
3	1	85.60	1	94.14	0	99.65	2.70	94.67

4.2. Optimization without OLTC System

In this case, an automatic controller is not available and transformer taps must be adjusted only one time for the operation period (10 h) during the three load profiles (Figure 6). This condition exhibits a more challenging task since the taps must be kept fixed in a position for all load profiles; in consequence, it is necessary to find the best operation point where power losses are minimal throughout the operation period. In this case, the optimization process is performed considering the fitness function given by Equation (7).

Table 3 shows the results for the three load profiles, obtaining tap position, power chargeability, mismatching voltage, the wanted chargeability and duration time of each profile. The tap positions $n_{m\_1} = 1$, $n_{m\_2} = 1$ and $n_{m\_3} = 0$ obtained are kept fixed throughout the operation period. In load profile 1, every transformer exhibits a different power chargeability ($S_{c\_1} = 54.70\%$, $S_{c\_2} = 61.48\%$ and $S_{c\_3} = 71.42\%$). The load voltage mismatch is 1.97%, fulfilling the load voltage constrain of 5% with respect to the nominal load voltage. In comparison with load profile 1 of the OLTC case, the voltage mismatch is lower; however differences in the chargeability of transformers are greater and further form the desired value ($S_{c\_l} = 61.16\%$), being the chargeability of transformer 2 the closest to S_{c_l}.

In load profile 2, every transformer also has a different power chargeability ($S_{c\_1} = 76.97\%$, $S_{c\_2} = 82.89\%$ and $S_{c\_3} = 87.21\%$) and the load voltage mismatch is 2.12%. In comparison with the load profile 2 from OLTC case, the chargeabilities are more sparse of $S_{c\_l} = 83.03\%$. However, the obtained tap settings guarantee a voltage mismatch lower than the one obtained with the OLTC system, and chargeabilities closer to $S_{c\_l} = 83.03\%$.

In load profile 3, the results are the same as those reported in Table 2 with OLTC system. This is because load profile 3 is the one that demands the highest power. Therefore, load profile 3 presents the major power losses and the optimization process prioritizes this profile. Nevertheless, load profiles 1 and 2 also comply with conditions 1 and 2, guaranteeing the best power chargeability balance and load voltage in the admissible range.

Table 3. Optimization results for TCP without OLTC system.

Load Profile	Time (h)	Transformer 1		Transformer 2		Transformer 3		Voltage Mismatch (%)	S_{c_l} (%)
		n_{m_1}	S_{c_1} (%)	n_{m_2}	S_{c_2} (%)	n_{m_3}	S_{c_3} (%)		
1	3		54.70		61.48		71.42	1.97	64.06
2	4	1	76.97	1	82.89	0	87.21	2.12	83.03
3	3		85.60		94.14		99.65	2.70	94.67

4.3. Optimization Performance

Figures 7 and 8 depict the best and mean value of the fitness function versus the number of generations, for the two cases under study: with and without OLTC system, respectively. Note that from the beginning of the optimization process (approximately within the first five generations), the best value of the fitness function quickly reaches values close to zero (the optimal solution). According to the objective function given by Equation (6), this means that after a few generations, among the current population of competing solutions there is at least one that minimizes power losses of the TCP and keeps the voltages within established limits. Despite of this fact; in each iteration, the GA continues to explore the search space to try to find better solutions, in this way the mean value of the fitness function quickly reduces as the algorithm iterates.

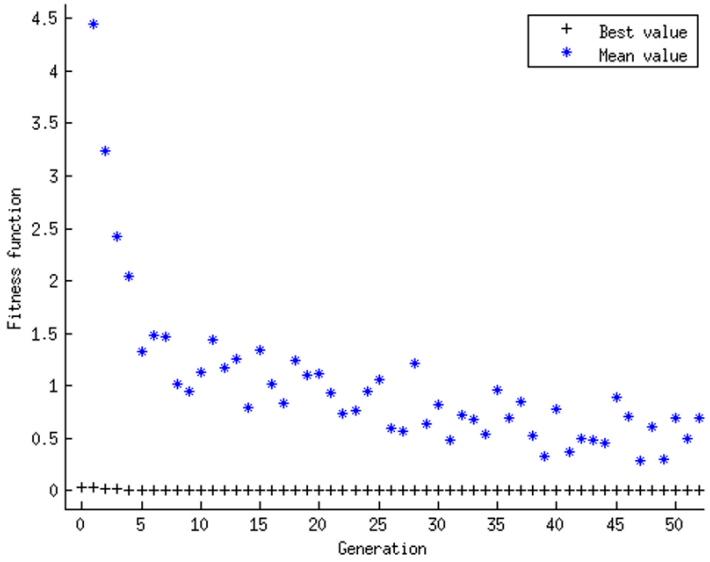

Figure 7. Optimization processes with OLTC system: best and mean value of the fitness function versus number of generations.

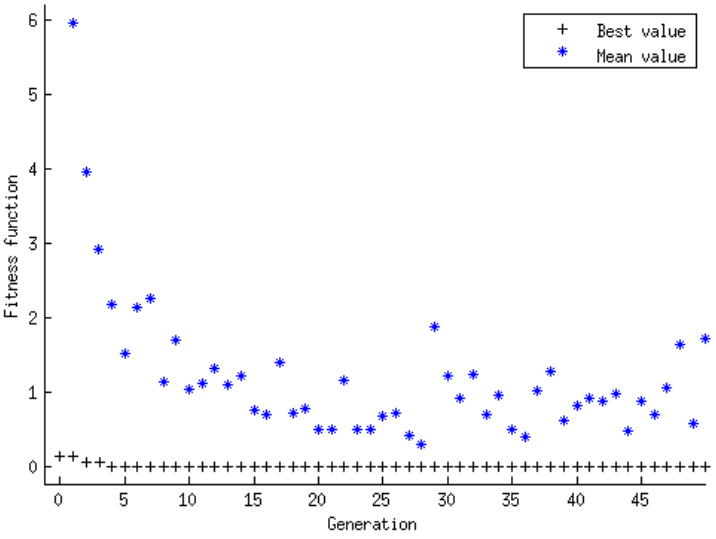

Figure 8. Optimization processes without OLTC system: best and mean value of the fitness function versus number of generations.

5. Conclusions

In this paper, a method for minimizing power losses in tap-changing TCP was proposed and implemented. The proposed method allows setting all TCP in one operation point where all transformers have similar power chargeability. The power chargeability balance allows reducing the quadrature components from transformer powers given to load due to circulating currents between TCP, guaranteeing power losses minimization. Furthermore, the optimization process takes into account load-voltage constraints; hence, transformers taps are obtained so that the load voltage remains within the admissible range. The optimization process delivers the transformer tap positions in the best operation point taking into account the constraints in power chargeability balance and load voltage; in consequence, the proposed method can be used for changing tap positions in conventional OLTC systems with different load profiles. In addition, the proposed method can be used in manual controllers without OLTC system. In this case, the tap positions must be fixed throughout the operation period.

The main contribution of the paper is a model for minimizing power loses in TCP that considers different parameters such as: short-circuit impedance, rated power, rated primary voltage, rated secondary voltage, tap step percentage and tap numbers. Therefore, a general method is proposed for optimizing the TCP operation even if transformers have different construction features. Several tests performed with three TCP showed the applicability of the proposed approach, being able to minimize power losses and keep voltage profile within an admissible range.

The test results show consistence between the two applications presented: with and without OLTC system. In the former application, the tap positions are obtained for each load profile setting the transformers in similar chargeability, guaranteeing power loss minimization; in the latter application, the tap positions are obtained for the most critical load profile; however, guaranteeing the best possible power chargeability balance while keeping load voltage within the admissible range for all load profiles. In the optimization performed considering the OLTC system, three different sets of tap positions were obtained (one for each load profile). However, without the OLTC system only one set of tap positions is obtained for all load profiles. It was found that despite of the flexibility provided by the OLTC system, lower voltage mismatches were obtained when a single set of tap positions is considered for all load profiles.

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