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IGBT Half-Bridge Power Switching Analysis Based on a Semi-analytical Point of View

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Abstract

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In this work a semi-analytical investigation is performed on an two level IGBT half-bridge topology under the assumption of constant current load. An analytical model is developed for turn on losses. Diode reverse recovery behaviour and its influence on power losses and turn on switching of opposite semiconductor are investigated upon a parametric consideration. Stray inductance, diode capacitances and conductances, IGBT capacitances, storage time and other factors are considered in order to analytically describe switching waveforms for a given semiconductor, but in a general frame that could be applied upon any other MOS type semiconductor. Turn off behaviour and losses are investigated upon a regression model. Data of simulation runs based on physical model of semiconductor are used in order to find turn off losses of IGBT. A statistical analysis is performed in order to encounter appropriate polynomial fitting of data.

Also, in order to describe a experimental verification tool for models developed, an indirect current measurement is performed. This is because transient behaviour of current is needed to be measured with high accuracy. The application circuit is a diode clamped-inductive. It is employed a digital data processing in which voltage across a wire is used as processed input data to obtain current through a series connected semiconductor.

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Abbreviations

IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PWM	**P**ulse **W**idth **M**odulation
VSC	**V**oltage **S**ource **C**onverter
CSC	**C**urrent **S**ource **C**onverter
NPT	**N**on **P**unch **T**hrough
RMSE	**R**oot **M**ean **S**quare **E**rror

Chapter 1

Introduction

Power losses on semiconductors within a power converter are of great importance in efficiency. In this research work analysis and calculation of power switching losses in IGBTs of a half-bridge two level converter is performed. From an analytical perspective, turn on switching behaviour is described by circuit and diode parameters applicable during reverse recovery process. Turn off losses are investigated upon a regression model which takes into account non-linearities of the semiconductor and results are backed up by statistical hypothesis. Measurement procedure is developed in order to show a tool for experimental verification. These models can be used to find total power losses in two level power electronic converters given conduction losses found by knowing the switching scheme.

1.1 General Work perspective

Efficiency is one of the major issues in power electronic converters. This makes necessary the investigation of power losses and its factors. Power losses are referred to heat dissipation in the different stages of a converter and represents power not consumed by the loads. Stages that dissipate power in a converter are, namely, driver circuit, measurement circuits, control circuits and power circuit. Among these stages, power circuit losses are the most important and, specifically, power semiconductors losses arise as the most important element to deal with [1].

Semiconductor power losses within a power converter have be investigated and found by measurements [2], by the aid of simulation programs [3], [4] and theoretical formulation [5]. There are several factors that must be taken into account when dealing with power semiconductor losses, namely, type of converter (AC-DC, DC-DC, multilevel), level of voltage (low, medium, medium-high, high), switching strategy (PWM, hysteresis), type of semiconductor (BJT, MOS type semiconductors-IGBT, MOSFET, IEGT-, thyristors), among others.

1.2 Literature Review

Semiconductor power losses are mainly split into two kinds: conduction losses and switching losses. Conduction losses are referred to the heat dissipation in the semiconductor when it is transferring power from load to the source or vice versa, this condition is referred to conduction state. Switching losses refer to the heat dissipation when semiconductor is changing its state, from conduction to blocking, or from blocking to conduction.

In the case of conduction losses, several works have been published. Methods are dependent on switching strategy, and in some cases, to the converter topology. In the case of predetermined switching strategies, some works [5], [6], [7], [8] deal with modulating functions needed to find the working conditions of semiconductors. In every case, load current is considered sinusoidal and static characteristics of semiconductors are needed to find voltage drop during conduction. Other works [9], [10], [11], [12] and [13] deal with the problem of undetermined switching strategies, switching function concept is used in order to find effective conduction through semiconductor.

In [5] conduction and switching losses are calculated for an IGBT in a PWM inverter. Conduction losses are found by stating a modulating function which defines duty cycle condition for conduction of semiconductors, namely, diode and IGBT. In [14] conduction losses expressions are derived for a neutral point clamped three level inverter modulated by PWM. Several PWM modulation techniques are considered in this study. The method is based on static characteristics of devices and duty cycle conditions. Conduction states for every device are determined based on switching scheme dictated by modulation strategy. In carrier-based PWM modulation techniques, four different modulating functions

are defined in order to describe effective change of state of each semiconductor. In the case of SVPWM technique, expressions for phase voltage equations are derived according to the region of modulation between 0 and 120 degrees. In [6] a four level inverter is presented and its total power losses are analysed for different switching strategies. Then, analysis of conduction losses is performed by defining duty ratio for each level of converter in every region of operation. In [7] an analytical derivation is performed in order to calculate conduction power losses on voltage and current source converters. In the case of conduction losses, they become expressions dependent on modulation index, power factor angle, peak current and Vdc.

Some other papers work the problem of conduction losses of undetermined switching strategies. In [10] a resonant DC-link, hysteresis current control and SPWM inverter are used to present a method to find power conduction losses by calculating the probability of on state of semiconductors. Probabilities are sinusoidal functions as load current and power are calculated by taking product of probabilities and instant power through semiconductors. In [15] a model for calculating power losses in a three phase SPWM inverter is derived based on switching function concept. Two switching functions are defined, one for calculation of phase voltages and phase currents are deduced by taking load impedances. Then the other switching function is used to calculate current through switches. In [9] an estimation of diode and IGBT losses is carried out under a hysteresis switching strategy. Test topology is a half-bridge where input data used for estimation are datasheet information of semiconductors used, load current, a switching function and dc bus voltage. The method consists in taking data of tests on the inverter, then a software to process, then to fit curves obtained by using points of current of datasheet information and apply a second order polynomial fitting of load current. Total losses are calculated and validated by using a calorimeter.

In the case of switching losses calculation, in some works the problem is treated by experimental data. In [16] a switching loss estimation method is employed for finding power switching losses of a Neutral Point Clamped multilevel converter based on a specific modulation method. The estimation method uses experimental waveforms of current and voltage through semiconductors of the converter along with datasheet information. Current and voltage waverforms of IGBT and diode are linearised using information like rise time, fall time, diode reverse recovery time, tail time, stray inductance and dc bus voltage. Estimation method includes a stage where modulation method can be

easily changed. In [17] a similar approach as in [16] is made for converters that employ cascaded H-bridge under several modulation methods. A similar method to linearise is used in [18], where an asymmetric shunt active power filter is analysed and compared to a symmetric one.

In [7], for voltage and current source converters, switching losses are calculated based on switching energies equations given by certain conditions of Vdc and load current given by semiconductor datasheet and then these equations are linearly scaled. In the case of CSC (Current Source Converters), switching losses are dependent on the same linearity and the same formula to calculate losses on VSC (Voltage Source Converters), but an additional fourier series is taken into account to describe voltage behaviour. In [5] rise time, fall time and reverse recovery time are considered linearly proportional to turn on, turn off and diode reverse current respectively in an SPWM inverter. In [15] switching losses in a three phase SPWM inverter are calculated by assuming linear relationship between energy and current at every transition. Energy in every semiconductor at every transition is approximated by second order polynomial functions of current through semiconductor.

In [19] a polynomial curve fitting is employed to calculate power switching losses of individual IGBT and diode of an H-Bridge sub-module of multilevel converter. Modelling of individual IGBT is carried out since thermal model is taken into account in order to get accuracy in determining losses. Turn on and turn off switching losses are calculated separately by finding constant coefficients. Model is validated on a voltage source converter based High Voltage Direct Current (HVDC) system. In [20] power losses are calculated on a SPWM two level inverter by taking power MOSFET and diode total conduction time. Switching losses are found by taking into account non-linearity of gate-drain capacitance and fall time of drain source voltage is calculated. Two distinct values of gate-drain capacitance are considered. The same is considered at turn off and average rise time is found. Turn on and turn off energy are calculated by integrating linearised current and voltage during average rise and fall times.

In [21] direct and square relationship between tail and recovery charge on load current of a PWM two-level inverter is used to build an averaged switched circuit model and predict switching losses. It is found that tail and reverse recovery losses are the most

critical at light loads, namely, a wind turbine. Also, a Neutral point clamped three level converter is employed to validate the results.

Behaviour of semiconductors, and namely, IGBTs are investigated within soft-switching circuits and its effects are clearly modified in regards to stand alone operation. Furthermore, the type of IGBT, analysed topology and commutation scheme must be taken into account [22], [23], [24] .

In [25], an investigation on losses of IGBT of type NPT and PT is performed in function of the kind of commutation, either soft or hard switching. A comparison of losses is carried out for zero-current switching, zero-voltage switching and hard switching. It is confirmed that PT IGBT is more affected by temperature than NPT type of similar characteristics at hard switching scheme. It is also found , that losses on PT device grow by 3 when temperature is increased from 25 degrees to 125 degrees at zero voltage switching; while NPT devices increase by a factor less than 1 under the same conditions.

In [26] a comparison of several high-voltage devices behaviour is performed at hard-switching and zero voltage switching condition. Zero-voltage-switching is carried out by using an Auxiliary Resonant Commutated Pole Inverter (ARCPI) within a Chopper topology. It is found there that ZVS (Zero Voltage Switching) has stronger impact on high-voltage devices than on devices with lower block voltage ratings. Also, it is found that Field-Stop (FS) diodes are more affected by hard switching in comparison to Soft Punch Through (SPT)-diode.

In [27] IGBT behaviour under a resonant snubber inverter at soft switching is compared to behaviour under hard-switching. Under zero voltage switching, Interaction between snubber capacitance and output capacitance is identified and its effect on tail current is analysed since current through output capacitance gets larger for a PT-type in regards to a NPT-type at turn off. It is found that, current tail duration is longer at turn off, but power losses are smaller as a consequence of reducing slope of collector emitter voltage. Also, turn on behaviour and the influence of diode reverse recovery is eliminated by employing snubber capacitor [28].

In [29] it is shown that reducing switching interval leads to reduction in switching times and therefore to reduction in switching energies both at turn on and turn off in NPT devices. This is confirmed by noticing that recombination of charge after turning off

is not completed, so turning on is faster and stored charge does not reach steady state condition at reduced duty cycles. In [30] two phenomena involved in switching of IGBT are outlined. First, dynamic tail charge at turn off which depends on current and its dynamics, it was found that this effect is more pronounced on NPT devices tested than on PT devices at high temperature. Second, dynamic conduction losses which is up to the frequency and makes turn on losses higher at higher switching frequency.

Some other works, namely, from manufacturers, deal with transient characteristics of diodes during reverse recovery. In [31] capacitive effects of diode during reverse recovery process are modelled. Distinct phases are analysed in detail and failure modes of operation are explained from the relationship between drift and junction capacitances given the amount of carriers at the end of recovery period. In [32] it is shown how rate of change of current and temperature affects diode performance, being diode more efficient and less energy consuming as speed increases, also at high temperature, diode reverse recovery current peak and time increase, being the case of current peak much more dependent on temperature than on current and voltage. Also, it is shown that additional capacitance in parallel with diode increases turn on losses of semiconductor (MOSFET or IGBT) and decreases turn off losses. In [33] a dependency of diode reverse recovery behaviour of a MOSFET body diode on gate voltage is outlined. It is seen there that keeping gate voltage within sub-threshold region and greater than zero and negative polarization improves recovery behaviour, making small reverse recovery current peak, and consequently making switching losses smaller. In [34] a MOSFET step down DC-DC converter is used to find out that body diode of synchronous rectifier reduces its reverse recovery charge during turn off if dead time is reduced (10 ns is found as an optimal point) and therefore, turn off losses are reduced.

Finally, IGBT simulation tools are up to the level of abstraction to be analysed, being system level and device level a good categorization in regards to off-line modelling [35]. In the case of device level, good accuracy is needed in order to realistically represent switching behaviour, power switching losses, thermal behaviour, non-linearities, breakdown, charge storage, MOS capacitances [4]. SABER and spice tools are useful in simulating these phenomena [36], [37] , [38]. In the system level category performance of power electronics system and its influence on power system, harmonic content, control performance, machine dynamics are of interest. Functional models and software tools like EMTP model or MATLAB simulink simulation tools arise [35].

However in the case of system level, some works deal with problem of accuracy. In [39] an EMTP modelling of IGBT during transient period is developed in order to improve simulation time in regards to other software programs. Simulation is based on the use of per-unit switching functions which model characteristic behaviour of IGBT at transient. In turn off transient, total time is considered constant and a per-unit switching function is scaled to the amplitude of current in steady state conditions. During turn on transient, diode reverse recovery is considered, and it is assumed that diode reverse recovery time is almost proportional to the square root of the ratio between current and rate of change of current. In [3] a transient simulation model is developed for an EMTP software of power semiconductors at high voltage systems. The model consists on the addition of a layer to the conventional semiconductor model used which updates parameter values by taking power switching losses computing and finding temperature. In this way transient behaviour is predicted or calculated by determining and updating parameters without the need of complex semiconductor models. Seed parameters are delivered by datasheet information. This is done since EMTP software only considers on/off behaviour of power switches by performing simulations at large time steps (several microseconds), while transient period of semiconductors is in the order of a few hundred of nanoseconds.

1.3 Problem to be solved

Given dependency of topology, switching scheme, type of semiconductor, circuit conditions, an exploration on behaviour of semiconductors within a half-bridge topology applicable to any type of two level hard-switched converter could be developed to meet the most important factors that affect performance of power converters. Also, given the necessity to meet accuracy, analytical depth, system considerations, simplicity, diode reverse recovery interaction and broad applicability, even flexibility for soft-switched topologies, it is necessary to develop a switching model. These characteristics must be applied within those switching schemes by which provided data are enough to calculate semiconductor switching behaviour and power switching losses, for instance, initial values of current through semiconductors at the beginning of switching periods.

Chapter 2

General Issues

In this chapter, main features about transient behaviour and measurement are outlined. In the first section, general issues of transient behaviour of IGBT are explained. Both turn on and turn off transient periods are explained. Then, main issues related to the measurement of current in semiconductors are presented. Oscilloscope and its main features are briefly explained. Some methods to perform measurement of current are also presented.

2.1 Transient Behaviour

In this section general transient behaviour of IGBT and factors related to the switching transient periods are explained. Both turn on and turn off transient periods are described. Also, diode reverse recovery process is outlined. Turn on period of commutation is described from IGBT capacitances and their process of charging. Turn off period is explained from a general perspective and the tail period. Diode reverse recovery process is explained from storage period and diode capacitances concept.

2.1.1 Turn on behaviour

Turn on transient period of an IGBT might be analysed by evaluating charging of its gate capacitances, both C_{gc} and C_{ge}. Circuit depicted in figure 2.1 is used as a reference to evaluate distinct intervals of turning on transient. Load connected at collector of

IGBT might be either resistive, inductive or both. In figure 2.2, different instants of times are bounded in order to describe each phase during transition from blocking state to forward state of an IGBT. Next, every interval of figure 2.2 is analysed according to the factors influencing it:

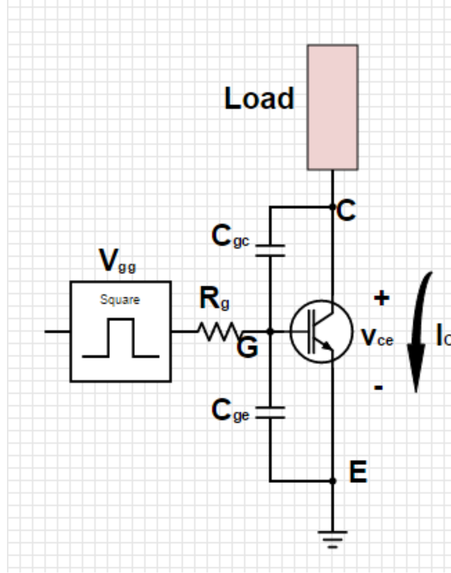


FIGURE 2.1: Gate circuit IGBT turn on and turn off

- Interval $t_0 - t_1$: At time t_0 a gate voltage V_{gg} is applied to the gate circuit of figure 2.1. Gate to emitter capacitance C_{ge} begins to charge through gate resistance R_g until gate emitter voltage reaches threshold value V_{gth}. No current flows through collector until threshold value is overcome.

- Interval $t_1 - t_2$: At the beginning of this interval, collector current begins to grow from zero almost linearly; a linear relationship given by equation 2.1 [40] could describe the active region of IGBT during turn on transient, where g_m is transconductance, V_{gp} is gate plateau level and V_{gth} is threshold level. At the end of this period C_{ge} has fully charged and gate charge has reached Q_{GS}.

$$I_C = g_m(V_{gp} - V_{gth}) \tag{2.1}$$

- Interval $t_2 - t_3$: Gate collector capacitance C_{gc} begins to charge, also gate-emitter voltage holds constant during this period keeping a gate plateau value V_{gp}. Consequently, collector emitter voltage begins to drop as a consequence of changing of gate-collector voltage across C_{gc} during its charging. At the end of this period,

total charge needed to switch collector current has been delivered to the gate. This stage is more complex than the shown in figure 2.2, since C_{gc} is inversely proportional to the collector emitter voltage level, which can be expressed by equation (2.2) [41].

$$v_{ce}(t) = V_{dc} - \frac{(V_{gg} - V_{gp})t}{R_g C_{gc}} \tag{2.2}$$

- Interval $t_3 - t_4$: Finally, saturation state of IGBT has been reached. Also, gate-emitter voltage must reach V_{gg} level and an exceeding amount of charge is collected by the gate through C_{ge} capacitance [42].

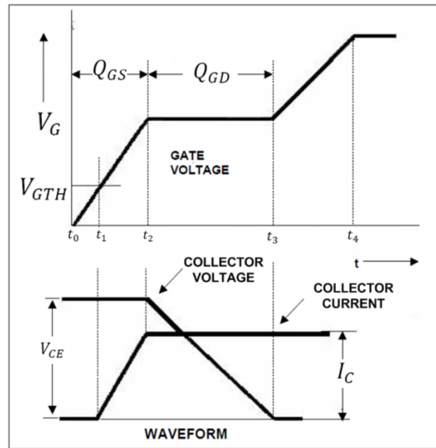


FIGURE 2.2: Turn on behaviour IGBT (adapted from [42])

Energy turn on losses can be defined as the integral of instantaneous power dissipation over the turn on switching time. Instantaneous power dissipation is the product of voltage and current along the turn on transient time. By taking the time during which current and voltage are simultaneously changing, energy can be calculated from t_0 to t_3 as expressed by equation 2.3. However, in practical terms, the integral is frequently calculated between the time when gate emitter voltage reaches 10% of its steady state value and the time when collector emitter voltage has fallen to 2% of its blocking level [43].

$$E_{onIGBT} = \int_{t_0}^{t_3} i_c v_{ce} dt \tag{2.3}$$

2.1.1.1 Obtainment of IGBT capacitances

IGBT capacitances as a function of collector emitter voltage are often delivered along with the datasheet of the device. However, C_{ge}, C_{gc} and C_{ce} are not obtained directly. These capacitances must be deduced by taking data of measurement of capacitances experimentally. In IGBT, these capacitances are output capacitance C_{oes}, input capacitance C_{ies} and reverse transfer capacitance C_{res}. Input capacitance is the measured gate-emitter capacitance when collector is shorted to emitter. Output capacitance is the capacitance between collector and emitter terminal when gate is shorted to the emitter. Reverse transfer capacitance is the miller capacitance between collector and gate [44]. These capacitances could be measured by short-circuiting respective terminals, adding a series capacitance of known value and then impedance is measured at a frequency of 1 MhZ, then equivalent measured capacitance is obtained and input capacitance is derived from the series [45]. In figure 2.3, data of measured capacitances of an IGBT irg4pc40fd of international rectifier are shown.

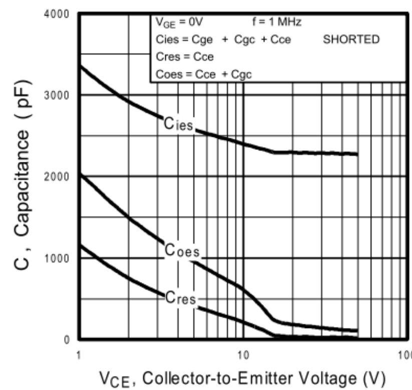


FIGURE 2.3: IGBT capacitances of an ir4pc40fd device(taken from [46])

2.1.2 Turn off behaviour

Turn off behaviour of IGBT is dependent on semiconductor characteristics. While turn on might be somehow controlled by means of external circuit (see equation 2.2), it is much more difficult to perform this task during turn off transient. While time during turn on can be considered highly dependent on IGBT capacitances and gate resistances, time to turn off IGBT is very dependent on both voltage and current magnitudes, being longer as voltage and load current is greater [40]. In this sense, tail period is

dependent on semiconductor characteristics and lifetime τ, that is, on rate at which minority carriers recombine during turn off. In this way is not possible to control tail period since excess minority carriers in drift region cannot be removed by reverse biasing gate emitter terminals of IGBT [44].

Tail period is up to the kind of structure of IGBT. PT (punch-through) structures are often built with an additional layer of n-type material near collector in regards to the NPT (non-punch through) structure [44]. In the case of NPT type, tail period is longer, however forward voltage is larger in regards to the PT kind.

Conversely to the case of turn on, gate emitter voltage begins to drop once V_{gg} is withdrawn. Turn off period could be analysed by observing at figure 2.4, where an inductive load is switched. Three distinct stages can be identified [40]:

- First stage of turn off begins by the increasing of collector emitter voltage as gate emitter capacitance C_{ge} is discharging. Gate emitter voltage falls to V'_{ge} and also current through collector falls below steady state value I_{CE}.
- At second stage, collector emitter voltage reaches blocking level V_{dc} and gate emitter voltage begins to drop below V'_{ge} and C_{ge} continues discharging.
- Third and last stage begins when gate emitter voltage falls below threshold level V_{th}. At this time, MOSFET portion of IGBT turns off and current through collector slowly decays beginning tail period.

2.1.2.1 Turn off times and Energy consumption

According to the IEC, turn off time t_{off} is the sum of turn off delay time and fall time. Although IEC standard does not define any percentages, it is often used the criterion by which turn off delay time t_d is taken as the time between 90% of v_{ge} and 90% of steady state value of collector current. Fall time could be taken between the end of turn off delay time and the time when current has fallen to 10% of its steady state value [43]. In every case, it is important to make sure that turn off time takes the whole transient period, and, in the case of waveforms shown in figure 2.4 turn off time is the sum of t_d and t_{fi}. Finally, turn off energy is calculated as the integral of current and voltage during turn off time as expressed by equation (2.4).

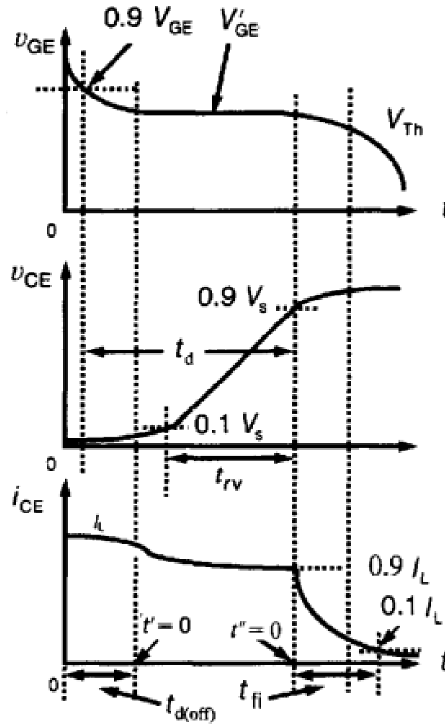


FIGURE 2.4: IGBT typical waveforms during Turn off (taken from [40])

$$E_{offIGBT} = \int_{t_{off}} i_c v_{ce}, dt \tag{2.4}$$

2.1.3 Diode reverse recovery behaviour

Diode reverse recovery process takes place when a fast diode must be turned off, that is, must be taken from its forward state to its blocking state [47]. It is frequently analysed by circuit of figure 2.5 when load is an inductive and a diode is connected in parallel to it, making a customary clamped inductive load circuit. In general terms, characteristic waveforms of diode reverse recovery process can be depicted as in figure 2.6. Initially, current through the diode begins to decrease until it crosses zero at t_0. Then, storage period begins from t_0 until t_w, at the end of which total excess carrier concentration of diode at pn junction is reduced to zero. From t_w on, capacitive effects take place as voltage across diode starts to increase until it reaches block level [31].

Referring to figure 2.6, total reverse recovery time (t_{rr}) could be defined as the time it takes diode to completely remove stored charge. Total reverse recovery time is the sum of two times: the time required for the diode current to reach its peak (t_{sa}) and the

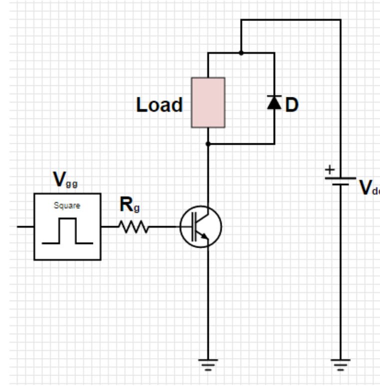


FIGURE 2.5: Diode clamped inductive load circuit

time it takes for the diode current to fall from its peak value to zero (t_f) [48]. However t_f could be defined as the time it takes for the current to fall from its peak value to 20% of that value [47]. Relationship between t_{sa} and t_f could be used to define soft factor $s_f = \frac{t_f}{t_{sa}}$ in order to minimise switching overvoltages (s_f should be greater than one), however a more fitting way to achieve this is by $\frac{di_r}{dt}$ which is the rate of change of current during t_f [48]. Total reverse recovery charge Q_{rr} is the area under current during t_{rr} (see figure 3.8). Energy dissipation during reverse recovery is calculated by taking instantaneous values of voltage and current along t_{rr} and then integrating. This computing is performed by taking the integral 2.5.

$$E_{rr} = \int_{t_{rr}} i_d v_d dt \tag{2.5}$$

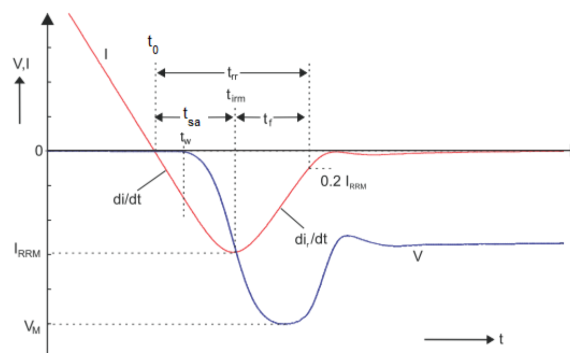


FIGURE 2.6: Diode reverse recovery behaviour of current and voltage(taken from [47])

2.1.3.1 Storage period

Storage period could be defined as the time from which current crosses zero (t_0) and the time when voltage begins to increase from its forward state(t_w). At the end of this time, total excess carrier concentration of diode at junction pn is reduced to zero and begins the formation of depletion region. This time is dependent on both external operating conditions and on diode structure [31]. In this way, storage period can be expressed by the equation (2.6).

$$t_s = t_w - t_0 \tag{2.6}$$

2.1.3.2 Conductance and capacitance of diode

After voltage across diode begins to increase, that is, after t_w in figure 2.6, capacitive effects take place. In this way, freewheeling diode can be modelled during its reverse recovery process as two capacitances in parallel with a conductance. Total diode capacitance is the sum of junction capacitance C_j which represents charges at both sides of pn junction after storage time has elapsed and of drift capacitance C_D, which is the capacitance associated with charges left in the drift region after diode voltage starts to increase [31]. These capacitances are dependent on diode recovery process and its speed, while conductance is a time dependent term needed in the model to fit behaviour of diode during reverse recovery. In this way, diode model can be drawn as that shown in figure 2.7.

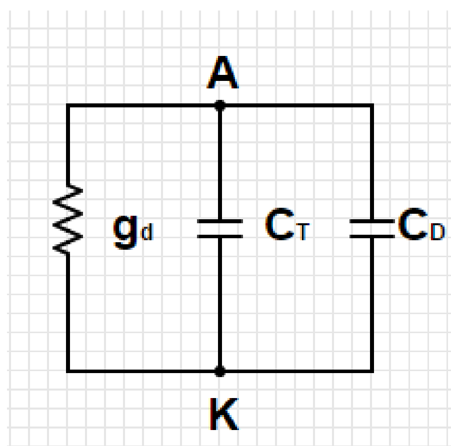


FIGURE 2.7: Diode model during reverse recovery process(adapted from [31])

2.2 Measurement issues

In this section, the main aspects that must be taken into account in order to perform measurement of currents and voltages through semiconductors are outlined. In order to measure power losses in semiconductors, current and voltage through them must be measured. As power switches get faster to commutate, measurement of voltage and current through them get harder to carry out.

Typically, a pulse train over the gate of fast power switches approaches a square wave. A square wave is compounded of infinite number of harmonic components and consequently its highest frequency component is infinite. However, no measurement system is able to accurately obtain these kind of signals. Furthermore, if an unfit measurement system is employed for a particular purpose, it could affect performance of measured system. Main issues like bandwidth, accuracy, PCB design and other factors must be considered in order to accurately measure high frequency current and voltage.

2.2.1 Measurement system issues

Typical measurement system to obtain, acquire and represent power semiconductor signals is the oscilloscope. Oscilloscope is an electronic measurement system that measure electrical signals and their variations over time. Oscilloscope can measure different kind of signals, however they need to be converted into electrical ones, and more specifically into voltage signals. It also means that current signals must be converted into voltage signals in order to see its variations over time. Several issues must be taken into account in order to evaluate the fitness of a given oscilloscope and voltage probes to accurately represent measured signals, namely: effect of oscilloscope impedance in measured system, bandwidth of measurement system.

2.2.1.1 Oscilloscope impedances

Given that oscilloscopes -in spite of the kind of signal to be measured- must take voltage signals and represent them on a screen, impedance of oscilloscope and auxiliary equipment used to take signals have to be large. Measurement system could affect the system to be measured if its respective impedances are comparable to the load connected in

parallel. As can be seen in figure 2.8, measurement system impedance could be represented in a simple way by oscilloscope impedances, probe impedances, and other series impedances between connections to the load.

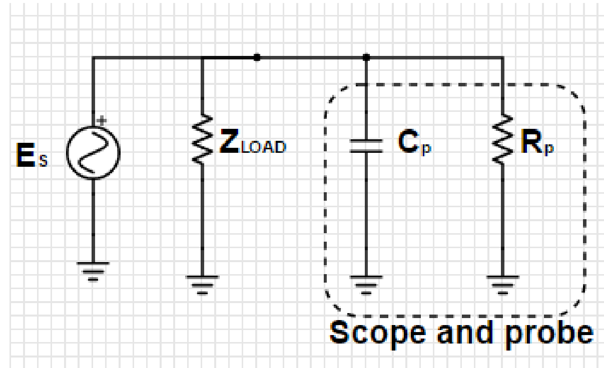


FIGURE 2.8: Oscilloscope and load impedances (adapted from [49])

By only considering shunt impedances, main factors to be accounted are shunt capacitance C_p and shunt resistance R_p. Both parameters must be small enough compared to Z_{load}; the first because at high load impedances, R_p will combine with Z_{load} making equivalent impedance shorter and consequently system to be measured modified. In the case of capacitance C_p, it must be small enough because at high frequencies of input sources E_s capacitive impedance gets shorter and can modify amplitude, phase and rise time of original signal [49].

2.2.1.2 Bandwidth and rise time

Bandwidth and rise time are frequently considered as two of the most important specifications of an oscilloscope and a probe. In the case of bandwidth, it is a measure of capacity of oscilloscope and the probe to represent on the screen sinusoidal signals of high frequency. It is specified as the frequency at which a sinusoidal input signal is attenuated to 70.7% of the signal's true amplitude [50]. As can be seen in figure 2.9 this means that as input load frequency gets larger and approaches bandwidth limit of measurement system, its represented amplitude will be attenuated on the screen by a given percentage. This bounds the user to select a measurement system whose bandwidth is almost five times the highest frequency component of signal to be measured. It is important to point out that both oscilloscope and probe could have different bandwidth specifications. In this way, total system bandwidth is always shorter than the smaller bandwidth. The probe's bandwidth must exceed oscilloscope's bandwidth [49].

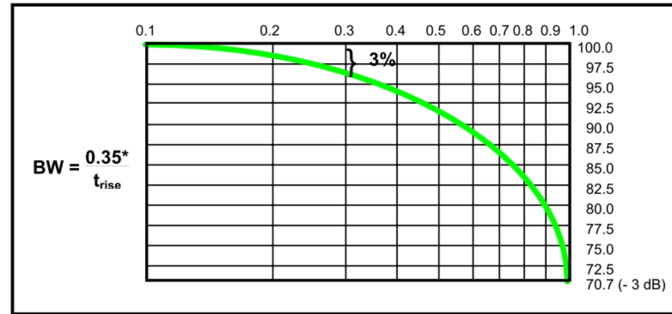


FIGURE 2.9: Percentage of attenuation as a function of frequency for a given system bandwidth (taken from [51])

However, rise time is also very important since it is much easier to measure the shortest transition of a signal than its highest frequency component, especially of step and pulses. In this case, oscilloscope rise time must be 5 times smaller than the fastest rise time of signal to be measured. Rise time of oscilloscope could be calculated by $BW = \frac{k}{risetime}$, where k could be 0.35 or 0.45 if bandwidth of oscilloscope is less than 1 GhZ or greater than 1 GhZ respectively [50].

2.2.1.3 Other effects and specifications

Other constraints that must be taken into account when measuring high frequency signals on a oscilloscope, and specifically, a digital one are: sample rate, record length, vertical sensitivity, vertical resolution, among others. Record length and sample rate are related to the quantity of points displayed on the screen and the interval of time taken at one display, the first refers to the quantity of points displayed and the latter to distance between points. Sample rate must be almost twice the highest frequency component of signal (Nyquist's theorem). Vertical resolution and vertical sensitivity are indicatives of accuracy of measuring. Vertical sensitivity represents the smallest voltage that could be measured and amplified at oscilloscope (given in millivolts per division). While vertical resolution is a indicative of the accuracy of ADC system in bits, being more accurate as the number of bits is larger [50].

In the case of probes, specifications like aberrations and attenuation factor are parameters that indicate how signal taken by the probe is affected by the probe. Aberration is an amplitude deviation from expected response of a measured signal, it is given as a percentage of final steady state value of a pulse signal. Attenuation factor indicate

how much a probe can reduce signal measured amplitude. Higher attenuations factors represent higher input resistance since voltage divider are employed [49].

2.2.2 Current measurement

There are several methods to perform measuring of current at high frequencies in a power converter. Measurement of current, as in any other measurement system, requires accuracy, resolution and other factors that need to be improved in order to get measurements reliable have to be met. Furthermore, current through fast semiconductor is characterized by fast transitions (in the order of nanoseconds for IGBTs and MOSFETs) with no possibility of obtainment by slow sensors. This makes current measurement in a power semiconductor very dependent on rise time and bandwidth characteristics of current sensors [52]. Next, some of the methods among which measurement of current is accomplished are briefly explained.

2.2.2.1 Hall Effect sensor measuring

Measuring of current by hall effect sensor is based on Lorentz force. Charges moving on a magnetic field are subjected to a force that is proportional to the magnetic field. By employing Hall effect principle, within a conductor where current to be measured is flowing, and also, a magnetic field is present, a voltage across terminals of conductor is developed. As depicted in figure 2.10 measured current i flows through a conductor, this generates a magnetic field enclosed by a magnetic core with high permeability and an air-gap δ and whose strength is H. Within the air-gap, across the terminals of a conducting plate a voltage u_H is generated and a current i_s flows through it. Transfer relationship of hall effect current sensor is given by equation 2.7 [53].

$$u_H = R_H \frac{i_s \mu_0}{d\delta} i = k_H i \tag{2.7}$$

Where R_H is the Hall coefficient and must be determined by calibration, d is the thickness of conducting plate, δ is the air-gap length and μ_0 is the vacuum permeability.

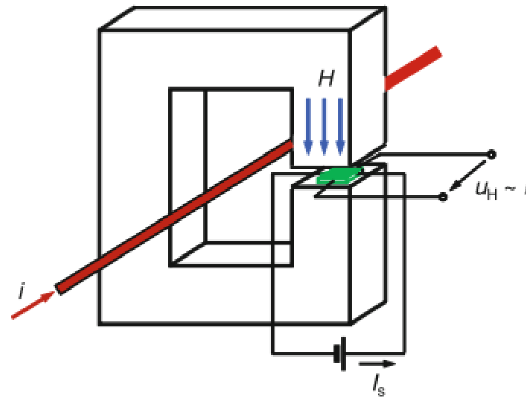


FIGURE 2.10: Hall effect principle diagram (taken from [53])

2.2.2.2 Coaxial shunt

Coaxial shunt is a measurement device by which current measurement is performed by taking voltage across a resistive tube. Coaxial shunt is connected in series with circuit where current is to be measured. Current comes in at input terminal, pass through a resistive tube and returns through return conductors connected at the opposite side [53]. By its construction characteristics, coaxial shunts have the great advantage of no having inductive effects on it. All coupling effects of inductance are eliminated by making current flow through a pure resistive path. It is provided by a shell that will avoid external fields [54]. Current step response of a coaxial shunt is given by the series expressed by the equation 2.8 [53].

$$g(t) = 1 + 2\sum_{k=1}^{\infty}(-1)^k e^{\frac{-k^2\pi^2}{\mu_0 \sigma d^2}t} \tag{2.8}$$

Where d and σ are the wall thickness of tubular resistors and the conductivity of tubular resistor respectively in mm and $\frac{m}{\Omega mm^2}$ and μ_0 is the vacuum permeability. This response is plotted in figure 2.11 for 3 different values of thickness and it is seen that there is no peaks related to inductive effects [53].

2.2.2.3 Rogowski Coil measurement

Principle involving measurement of current by Rogowski coil is induction of a voltage across terminals of a toroid. Path where current has to be measured is wrapped by a

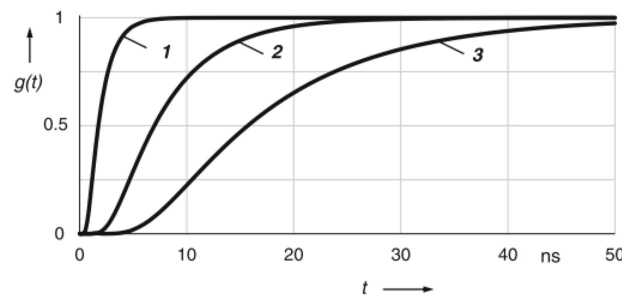


FIGURE 2.11: Current step response of coaxial shunt at $d = 0.1mm$ (1), $d = 0.2mm$ (2) and $d = 0.3mm$ (3)(taken from [53])

toroid, this current produces a field along the axis of toroid and then a current through coils will induce a voltage across its terminals. This voltage is proportional to the change of original current, and, therefore, this must be integrated in order to obtain current. A great advantage of this system is its little influence on measured circuit since there is not electrical connection. However, a drawback is the need of using high frequency operational amplifier to take signals of voltage without missing transient behaviour. Another drawback is the effect of leakage inductance and shunt capacitance on circuit at high frequencies that must be taken into account when finding transfer relationships [55]. System of measurement by Rogowski coil is shown in figure 2.12, where operational amplifier as integrator at the output of terminals of coils is shown.

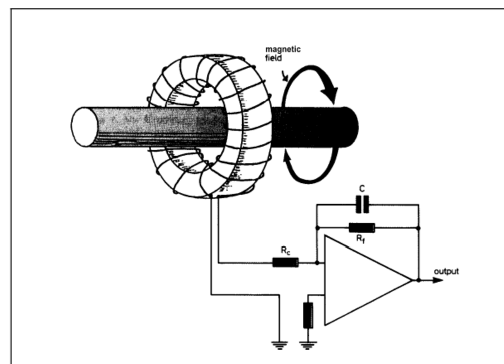


FIGURE 2.12: Rogowski coil measurement system (taken from [55])

2.2.2.4 Current transformer

Unlike Rogowski coil, current transformers have magnetic core. A current transformer has the same principle as voltage transformer. It is built by a primary winding put in series with semiconductor and a secondary winding that often has much more turns

than primary. Current is obtained by calibrating a linear relationship between turns ratio, burden and voltage across secondary winding, which is the measured variable. The main advantages of measuring by current transformer is galvanic isolation, high frequency response and low power loss (since primary winding has few turns, often one). Drawbacks include its useless at measuring DC currents, their high cost, its size and saturation at high current ratings [56].

2.2.3 Taguchi's Methodology

Now, aspects of Taguchi's experiment method are described. Taguchi's philosophy is intended to the design of robust systems. Robust system from this point of view means that the design of systems needs to take into account variability of the mean response of a main variable. This variability is correlated to the noise and factors that are out of control of the system. Taguchi's conception defines this variability in systems as "loss to society" and must be diminished in order to optimize designs. This loss is depicted as function loss and minimizing that function for a specific combination of parameters of the process is the target of the Taguchi's method [57].

2.2.3.1 Signal to noise ratio

Usually, minimizing loss function could be carried out by minimizing signal to noise ratio of a process where mean value must be obtained as reliable as possible. In this sense, it is useful for this task to use a relationship for signal to noise ratio given by the equation 2.9 [58].

$$SN = \frac{power\,of\,signal}{power\,of\,noise} = \frac{sensitivity^2}{variability^2} \tag{2.9}$$

This relationship entails several characteristics that must be taken into account, especially at measuring a given signal. One of them is linearity, which means that system relation input/output must be linear in order to guarantee a true measure. If noise is introduced or present in system, other factors not considered in the model could damage linearity, and therefore reliability of measuring system. Other characteristic is the sensitivity of system, which is related to the range of measures that can be read from

an instrument. As signal to noise ratio is less, noise is greater and therefore only signals much greater than noise could be measured without misleading effects. Finally, variability affects directly accuracy of system, needing larger intervals of tolerance and therefore making it barely reliable [58]. In summary, all these issues can be fully, or partially, avoided by maximizing signal to noise ratio, or, in Taguchi's jargon, minimizing function loss.

2.2.3.2 Taguchi's experiment procedure and L-arrays

In order to reduce signal to noise ratio, process must be identified and factors that affect signal to noise ratio must be determined. In this way, signal response or results of measurement could get affected by several factors that could damage accuracy. For instance, measuring of ohmic resistance might be affected by factors like temperature, sensitivity of ohmmeter, additivity of lead resistance to the measure, etc. An experiment intended to reduce the effect of these factors must take into account several levels for temperature, different instruments with several sensitivities and different cables with various lead resistances, among other factors.

The process for arranging such a experiment can be carried out by employing L-arrays. L-arrays are matrices where rows indicate every run to perform the experiment, whereas columns indicate factors to be varied. The elements inside the matrix indicate levels of the respective factors in every run. L-array is denoted by letter L followed by a subscript indicating the number of rows, that is, the number of runs. L_i indicates an L-array for performing an experiment whose number of runs is i. Up to the number of factors and levels, an specific L-array is employed, for example, an L_8 could be employed where there are from two to seven factors with 2 levels each, an L_{16} from four to fifteen factors with 2 levels each, an L_9 from two to four with 3 levels each and so on [57]. In table 2.1 a L_4 array is shown, where factors are arranged in columns 2, 3 and 4 and there is another column which indicates signal to noise ratio. The elements of the columns are respective levels of factors and indicate levels of factors to be run in each experiment.

Last column of table 2.1 indicates the signal to noise ratio found at every run of the experiment. Up to the process to be studied and the kind of response desired, signal to noise ratio could be found according to table 2.2. Where STB (Smaller-The-Best) indicates a process where making response variable as small as possible is intended. LTB

Table 2.1: L_4 array and factors (adapted from [57])

Experiment \ Factor	$Factor_1$	$Factor_2$	$Factor_3$	$SN\,ratio$
1	1	1	1	SN_1
2	1	2	2	SN_2
3	2	1	2	SN_3
4	2	2	1	SN_4

(Larger-The-Best) where characteristic response must be maximized. NTB (Nominal-The-Best) indicates a process where variability must be reduced. In type I (NTB I), variability of positive values must be reduced, while in type I (NTB II) also variables that take negative values into account [58].

Table 2.2: SN ratio according to the kind of process (adapted from [57])

Kind of process	$SN\,ratio$
STB	$-10\log\frac{1}{n}\sum_i^n Y_i^2$
LTB	$-10\log\frac{1}{n}\sum_i^n \frac{1}{Y_i^2}$
NTB I	$10\log\frac{1}{n}\sum_i^n \frac{Y_i^2}{S^2}$
NTB II	$-10\log\frac{1}{n}\sum_i^n S^2$

In table 2.2 n is the number of data collected for variable Y, Y_i is the data of variable taken at sample i and S is the sample variance. In this way, every $SN\,ratio$ is computed at every experiment of table 2.1 but taking the number of replicates as n. Then, average $SN\,ratio$ of $Factor_1$ at level 1 is computed by adding SN_1 and SN_2 and then divide it by 2, this is done for the remaining factors as shown in variance table of table 2.3.

Table 2.3: Variance table from $SN\,ratios$

Level \ Factor	$Factor_1$	$Factor_2$	$Factor_3$
1	$\frac{SN_1+SN_2}{2}$	$\frac{SN_1+SN_3}{2}$	$\frac{SN_1+SN_4}{2}$
2	$\frac{SN_3+SN_4}{2}$	$\frac{SN_2+SN_4}{2}$	$\frac{SN_2+SN_3}{2}$

Chapter 3

Modelling power switching losses

In this chapter, IGBT switching power losses analysis is performed. First, turning on analysis is carried out by analysing main factors that model behaviour of current and voltage both on diode and on IGBT; then, turn on power losses are calculated and compared to simulation results. In the second part of the chapter, turning off analysis is performed by statistical analysis at various current and voltage operating conditions.

3.1 Half-Bridge circuit under consideration

In this section circuit under consideration both under turning on and turning off process of IGBT is presented. In figure 3.1 a Half-Bridge circuit with load connected at ground of dc bus is depicted. Regardless of switching scheme, and as a matter of analysis only, it is considered that either down or up IGBT is commutating just when the opposite switch has already commutated and only its respective diode is conducting. Also, along this chapter it will be considered that load current is constant and has reached a steady state value.

3.2 Analysis of turn on period of commutation

In this section, a general description of mechanisms of IGBT switching turn on is outlined. Analysis is performed on the circuit shown in figure 3.1 where one IGBT (either UP or DOWN) is turning on and the opposite frewheeling diode at collector is turning

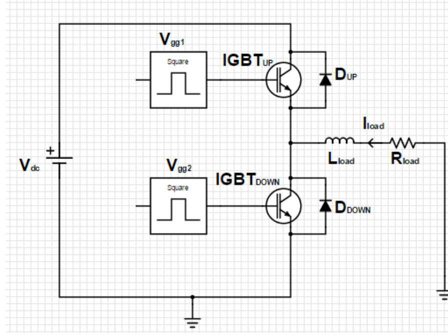


FIGURE 3.1: Half-Bridge circuit

off under reverse recovery process. The analysis is carried out during two phases: a) During turning on transient of IGBT b) During reverse recovery process of freewheeling diode. Ordinary differential equations are solved to find current and voltage during turn on phases. Parameters of differential equations are found by using simulation data. Finally, power losses are computed by taking voltage and current product and results are compared to simulation data.

3.2.1 Circuit analysis of Turn on period

In figure 3.2 a simplified diagram of circuit of figure 3.1 is depicted, but now stray inductances and resistances are being considered. This simplified circuit will be used to analyse turning on of DOWN (or UP) IGBT . In this analysis $IGBT_{DOWN}$ is considered. It must be assumed here that current through load does not change at all during this period of commutation. This is because load inductance is much greater than stray total inductance of the circuit, and then current through load inductance does not change as quickly as current through stray inductance. By applying current Kirchhoff's law on point x and since I_{load} is constant, equation for currents through IGBT and diode are expressed by equation 3.1 and 3.2.

$$I_{Load} = i_{diode} + i_{IGBT} \tag{3.1}$$

$$\frac{di_{diode}}{dt} = \frac{di_{IGBT}}{dt} = \frac{di}{dt} \tag{3.2}$$

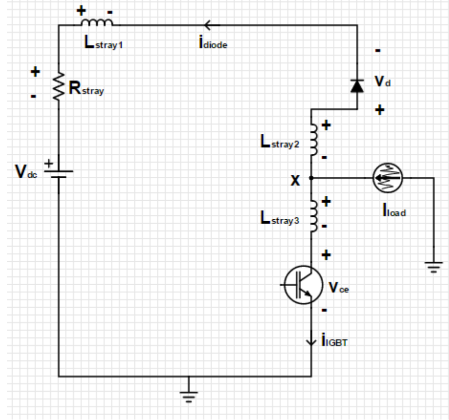


FIGURE 3.2: Circuit diagram of analysis

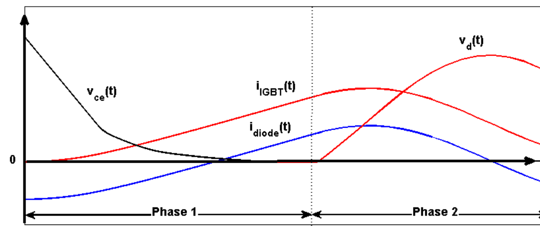


FIGURE 3.3: General behaviour of current and voltage on IGBT and diode

Since current is growing in all the stray inductors (current through diode is becoming less negative), an electromotive force is created across the inductors which is opposed to the change of magnetic flux. This, in the circuit diagram of figure 3.2 is represented by the polarities shown for every stray inductor. By applying voltage Kirchhoff's law, voltage across each element can be expressed by equation 3.3.

$$V_{dc} - L_{stray}\frac{di}{dt} - v_d(t) - v_{ce}(t) + iR_{stray} = 0 \tag{3.3}$$

In this expression, L_{stray} has been simplified as the sum of L_{stray1}, L_{stray2} and L_{stray3} since variation of current through IGBT and diode are the same according to equation 3.1.

Next, an analysis of circuit of figure 3.2 is performed according to two phases of behavior of the current of the diode, like the one shown in figure 3.3 . First, diode current and v_{ce} voltage are analysed while diode begins to increase from its steady state (negative). Then, when voltage across diode begins to increase from its forward saturation level.

3.2.1.1 First Phase: IGBT turn on

In the first phase, diode current begins to increase from the most negative point. At this time, also current through IGBT begins to increase from zero. In this stage, gate-emitter voltage has reached its threshold value, and also, it might be assumed that gate emitter capacitance C_{ge} has already been charged. Therefore, in this stage, miller capacitance is charging and gate-emitter voltage is constant with a plateau value of V_{gp}. Once miller capacitance has been charged, IGBT collector-emitter voltage v_{ce} reaches saturation level and, therefore, current rate of change is constant (see equation 3.3 with $v_{ce}(t)$ and $v_d(t)$ constant). Once current has crossed zero point, after the storage period of the diode (time required for depletion of charges), voltage across the diode begins to increase. This phase of commutation should be described by the equation 3.4, that is, a first order differential equation with a time-dependent term $v_{ce}(t)$.

$$\frac{di}{dt} = \frac{V_{dc} + V_{dsat}(t)}{L_s} - \frac{v_{ce}(t)}{L_s} \tag{3.4}$$

In equation 3.4, $v_{ce}(t)$ behaviour is dependent on both miller capacitance and gate resistance, according to the equation for v_{ce} (see equation 2.2 in chapter 2). Also, in this equation, L_{stray} has been renamed as L_s.

3.2.1.2 Second Phase: Capacitive Effects(Diode reverse recovery)

At the beginning of second phase both v_{ce} and v_d stay on their saturation levels and current continues to grow linearly since $\frac{di}{dt}$ is constant. This stage lasts as long as storage time has elapsed. Once storage time has elapsed, diode voltage begins to grow until it reaches the block reverse level (V_{dc}). Finally, after diode voltage reaches block level, diode current and voltage begin to oscillate according to the reverse recovery behaviour of diode. Diode capacitors (junction capacitance and drift capacitance) along with series stray inductance make the system behave as a second order system [31].

By replacing symbol of diode depicted in figure 2.7 and representing C_j and C_D together as C_T into the figure 3.2, and also taking just one stray inductance in series with diode and naming it as L_s, load current is eliminated from the circuit and only its value is

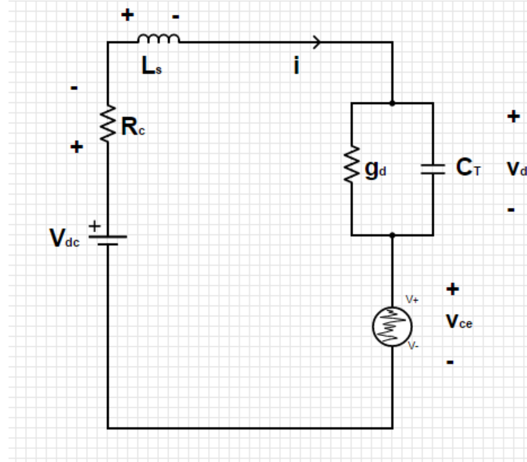


FIGURE 3.4: Circuit diagram for analysis of diode reverse recovery process

used as initial condition for current, circuit representation of figure 3.4 now describes electrical behaviour of system under capacitive effects of diode.

By applying voltage Kirchhoff's law on circuit, and also current through diode capacitance C_T, equation 3.5 and 3.6 are obtained.

$$V_{dc} = iR_c + L_s \frac{di}{dt} + v_c(t) + v_{ce}(t) \tag{3.5}$$

$$i = C_T \frac{dv_c}{dt} + g_d v_c(t) \tag{3.6}$$

Where i is total current through circuit, v_c is voltage across freewheeling diode, R_c is stray resistance and $v_{ce}(t)$ is voltage across IGBT (found by equation 2.2). By taking derivative of 3.5 and solving 3.6 for $\frac{dv_c}{dt}$ and making some additional algebraic manipulations, second order differential equation 3.7 is obtained (adapted from [31]).

$$\frac{d^2i}{dt^2} + \frac{R_c C_T + L_s g_d}{L_s C_T}\frac{di}{dt} + \frac{1 + R_c g_d}{L_s C_T} i + \frac{1}{L_s}\frac{dv_{ce}}{dt} + \frac{g_d}{L_s C_T} v_{ce}(t) = \frac{g_d}{L_s C_T} V_{dc} \tag{3.7}$$

Which is a second order differential equation of variable i with time dependent terms ($\frac{dv_{ce}}{dt}$ and v_{ce}).

3.2.2 Simulation Tools

In figure 3.5, simulation diagram used to obtain several parameters of differential equation that model current and voltage on both IGBT and diode is shown. Also, this diagram of simulation is used to compare the results of the model with data of LTspice. By using data of simulation of LTspice, storage time, conductance and capacitance of diode will be estimated. The simulations are run for several values of current of the load (the current source I_{load}), several values of DC bus voltage (V_{dc}), stray inductance (L_{stray}) and gate resistance (R_g), R_{stray} is the stray resistance. U1 and U4 are IGBTs whose model is an irg4pc50fd ([59]) of International Rectifier. Freewheeling diodes are body diodes of U1 and U4. This is a fast IGBT rated at collector current of 39 amperes and collector emitter voltage of 600 volts. It must be stated here that measured data regarding losses and other parameters are applicable to this device, but, by starting an analysis from a broad perspective, results and methodology could be applicable to other devices.

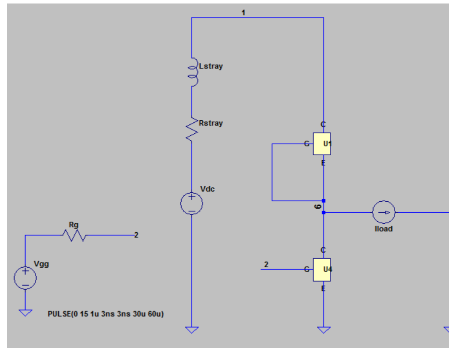


FIGURE 3.5: Diagram of simulation on LTspice

3.2.3 Obtainment of parameters for differential equations used

Differential equations of last section could be solved if the parameters are determined. In the case of the first order differential equation applicable during the first phase (equation (3.4)), parameters of equation for v_{ce} (equation 2.2) voltage must be obtained. Gate plateau voltage V_{gp} and miller capacitance C_{gd} are both characteristics that change as the conditions of the circuit change. In the case of second phase of capacitive effects of diode, parameters of second order differential equation 3.7 must be determined, namely diode capacitance and conductance are obtained by applying logarithmic decrement.

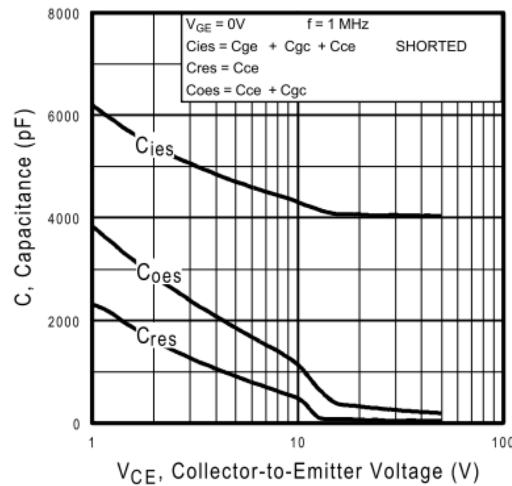


FIGURE 3.6: IGBT capacitances irg4pc50fd (taken from [59])

Also, storage time as a value needed to find initial value of current at the beginning of second phase is investigated.

For this task, characteristics of IGBT are needed along with data of simulations. Along this subsection, several runs of simulations have been carried out to estimate conductance and storage time. Specifically, referring to diagram of figure 3.5, DC bus voltage V_{dc} has been varied from 20 to 400 volts, load current I_{load} from 5 to 30 ampere, gate resistance R_g from 2 to 200 ohms and stray inductance L_s from 1nH to 100uH, V_{gg} is square wave of low value 0 volts and high value 15 volts, while R_c has been kept at 0.1 ohm along all simulations.

3.2.3.1 IGBT capacitances estimation

IGBT capacitances as a function of collector emitter voltage are delivered along with the datasheet of the device (see figure 2.3 in chapter 2). In figure 3.6, these capacitances are shown for an IGBT irg4pc50fd.

By using data from IGBT datasheet, gate collector capacitance (along with the remaining parasitic capacitances) are derived. All these capacitances are in function of v_{ce} univocally, and therefore a look up table is built which always has to relate a value of capacitance with only one value for collector emitter voltage. In the equation 2.2 C_{gc} capacitance is needed in order to find out collector emitter voltage. In figure 3.7, IGBT capacitances are shown after retrieving data from datasheet.

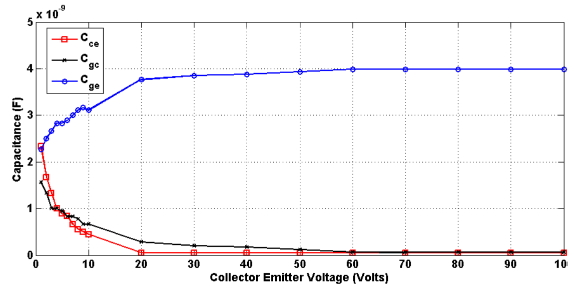


FIGURE 3.7: IGBT capacitances as a function of collector emitter voltage

3.2.3.2 Storage time obtainment

As suggested by equation 2.6, storage time of diode must be obtained by taking difference between time when current crosses zero point and time when voltage begins to increase from forward condition. In this case, voltage zero crossing is taken as the end of storage time as can be seen in figure 3.8. Storage time has been measured for several simulation runs. Gate resistance R_g, stray series inductance L_s, dc bus voltage V_{dc} and load current I_{load} have been swept at different levels. For instance, in figure 3.9, behavior of storage time as a function of voltage is shown when current is 15 ampere (figure 3.9b) and when current is 30 ampere (figure 3.9a) at several stray inductances. Especially at small values of inductance, this time could be assumed as constant with voltage.

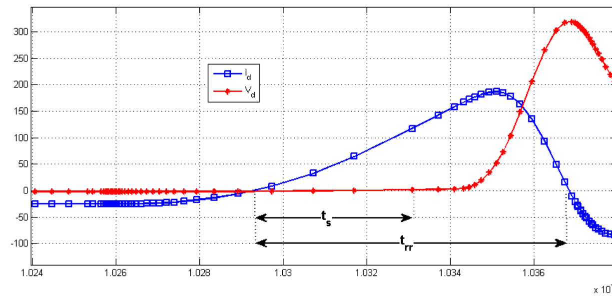
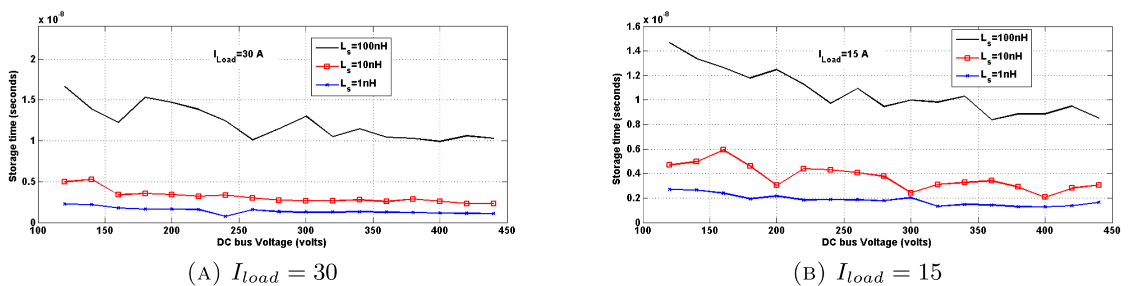


FIGURE 3.8: Zero crossing diode voltage and current, storage time



(A) $I_{load} = 30$ (B) $I_{load} = 15$

FIGURE 3.9: Storage time at different voltages and stray inductance.

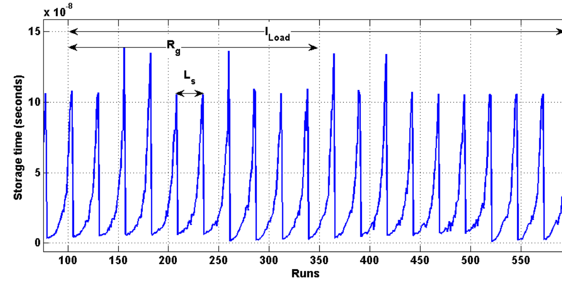


FIGURE 3.10: Storage time for all runs

Also, by varying gate resistance, load current and stray inductance, it could be observed that storage time is most dependent on latter. In figure 3.10, runs from 100 to 600 of a simulation in LTspice are shown. In which current has been varied from 5 to 30 amperes, gate resistance from 2 to 200 Ω, and stray inductance from 1 nH to 100 μH. The narrowest order of runs represents variations in inductance (26 runs straight), while the next narrower variation are gate resistance which is varied every 26 runs and finally I_{load} which is varied every 260 runs.

As it can be seen in figure 3.10, storage time could have an exponential dependency on stray inductance. Although several effects of voltage, current and gate resistance might be missed by only taking the effect of inductance, it has been seen that this dependency is a good approximation, especially at values of inductance between 10 nH and 10 μH (see figure 3.12). In this way, a regression model for storage time is proposed as expressed by equation 3.8

$$t_s = K_1 Ls^{K_2} \tag{3.8}$$

Which is a non-linear equation of K_1 and K_2 and where K_1 and K_2 are constants to be determined and L_s is the stray inductance. In order to make the equation a linear one and also, in order to find constant coefficients, natural logarithm is taken on both sides of equation 3.8 thus, we can hold equation 3.9

$$\ln t_s = \ln K_1 + K_2 \ln L_s = K_1 + K_2 \ln L_s \tag{3.9}$$

Which is a linear equation and could be expressed as a linear system by equation 3.10

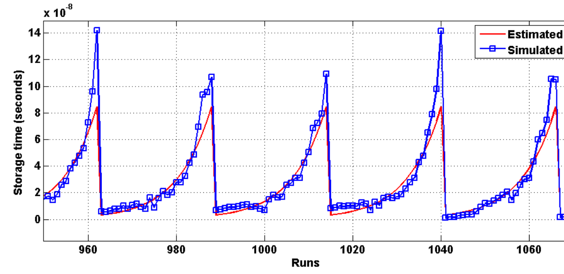


FIGURE 3.11: Storage time estimated for several runs

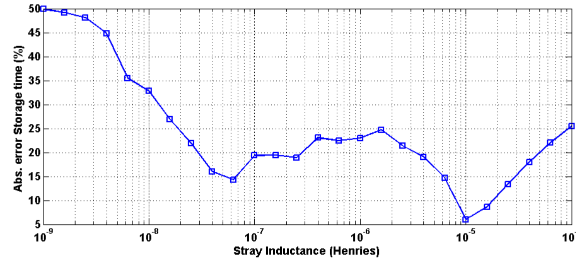


FIGURE 3.12: Absolute average error storage time

$$[\ln t_s] = A * K \tag{3.10}$$

Where $\ln t_s$ is a vector containing n elements from n runs of simulation data of storage time. A is a 2-by-n matrix whose first column is built of ones and second column is built of $\ln L_s$. K is the 1-by-2 coefficient vector to be found. K is found by taking pseudoinverse of matrix A, then, t_s is once again calculated by equation 3.11.

$$\hat{t_s} = e^{K[1]} L_s^{K[2]} \tag{3.11}$$

In last equation, $K[1]$ and $K[2]$ are the elements of vector K found by equation 3.10. In figure 3.11, both estimated and simulated t_s are shown for several runs of simulation. Also, in figure 3.12 absolute average error is calculated for each run that keeps constant stray inductance value. As can be seen there, error gets smaller as stray inductance takes values from few decs (10^{-8}) of nanohenries to values of tens of microhenries (10^{-5}).

3.2.3.3 Conductance and diode capacitance obtainment

In differential equation (3.7), characteristic parameters can be distinguished. Namely, damping ratio ξ and undamped natural frequency ω_n which can be found by 3.12 and

3.13.

$$2\xi\omega_n = \frac{R_cC_T + L_sg_d}{L_sC_T} \tag{3.12}$$

$$\omega_n^2 = \frac{1 + R_cg_d}{L_sC_T} \tag{3.13}$$

If R_c and L_s are known parameters of the circuit, ξ and ω_n are parameters measured from several runs of simulations (or experimental data), both C_T and g_d can be found by solving last set of equations. However, ξ and ω_n must be somehow determined. This could be performed by using logarithmic decrement on data of diode current while vanishing and oscillating during recovery process. In figure 3.13 variables needed to carry out logarithmic decrement on data of current and voltage are illustrated. Two periods of oscillations ($2T_d$) and magnitude of peaks (X_1 and X_3) at which periods are taken are measured from wave of current on diode (I_d). Where $W_d = \frac{2\pi}{T_d}$ is the damped natural frequency of system. Logarithmic decrement is applied as follows, where n is the number of periods taken (our case $n = 2$):

First, find δ by 3.14

$$\delta = \frac{1}{n}(\ln(\frac{x(t)}{x(t+nT)})) = \frac{1}{2}(\ln(\frac{x_1}{x_3})) \tag{3.14}$$

Then, find ξ by 3.15

$$\xi = \frac{1}{\sqrt{1 + \frac{2\pi}{\delta}}} \tag{3.15}$$

Finally, ω_n is found by

$$\omega_n = \frac{w_d}{\sqrt{1 - \xi^2}} \tag{3.16}$$

Now, a similar procedure for obtaining storage time is carried out to find conductance. Equation 3.17 relates conductance and stray inductance exponentially. This relationship

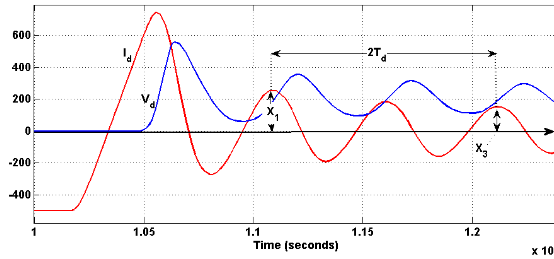


FIGURE 3.13: Logarithmic decrement proceeding

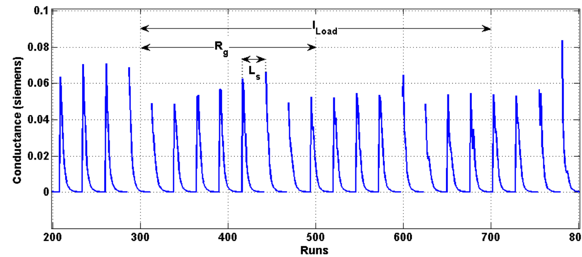
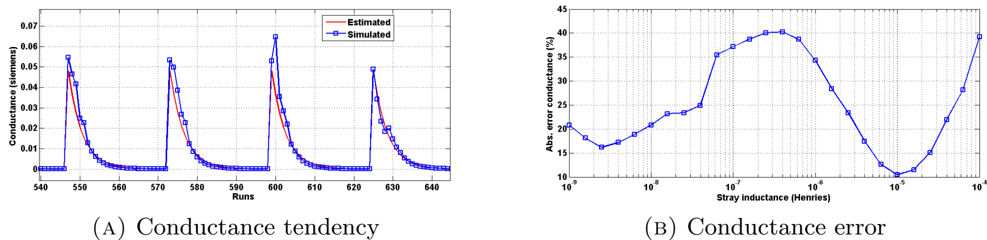


FIGURE 3.14: Conductance for several runs

is better understood by seeing figure 3.14 where several simulation runs have been carried out. Once again, stray inductance represents the narrowest variations (26 runs straight), gate resistance varying every 26 runs and I_{load} every 208 runs. $C[1]$ and $C[2]$ were found to be -15.1691 and -0.5769. Results that fit tendency of traces of figure 3.15 since conductance gets smaller as stray inductance gets larger.

$$\hat{g}_d = e^{C[1]} L_s^{C[2]} \tag{3.17}$$

In figures 3.15a and 3.15b both estimations vs simulations and absolute errors are shown. Also, there is better fitting for some values of inductance, in this case there is an optimum value of stray inductance (1^{-15}) where error at computing conductance is minimum.

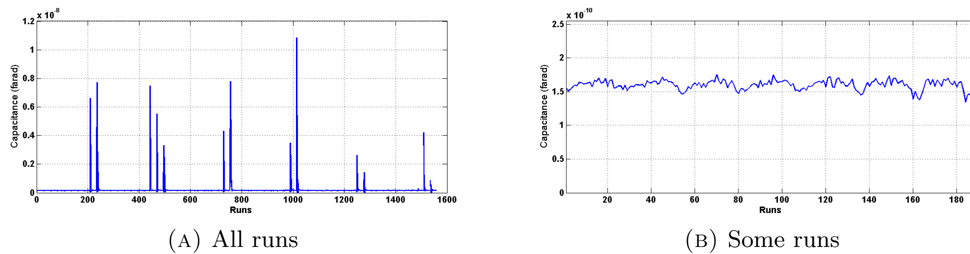


(A) Conductance tendency

(B) Conductance error

FIGURE 3.15: Conductance estimated vs simulated.

Under the same data of simulations to estimate conductance, capacitance is also found by applying logarithmic decrement. In figure 3.16a is plotted capacitance for all runs. While figure 3.16b shows capacitance for about the first 180 runs. From run 180 on gate resistance is greater than 100 Ω. In figure 3.16a this is shown by large values of capacitances (10^{-8} farad) when gate resistance is run for those values over 100 Ω. Figure 3.16b shows an almost constant value of capacitance ($1.5 - 1.6^{-10}$ farad) which could be a good seed in order to optimize calculation of turn on power losses.



(A) All runs

(B) Some runs

FIGURE 3.16: Capacitance for several runs of simulations.

3.2.4 Results of applying of differential equations

In this section some results regarding the shape of waves after solving differential equations presented in previous sections are outlined. Those results are compared graphically with those of simulation data. Some observations are done in order to ease understanding of behaviour of losses that will be presented next section. Behaviour of IGBT and diode waves, current and voltage, are shown for several conditions, especially at different stray inductances and different values of diode capacitor.

In figure 3.17 waves of current and voltage of IGBT are shown for a load current of 30 Ampere, a dc bus voltage of 200, a gate resistance of 10 ohm, a stray inductance of 100 nH and a value of diode capacitor of 800 pF. By also seeing at figure 3.18, it might be noticed that collector emitter voltage behaviour, as expected because of dependency of equation 2.2, does not change despite having changed capacitor to 160 pF. Also, collector current behavior is similar in both cases, especially before reaching peak value. In this way it is not expected that at large values of stray inductance (say greater than 100 nH) and at low values of gate resistance (less than 10 Ω) power losses are not affected by diode capacitance nor by other parameters of differential equation 3.7 since collector emitter voltage has reached 2% of final value before current has reached its peak value.

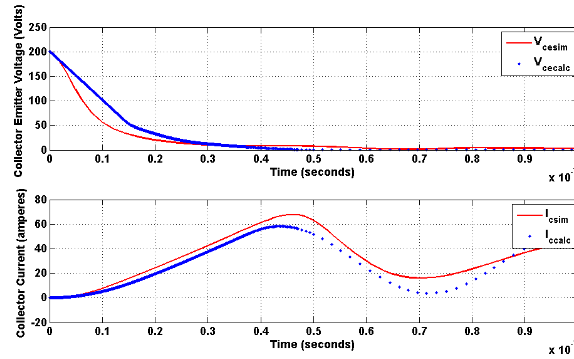


FIGURE 3.17: Comparing simulations and calculation of current and voltage of IGBT at $C_T = 800pF$

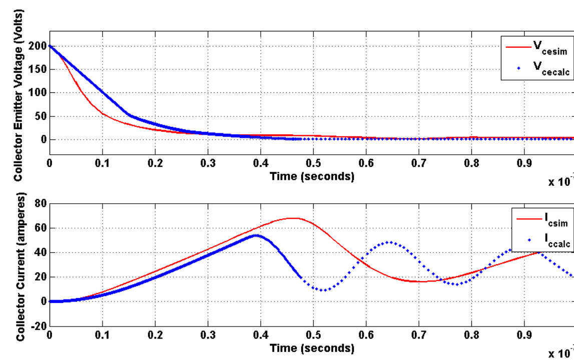


FIGURE 3.18: Comparing simulations and calculation of current and voltage of IGBT at $C_T = 160pF$

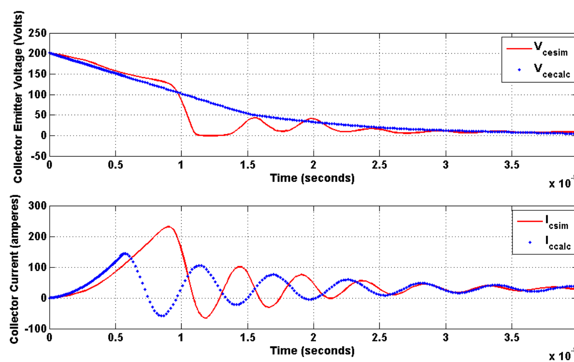


FIGURE 3.19: Comparing simulations and calculation of current and voltage of IGBT, v_{ce} distorted

However, if rate of change of current is increased by decreasing stray inductance, or, rate of change of collector emitter voltage is decreased by increasing gate resistance it is likely that power losses on IGBT are not easily determined by model, for instance, traces of figure 3.19 show how behaviour of collector emitter voltage could be affected by recovery process of diode. This is because diode recovering begins before collector emitter voltage has reached 2% of final value as an outcome of a large $\frac{di}{dt}$.

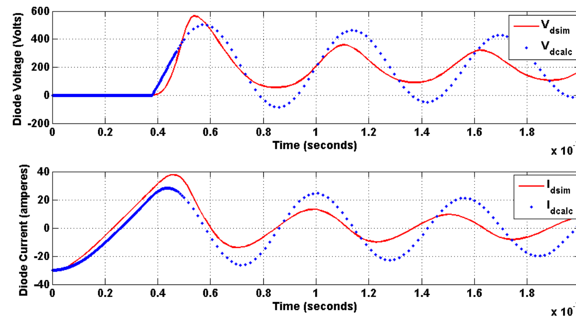


FIGURE 3.20: Comparing simulations and calculation of current and voltage of diode, $C_T = 800pF$

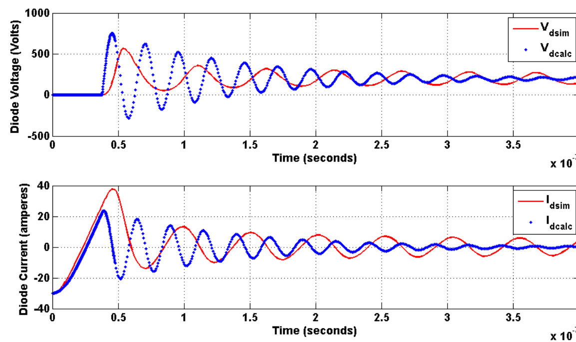


FIGURE 3.21: Comparing simulations and calculation of current and voltage of IGBT, $C_T = 160pF$

In the case of the diode, differences regarding change of diode capacitance are sharper than those in the case of IGBT. As can be seen in figures 3.20 and 3.21, diode total capacitance directly affects calculation of current and voltage during recovery process. As expected, for a small capacitance (160 pF in fig 3.21) frequency of oscillation is large and also damping ratio is large in comparison with those frequencies and damping ratios calculated in figure 3.20. This means that the total diode capacitance must be estimated so that results of calculation match with those results obtained by simulations. This is performed in next section when computing power losses.

3.2.5 Turning on losses of IGBT and reverse recovery losses (comparing)

In this section, turn on losses of diode and IGBT are shown for several conditions of simulation. Both kinds of losses are calculated based on definitions of switching losses at turn on. Also, these results are compared with those obtained by means of the

model described by the differential equations 3.4 and 3.7 by which current and voltage at turning on are found for diode and IGBT.

3.2.5.1 IGBT turn on losses, simulation results

By using definition of equation 2.3 and taking the bounded time ton_{TOT} in figure 3.22, energy losses of IGBT under simulation data are calculated. In this way energy during turn on time is calculated by (3.18).

$$E_{onIGBT} = \int_{ton_{TOT}} i_c v_{ce}, dt \tag{3.18}$$

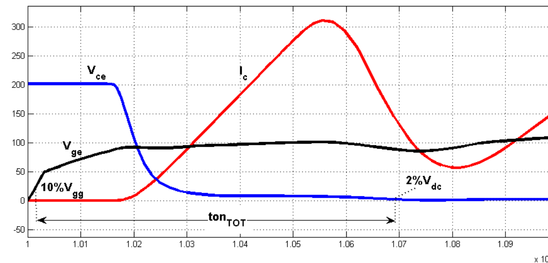
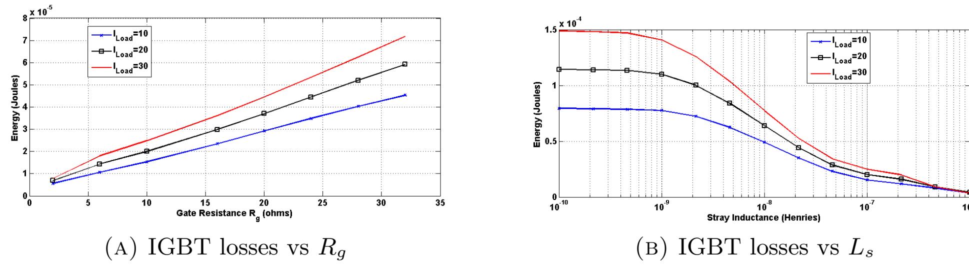


FIGURE 3.22: Turn on transient IGBT, energy calculation

In the circuit shown in figure 3.5, several simulations are run to investigate the effect of magnitude of DC bus voltage, load current, stray inductance and gate resistance on power losses during turn on transient. For instance, in figure 3.23a by varying gate resistance, losses on IGBT could be seen as increasing for any value of load current. Conversely, in figure 3.23b can be seen that at low values of inductance, power losses can be assumed almost constant and get smaller as inductance of circuit is greater. It is remarkable here that rate of change of current is inversely dependent on inductance $\frac{V_{dc}}{L_s}$. While collector emitter voltage takes the same long to reach saturation level, current gets steady state value later as inductance grows in value.

3.2.5.2 Diode reverse recovery losses, simulation results

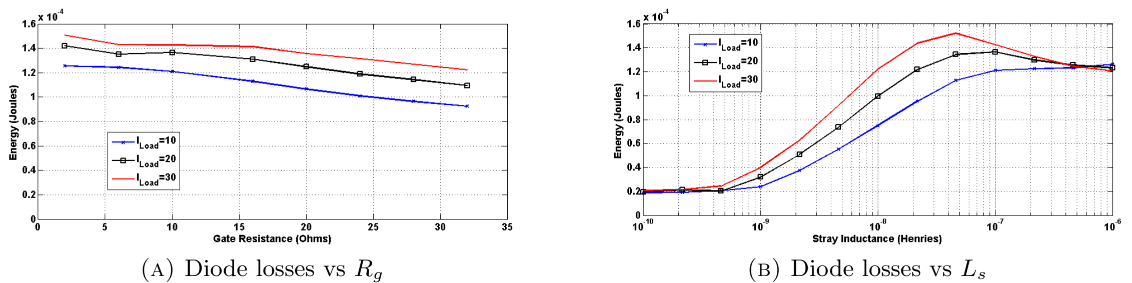
Diode reverse recovery losses are calculated using definition of equation 2.5 and applying it to simulated waves of current and voltage on diode as seen in figure 3.8. Under the same simulations carried out to show losses on IGBT depicted in figure 3.23, diode losses



(A) IGBT losses vs R_g (B) IGBT losses vs L_s

Figure 3.23: Energy losses IGBT comparing.

have also been taken. In figure 3.24a and 3.24b behavior of losses during recovery period t_{rr} are shown.



(A) Diode losses vs R_g (B) Diode losses vs L_s

Figure 3.24: Energy losses Diode comparing.

There are no simple relations as can be seen in IGBT losses since this time process entails several more factors. However, some sights could be drawn in regards of these results. For instance, gate resistance affects directly lasting of collector emitter voltage of IGBT. This in return means that, referring to equation 3.3, rate of change of current is reduced, or, in other words, current through diode might grow slowly as an outcome of increasing gate resistance. The slower the current diode grows the greater the damping ratio ξ, and therefore, the smaller the peak of current during t_{rr}.

3.2.5.3 Comparing simulation and calculation

Now, results of simulation runs will be contrasted against analytical results obtained by the model described by equations 3.4 and 3.7. It is needed to point out here that total diode capacitance has been varied for several calculations. This is because diode capacitances are a very non-linear characteristic of freewheeling diode [31]. Figures 3.25 through 3.28 show behaviour of losses as a function of the different parameters analysed, in all the cases, a value of diode capacitance has been chosen of $C_T = 1.4nF$. This is because error in calculation of losses gets smaller at certain values of capacitance

(see figures 3.30 and 3.31) as expected for diode and IGBT, losses increase with gate resistance in the case of IGBT and decreases in the case of diode. Similar behaviour was observed for stray inductance in regards to those plots of figures 3.23 and 3.24. In the same way, for both devices losses increase by increasing load current and dc bus voltage.

In figure 3.25, losses are plotted against stray inductance, these traces have been taken for a value of gate resistance of 10Ω , a dc bus voltage of 200 volts and a load current of 30 ampere. It is seen there that in the case of IGBT error in determination of losses gets larger as stray inductance gets smaller. Also, though in a lesser extent, referring to figure 3.26, as gate resistance gets smaller, error gets larger. In both cases a reshaping of collector emitter voltage wave takes place, but it is much more determinant in the former case since that wave gets affected by fast transitions of diode current (as stray inductance gets smaller, $\frac{di}{dt}$ gets larger). This, as it was seen in previous subsection, entails a great difference between calculation and simulation of collector emitter voltage behavior (see figure 3.19). These differences are not so sharply in the case of diode, in which a difference could be seen, especially at high gate resistances. This could influence the second phase of turning on because collector emitter voltage could not reach saturation level at the moment when recovery period begins.

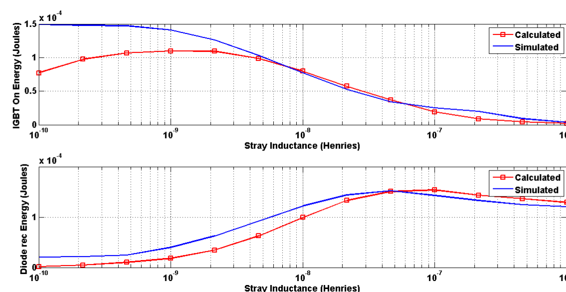


FIGURE 3.25: Energy losses comparing IGBT and diode vs stray inductance

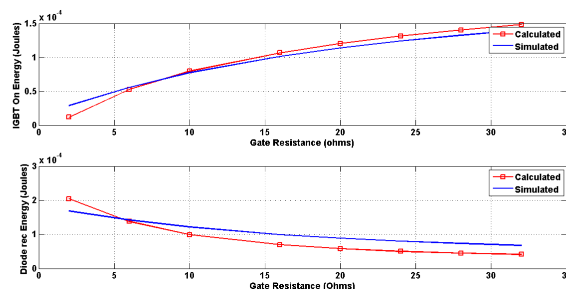


FIGURE 3.26: Energy losses comparing IGBT and diode vs gate resistance

In the case of voltage and current variations, figures 3.27 and 3.28 show how calculations and simulation diverge as these factors change. It is seen in the case of diode that error gets larger as load current increases (fig 3.27 below). And as dc bus voltage level increases, in both cases, calculations yield smaller values of losses in regards to simulation data.

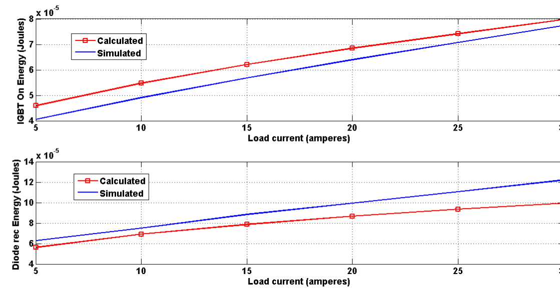


FIGURE 3.27: Energy losses comparing IGBT and diode vs load current

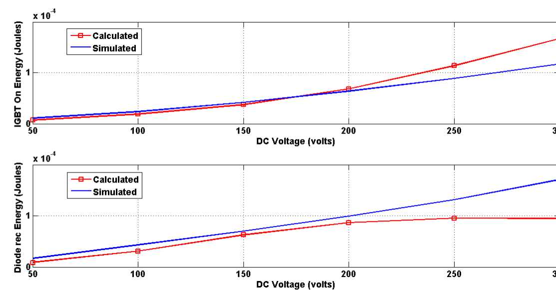


FIGURE 3.28: Energy losses comparing IGBT and diode vs DC bus voltage

Finally, in figures 3.29 through 3.31 a more general perspective could be analysed by comparing model results with simulation data. First, comparing figure 3.23b with figure 3.29, it is endorsed for IGBT on losses that error gets larger for small values of inductances, this is drawn since runs plotted in figure 3.29 show the narrowest changes on stray inductance. From this perspective, figure 3.23b could be a good reference of losses on IGBT as a function of stray inductance no matter what gate resistance level is, and in spite of variations of load current and dc bus voltage (explained by figures 3.27 and 3.28). In the same way, error on losses on diode gets larger as gate resistance gets larger, in the bottom of figure 3.29 gate resistance can be seen as varying less narrow than stray inductance. Finally, figures 3.30 and 3.31 show average absolute error by calculating losses. Average error is calculated by taking all simulating runs and subtracting its respective calculation under the same conditions, but changing only diode capacitance at every calculation. This, as it can be seen, makes the error become smaller for certain

values of capacitance. That influences on a larger extent diode losses than IGBT losses since diode losses calculation is highly dependent on second order model.

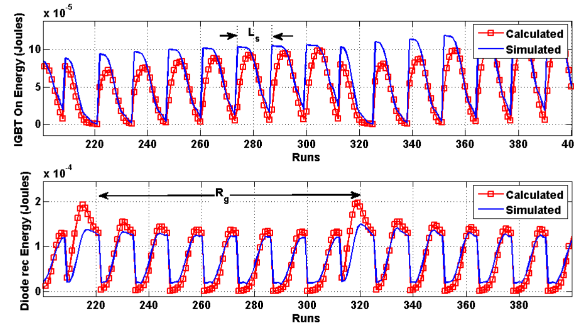


FIGURE 3.29: Energy losses comparing IGBT and diode for all runs

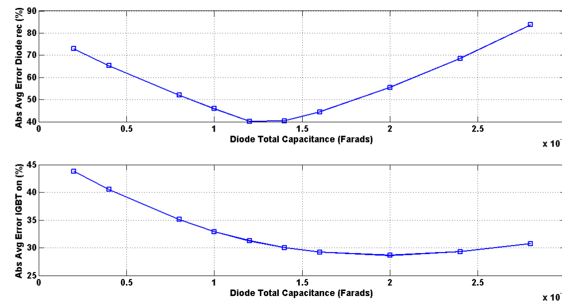


FIGURE 3.30: Absolute average error for all runs varying current

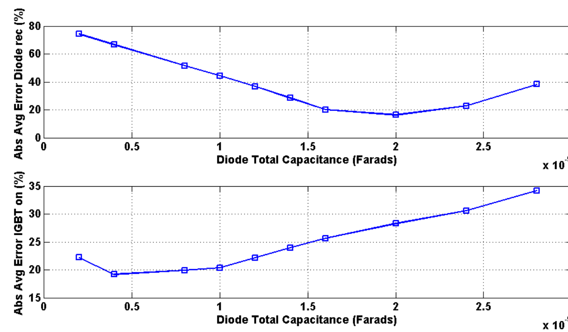


FIGURE 3.31: Absolute average error for all runs varying voltage

3.3 Analysis of turn off periods of commutation

In last section, a linear model was outlined for both current and voltage of an IGBT during turn on period, equations of current and voltage together at the computing of power are in good agreement with simulation results. However, Turn off losses of IGBT are highly non-linear since both current and voltage across it are non-linear. In this section turn off analysis is performed by taking simulation data and making some

polynomial regression to model turn off power losses. Some hypothesis tests are carried out in order to investigate the effect of gate resistance, current and voltage on turn off times and power losses. Power losses are calculated based on definition given in equation 2.4 in chapter 2.

3.3.1 Simulation procedure

Simulation diagram to perform analysis of turn off period is depicted in figure 3.32. The analysis that will be carried out on circuit diagram is intended to obtain data and make polynomial regression. For this task, 80000 simulation runs will be performed in which load current I_{load} will be varied from 2 to 20 ampere with steps of 2 ampere, gate resistance R_g from 1 to 200 Ω with steps of 1 Ω, DC bus voltage V_{dc} from 20 to 400 volts with steps of 20 volts.

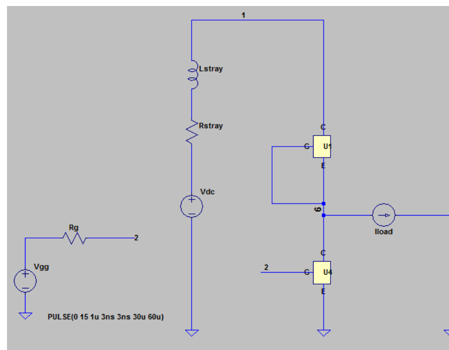
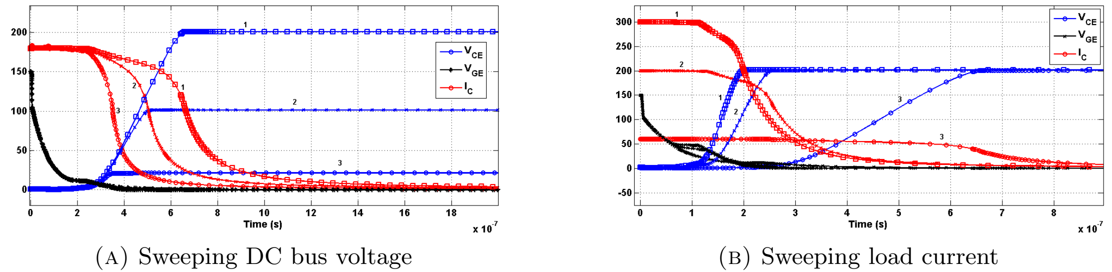


FIGURE 3.32: Diagram of simulation on LTspice for turning off process

3.3.2 Simulation results at turn off

In this subsection, several plots and analysis are performed in order to describe behaviour of IGBT during turn off process. As it can be seen in figure 3.33b, for a constant value of load current (6 ampere, in a scale of 30units/ampere), gate resistance (5 Ω), and V_{gg} (15 Volt), collector-emitter voltage takes longer (in regards to the time when V_{ge} begins to drop) to reach blocking level. Also, in figure 3.33b it can be seen that for levels 20, 100 and 200 volts, it takes 350, 500 and 650 nanoseconds respectively to reach blocking level. Likewise, in the case of current, in figure 3.33a several traces are shown where different load current values have been simulated: 6, 20 and 30 amperes. There, DC bus voltage has been kept constant at 200 volts and also gate resistance R_g and gate

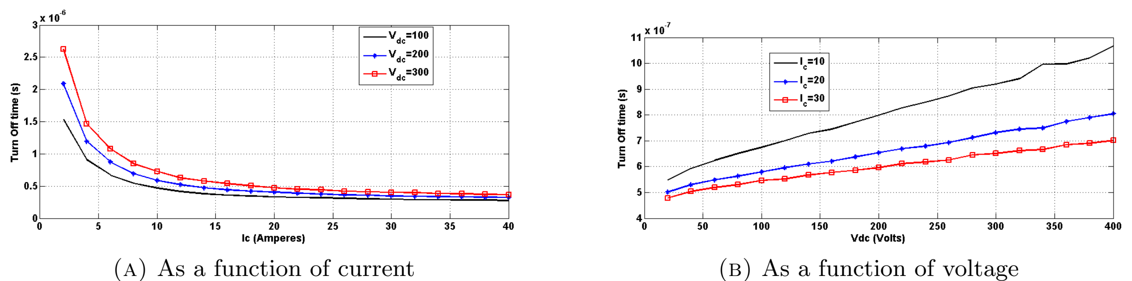
polarization V_{gg} are 5 Ω and 15 volts respectively. Once again, the time it takes the voltage to reach blocking level gets longer. Also, current tail period is shifted right at the beginning of time too.



(A) Sweeping DC bus voltage (B) Sweeping load current

Figure 3.33: Waves simulated during turn off period.

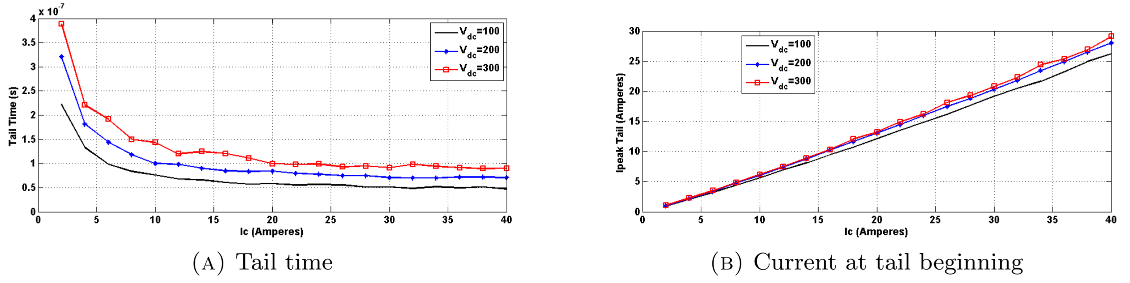
If total turn off time is measured from the time V_{gg} is withdrawn until the time the current reaches 1% of its steady state value. Then, turn off times at different rates of current, voltage and gate resistance could be built to show the influence of these factors on power losses. In figure 3.34a an inverse relationship is seen between current and total turn off time. Both plots show that for large currents, the total time it takes the IGBT to turn off is inversely proportional to the magnitude of current of the load. Also, as it was expected, turn off time has a direct relationship on dc bus voltage magnitude as can be seen in figure 3.34b.



(A) As a function of current (B) As a function of voltage

Figure 3.34: Turn off time behaviour.

From plots of figure 3.33, a strong dependency upon current and voltage is seen for turn off times. Especially for that period of time it takes voltage reach the DC bus level. But also, there is a dependency of tail period upon these variables that must be taken into account. As can be seen in figure 3.35, tail period is shorter as current increases, but also, is greater for different levels of voltage. In the same way, the value of current at the beginning of tail period is also dependent on voltage and current, but being shorter than load current Ic as DC bus voltage gets shorter (see figure 3.35b).



(A) Tail time (B) Current at tail beginning

FIGURE 3.35: Tail period behaviour and current.

3.3.3 Statistical observation on turning off variables and factors

Given the plots shown in figures 3.33 through 3.35a, a statistical analysis is needed in order to know the real effect of every factor on the variables: tail time, current peak value at beginning of tail period, rise time and total turn off time. This analysis could be performed by building an analysis of variance (ANOVA) of every factor upon each variable. The ANOVA is built by stating an hypothesis which determines whether or not a factor is influencing the change of the variable. Null hypothesis states that the factor has no effect on the variable, and, conversely, alternative hypothesis states that the factor has effect on the variable. The $p-value$ represents the likelihood of acting wrong at accepting null hypothesis and the criterion used to accept or reject null hypothesis is given by the significance level. Table 3.1 shows the $p-values$ for every hypothesis test on every variable and the influence of the factors. Equation 3.19 describes every hypothesis test carried out to investigate the effect of every factor. Every factor α_i represents the factors listed on the table: R_g, I_{load}, V_{dc} and their interactions. If we choose a significance level of 1%, then $p-value$ must be less than 0.01 in order to reject null hypothesis given that level of confidence. In table 3.1 this means that for instance, gate resistance R_g does not have any effect upon lasting of tail period (tail time) because there is a likelihood of almost 9% to make a mistake by rejecting null hypothesis, then null hypothesis is accepted.

$$H_o : \alpha_i = 0; for\, any\, i \qquad H_1 : \alpha_i \neq 0; for\, some\, i \tag{3.19}$$

Given the results obtained in table 3.1 several conclusions could be drawn: both current and voltage have effects on every variable. This is in concordance with the plots of figures 3.33 through 3.35a. Also, it could be seen that gate resistance does not have any

Table 3.1: $p - value$ of effect of factors on variables τ, I_{pktail}, t_{bloc} and t_{tot}

Factor/Variable	τ	I_{pktail}	t_{bloc}	t_{tot}
R_g	0.0809	$2.0e-16$	$2.0e-16$	$2.0e-16$
I_{load}	$2.0e-16$	$2.0e-16$	$2.0e-16$	$2.0e-16$
V_{dc}	$2.0e-16$	$2.0e-16$	$2.0e-16$	$2.0e-16$
$R_g : I_{load}$	0.0317	$2.0e-16$	$2.0e-16$	$2.0e-16$
$R_g : V_{dc}$	0.0431	$2.0e-16$	$2.0e-16$	$2.0e-16$
$I_{load} : V_{dc}$	$2.0e-16$	$6.44e-16$	$2.0e-16$	$2.0e-16$

effect on tail period duration, a result that confirms that the process of slow current vanishing during this period is a internal process that could not be modified by external parameters. Also, it could be seen that there are interaction effects of current and voltage on tail time. This means that this tail time could not be modelled separately by current and voltage and then added together applying superposition principle. The other results show that gate resistance has effect even at the value of current at the beginning of tail peiod (I_{pktail}) which is a border condition dependent of the previous period of turn off process.

A similar analysis of variance could be performed to investigate the effect on turn off power losses of every factor listed on table 3.1. As can be seen in table 3.2 every factor has an influence on power losses on freewheeling diode and on both losses of IGBT before and after tail period beginning. In the case of gate resistance, it is important to notice that it has a direct effect on the magnitude of tail current when tail period starts and that is why gate resistance must also be taken into account on calculation of energy dissipation during tail period.

Table 3.2: $p - value$ of effect of factors on Turn off losses E_{OFFpre}, $E_{OFFtail}$ and $E_{ONdiode}$

Factor/Variable	E_{OFFpre}	$E_{OFFtail}$	$E_{ONdiode}$
R_g	$2.0e-16$	$2.0e-16$	$2.0e-16$
I_{load}	$2.0e-16$	$2.0e-16$	$2.0e-16$
V_{dc}	$2.0e-16$	$2.0e-16$	$2.0e-16$
$R_g : I_{load}$	$2.0e-16$	$2.0e-16$	$2.0e-16$
$R_g : V_{dc}$	$2.0e-16$	$2.0e-16$	$2.0e-16$
$I_{load} : V_{dc}$	$2.0e-16$	$2.0e-16$	$2.0e-16$

3.3.4 Characterization of power losses during turn off

Since every factor analysed in previous section has direct effect on power losses, even their interactions, a regression model that takes into account at least one interaction is needed. Several traces of characteristics are delivered along with the datasheets of IGBTs. These characteristics are dependent upon gate resistance, gate voltage, collector voltage, load current and temperature. For instance, the total switching losses of an IGBT could be a few millijoules given a value of load current (for instance 30 ampere), a value of temperature (often 25 , a value of dc bus voltage and a value of series gate resistance. In this way, a model for turn off losses could be built by taking several values of gate resistance, one at a time, and then build a model which includes variations of current and voltage. A method used to carry out this task is to propose a polynomial of degree n like the one drawn on equation 3.20.

$$E_{off}^{R_g=i} = K_m I_{load}^n + K_p V_{dc}^n + ... + K_6 I_{load}^2 + K_5 V_{dc}^2 + K_4 I_{load} + K_3 V_{dc} + K_2 V_{dc} I_{load} + K_1 \tag{3.20}$$

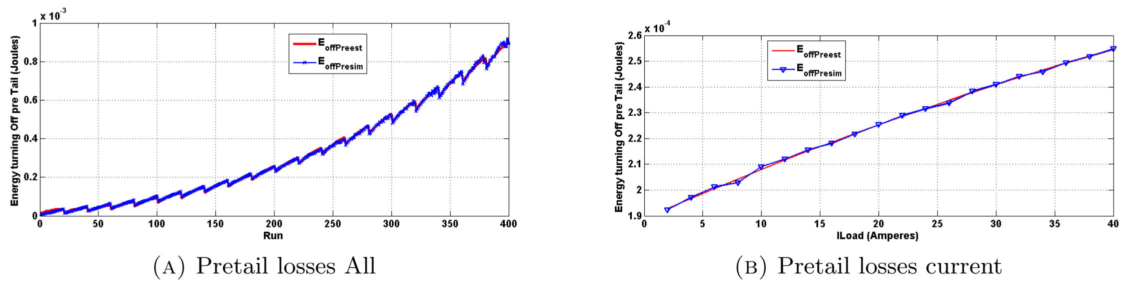
Where $E_{off}^{R_g=i}$ is the energy consumption at turn off on either IGBT or diode, i takes several values for gate resistance. K_m are the coefficients of the polynomial and V_{dc} and I_L are dc bus voltage and load current respectively. To get the coefficients of the polynomial equation 3.20, data for $E_{off}^{R_g=i}$ is needed to be collected from several simulations. Obtainment of these data yields the system of equations given by 3.21.

$$E_{off} = AK \tag{3.21}$$

The solution K minimizes the distance of the simulated data to the estimation of them by the polynomial.

Now, we will take several degrees for polynomial to solve the system and then estimate the losses of both IGBT and diode. For example, in figure 3.36 a plot of energy loss in IGBT during pretail period is shown making gate resistance equal to 10 Ω. In figure 3.36a estimated losses and simulated data of losses are compared for 400 runs. Voltage is taking different values every 20 runs. That means that for the first 20 runs V_{dc} is 20

volts, then from run 20 to 40 is 40 volts and so on. In figure 3.36b the same traces are shown for $V_{dc} = 200$ volts, that is, from run 200 to the 220.



(A) Pretail losses All

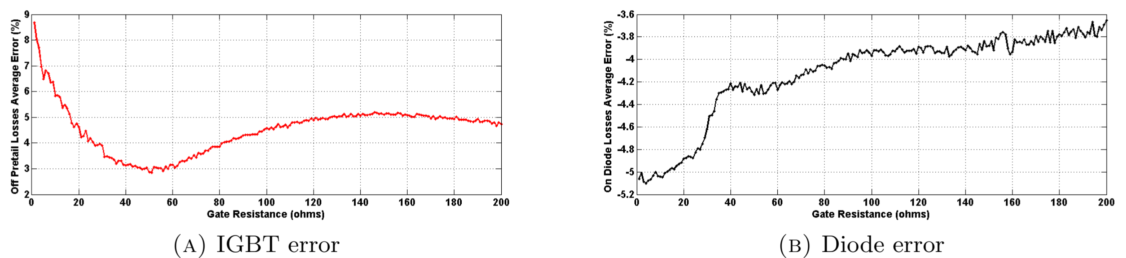
(B) Pretail losses current

FIGURE 3.36: Comparing simulated and estimated Turn off losses.

By taking the difference in every run between estimations and simulated data, we can hold the equation 3.22.

$$Error_{OFF} = 100\% | \sum \frac{E_{OFFsim} - \hat{E_{OFF}}}{E_{OFFsim}} | \tag{3.22}$$

Then, by taking the average of all runs average error is found at a given gate resistance. These traces are shown in figures 3.37a and 3.37b for losses in IGBT and diode.



(A) IGBT error

(B) Diode error

FIGURE 3.37: Turn off losses error at each value of gate resistance.

Once again, we take the average of traces of figure 3.37 to get the average error of all runs and all gate resistance conditions. In table 3.3 these results are summarized for every loss and every degree of polynomial choosing.

TABLE 3.3: Turn off losses polynomial regression absolute error at different degrees

Degree of polynomial	$E_{OFFpre}(\%)$	$E_{OFFtail}(\%)$	$E_{ONdiode}(\%)$
1	26.57%	52.82%	−34.66%
2	4.53%	20.18%	−4.12%
3	4.64%	20.41%	−3.17%
4	4.73%	20.36%	−2.55%

3.4 Conclusions

By simulation data, it has been found that at turn on, and regardless of load current value there is a direct relationship between IGBT turn on energy consumption and gate resistance. Also, it is seen that turn on energy consumption is almost constant for values of stray inductance less than 1 nH and drop for larger values. In the case of diode reverse recovery losses, relationship with gate resistance is weaker, however, constant values of energy consumption are also seen for values of stray inductance of 1 nH.

It has been shown how to model behaviour of current and voltage in IGBT during turn on by taking IGBT capacitances and circuit relationship. Non-linearity effect of gate-drain capacitance C_{gd} has been taken into account in the expressions for current and voltage in IGBT during first phase of turn on period. Also, stray inductances have been included in the model and their effects have a direct relationship to the rate of change of current. From simulation data, it has been found that storage time is a dependent parameter that could be modelled directly from stray inductance only.

Conductance and capacitance have been found in a similar way as storage time, but a logarithmic decrement time-domain technique of parameter extraction has been employed to find them from simulation data too. Non-linearity of diode capacitances during reverse recovery process has been found as an important factor that affect accuracy of model. In this way, value of diode capacitance found by parameter extraction has been used as a seed for fitting current and voltage traces.

It has been shown that second order polynomial regression procedure for finding turn off power losses is a good approximation, however it is needed that current, voltage, gate resistance and interaction between current and voltage were taken into account. Also, in spite of the independence of tail time upon gate resistance, it is seen that current magnitude at the beginning of tail period is dependent on gate resistance.

Finally, unlike turn on period, during which IGBT capacitances could model behaviour of collector emitter voltage and diode reverse recovery process, it has been shown that turn off period of IGBT is highly dependent on current and voltage magnitude, not being possible to apply approximations like those performed for turn on period.

Chapter 4

Indirect current measurement

In this chapter a procedure to carry out an indirect measure of transient current through a power semiconductor is outlined. The procedure is verified on a clamped inductive load circuit. The procedure performed aims to investigate factors affecting measuring of current. The method used is based on direct measuring of voltage waveform across a wire put in series with an IGBT. Then current is obtained by processing voltage measure data. The method used takes into account both self-inductance and resistance of a wire, also capacitance of probe employed to measure voltage across wire. The method is verified via LTspice and methods to obtain signals from LTspice and process them digitally are also explained. Finally, an experiment to determine those factor influencing signal to noise ratio of measuring is carried out. This experiment is based on Taguchi's methodology and dc bus voltage, length of wire used, bandwidth and prewarping are taken as factors.

4.1 Measurement circuit analysis

In this section an analysis is performed in order to indirectly obtain current through a power semiconductor . Analysis takes into account resistance and self-inductance of a wire put in series with semiconductor. In figure 4.1 a measurement system in series with an IGBT is depicted. In circuit, L_w represents wire self-inductance, R_w is wire resistance, and voltmeter in parallel V represents oscilloscope and probe system used to

obtain voltage across wire. The main objective is to obtain current i_{switch} by means of wire and measurement system parameters.

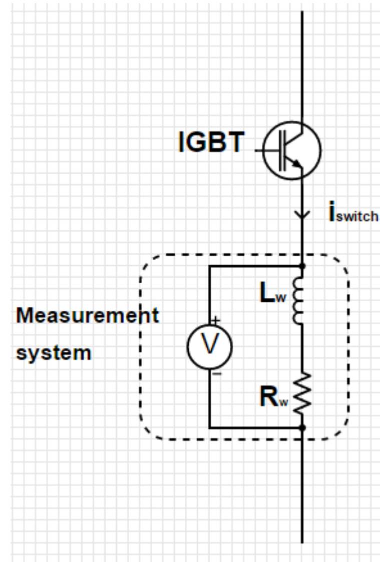


FIGURE 4.1: Measuring Circuit elements

4.1.1 Circuit Model

Measurement system pointed out in circuit of figure 4.1 can be represented by the system shown in figure 4.2. In this diagram, both resistance and self-inductance of wire are now connected in parallel with a capacitance C_p and a voltage source v_p. C_p is the capacitance of the probe used to take voltage across wire to acquire it in an oscilloscope. v_p is the voltage signal measured by the system probe-oscilloscope. Resistance R_s is a resistance taken in order to create a mesh between wire and oscilloscope. In this analysis, input resistance of probe-oscilloscope is not taken because v_p is analysed at high frequencies and fast transitions of signal i_{vdc}, which represents current through semiconductor. Finally, i_c and i_w represent currents through probe capacitor and wire respectively.

Given the system depicted in figure 4.2, voltage and current Kirchhoff's laws could be applied. By knowing that current through probe capacitor is $i_c = C_p \frac{dv_c}{dt}$, equations 4.1 and 4.2 represent behaviour of circuit.

$$v_c = i_w R_w + L_w \frac{di_w}{dt} \tag{4.1}$$

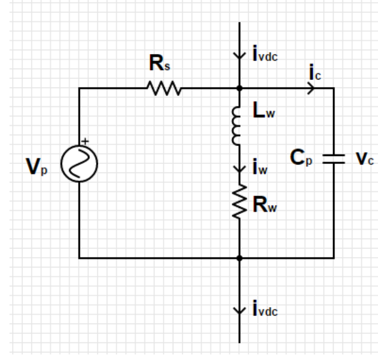


FIGURE 4.2: Measuring equivalent circuit

$$\frac{v_p - v_c}{R_s} = i_w + C_p \frac{dv_c}{dt} \tag{4.2}$$

Latter set of equations could be rearranged to represent system in a state space form. Voltage across capacitance v_c and current through wire i_w are state variables, while voltage taken by the probe v_p is represented as the system input. In this way, equations 4.3 and 4.4 model the system.

$$\begin{bmatrix} \dot{x} \end{bmatrix} = \begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_w}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_p R_s} & -\frac{1}{C_p} \\ \frac{1}{L_w} & -\frac{R_w}{L_w} \end{bmatrix} \begin{bmatrix} v_c \\ i_w \end{bmatrix} + \begin{bmatrix} \frac{1}{R_s C_p} \\ 0 \end{bmatrix} u = Ax + Bu \tag{4.3}$$

$$y = x_2 = i_w = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_c \\ i_w \end{bmatrix} + 0u = Cx + Du \tag{4.4}$$

Where A is the state-transition matrix, B is the input matrix, C is the output matrix and D is the feedforward matrix, which is zero because input u does not affect directly output i_w.

4.1.2 Discretized matrices

System outlined by equations (4.3) and (4.4) needs to be discretized because input represents digital data obtained by a digital oscilloscope. In this way, system discretized is represented by equations 4.5 and 4.6.

$$x[k+1] = A_d x[k] + B_d u[k] \tag{4.5}$$

$$y[k] = C_d x[k] + D_d u[k] \tag{4.6}$$

Where matrices A_d, B_d, C_d and D_d can be obtained according to the method used to discretize the system. Discretization might be performed by numerical integration, zero-pole matching or hold equivalents. Among numerical integration, polygons are used to carry out integration. Discretization is performed by taking horizontal difference between corners of polygon and leading horizontal distance between them (sample time) to zero. Another methods of discretization are: zero-pole matching and hold equivalents [60]. Table 4.1 shows equivalent discretized matrices by using numerical integration.

TABLE 4.1: Discretized matrices by numerical integration (taken from [60])

Matrix	Forward	Backward	Tustin (Bilinear)
A_d	$I + AT_s$	$(I - AT_s)^{-1}BT_s$	$(I + \frac{AT_s}{2})(I - \frac{AT_s}{2})^{-1}$
B_d	BT_s	$(I - \frac{AT_s}{2})^{-1}$	$(I - \frac{AT_s}{2})^{-1}B\sqrt{T_s}$
C_d		$C(I - \frac{AT_s}{2})^{-1}$	$\sqrt{T_s}C(I - \frac{AT_s}{2})^{-1}$
D_d	D	$D + C(I - \frac{AT_s}{2})^{-1}BT_s$	$D + C(I - \frac{AT_s}{2})^{-1}\frac{BT_s}{2}$

In table 4.1 T_s is sample time of discret data. Sample time will be determined by the record length and time interval at experimental measured signals, while in the case of simulation routines it is necessary to interpolate data obtained by SPICE since sample time of its signals is variable.

Discretization method that will be used here is numerical integration by trapezoidal rule (or Tustin's method). This method will be applied on system by using prewarping and no prewarping, that is, by establishing the cutoff frequency of measurement system in order to avoid distortion. Also, some results will be shown by performing another discretization method, for instance, zero order holding.

4.2 Circuit of application: diode clamped inductive load

In this section a diode clamped inductive load circuit is presented as the case of application of procedure carried out last section. This circuit will be used in order to show behaviour of current through semiconductor IGBT and the feasibility of measuring current through it. The circuit will be employed to perform both experimental and

simulation verification intended to measure current indirectly. In figure 4.3 circuit is shown along with measurement system.

As it can be seen in figure 4.3, circuit is composed of an IGBT $Q1$ commutating by the action of a gate signal v_{gg} through a gate resistance R_g. Diode $D1$ function is to conduct load current when IGBT is in offstate. V_{dc} represents dc bus voltage, R_{load} and L_{load} are selected such as there is diode reverse recovery during turn on of $Q1$ and then, current through IGBT keeps its speed since no time is required to charge load inductance during transient periods. Finally, R_w and L_w are the parameters of wire used to perform measuring of current and symbol V represents the system of measurement, which in this case is the probe and the oscilloscope used to perform the measurement and outlined in last section.

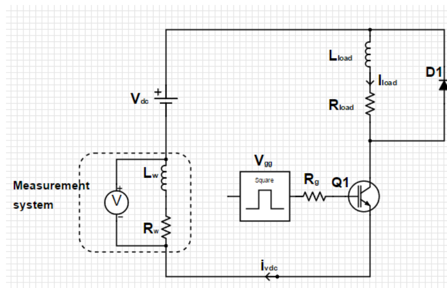


FIGURE 4.3: Diode clamped inductive load circuit of application

4.3 Simulation Verification

In this section, main simulation results and procedure carried out to verify measurement procedure are described. Circuit diagram employed to verify procedure is shown in figure 4.4. Software used to perform simulations is LTspice IV. As it can be seen in figure 4.4, load parameters R_{load} and L_{load} hold values of 6 Ω and 6 mH respectively, while R_g is 10 Ω. Subcircuits $U1$ and $U2$ represent IGBTs whose model is an IGBT irg4pc50fd. In this case $U2$ takes the function of commutating IGBT and $U1$ only represents freewheeling diode by shortcircuiting its gate and emitter terminals. Measurement system is represented by capacitance C and by wire inductance and resistance R_w and L_w. Pulse train V_{gg} is a modulated wave whose carrier signal is square wave of 80 μs of period and 80 % of duty cycle, while its reference signal is a square wave whose period is 1600 μs and duty cycle of 50 %.

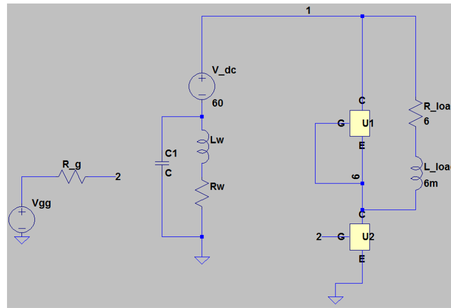


FIGURE 4.4: Clamped inductive load circuit simulation diagram

Simulations will be run such as to investigate the effect of dc bus voltage V_{dc}, probe capacitance C, wire inductance L_w and wire resistance R_w in acquiring current through dc bus voltage (which is the same as current through IGBT) by means of voltage across wire. Namely simulations will be done by setting inductance of wire from 10 nH to 1 μH, resistance of wire from 0.01 Ω to 1 Ω and probe capacitance between 3 pF to 1nF which are values typical of input capacitance of an oscilloscope's voltage probe.

4.3.1 Performance of clamped inductive load circuit

Circuit of figure 4.4 must behave in such a way that current through load does not drop to zero during switching of $U2$. This circumstance is reached by setting a load self-inductance and a load resistance large enough to sustain current during time intervals when IGBT is in off-state. Load constant $\frac{L_{load}}{R_{load}}$ is $1e-3seconds$, which is greater compared to semi-period of modulated wave $800e-6 = 0.8e-3seconds$, in this way, current through load behaves approximately linearly as shown in the top red dotted trace of figure 4.5 and does not reach zero, even after semi-period off-state has elapsed. In the same figure, current through IGBT is plotted where it can be seen that there is a normal switching and IGBT is turning on and off.

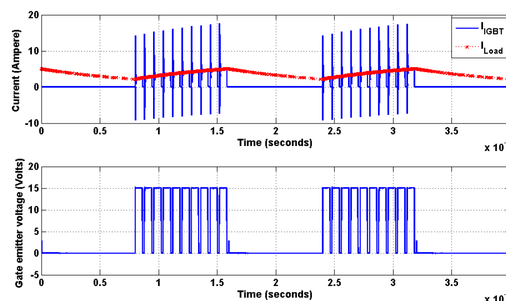


FIGURE 4.5: Current through IGBT and load (above). Gate emitter voltage (below)

In the same way, figure 4.6 shows gate voltage and currents during transient period, that is, a zoom picture of figure 4.5 on first pulse after off-state semi-period. As it can be seen, current through IGBT (blue continued trace top) is oscillating by the action of diode reverse recovery process with a period of the order of tens of nanoseconds, while current through load (red dotted) appears as constant with a zero-different value. This behaviour lets to analyse switching of IGBT accordingly to expected performance.

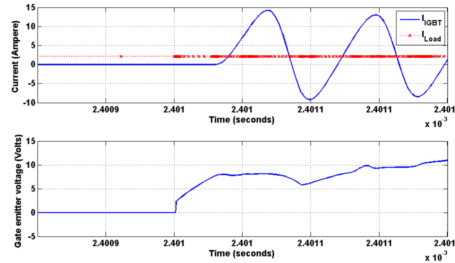


FIGURE 4.6: Transient behaviour of current through IGBT and load (above) and of Gate emitter voltage (below)

4.3.2 Measurement procedure verification

Simulated waves must be obtained from LTspice and then process them by a software analysis tool which carry out discretization and solving system given by equations (4.5) and (4.6). This is performed by using MATLAB which is endowed with fitted tools to perform acquiring and processing of digital data. Simulation analysis is intended to evaluate precision of method described, this could vary according to the method of discretization, initial values of states, among others. In this way, simulation results taking into account these issues will be shown.

4.3.2.1 Simulated data acquirement procedure

In order to perform analysis of simulation data, the procedure depicted in figure 4.7 must be followed. As it can be seen there, only measured voltage across wire is needed as input signal from simulation data. Input arguments are parameters of wire and probe capacitance. While outputs signals are state variables, current through wire and voltage across probe capacitor, and current through dc bus, which is easily deduced by taking current through capacitor probe and current through wire.

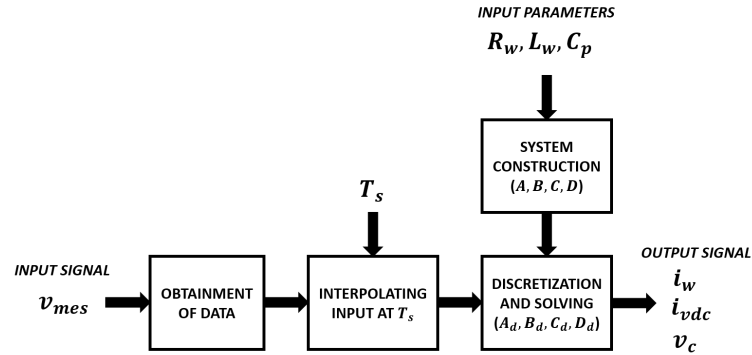


FIGURE 4.7: Block diagram simulation procedure

Stage of interpolation is needed since simulated data retrieved from LTspice are variable sampled because it uses Newton-Rhapson's method to solve voltages and nodes of electric circuits. In this way, data with sharp changes and high derivatives will require much more points than signals with derivatives close to zero, or, in other words, signals that are constant during long periods and later change abruptly (see figures 4.6 and 4.5) will be uneven sampled. For example, by observing at figures 4.6 and 4.5, it might be noticed that before setting a pulse on gate emitter terminals of IGBT, samples are more separated than they are after gate emitter voltage has begun rising (see red dotted trace). This bound us to process digital signals in such a way to transform simulation data into constantly sampled signals because by discretizing it is assumed that signals are separated by equal times. This digital processing is carried out by cubic interpolation of signals of LTspice and sample time T_s is set as a input parameter for this process.

Discretization is performed by using bilinear transformation (Tustin's method) of table 4.1. Transient periods are taken one at a time. First, during turn on period of commutation of IGBT, voltage across wire is obtained, and then current is found by applying equations 4.5 and (4.6).

4.3.2.2 Simulation results

At this point, main simulation results will be shown. Given some differences between performance of method at turn on and turn off transient, traces will be depicted where Tustin's method is employed with prewarping and no prewarping.

- Turn on

Turn on transients are shown in figure 4.8, where original signal taken from LTspice is the red continuous signal and calculated and discretized signal is the dotted blue trace. As it can be seen, some error is introduced by prewarping discretization, however in both cases, high frequencies are reliably reproduced. Sample time is $0.2ns$, wire inductance and resistance $L_w = 10nH$, $R_w = 0.01\Omega$ and probe capacitance $C_p = 3pF$.

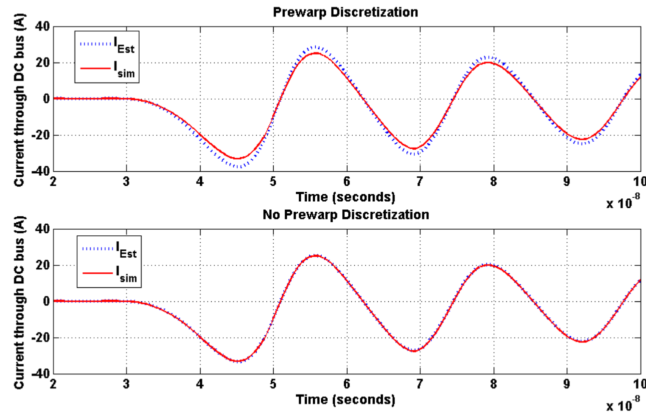


FIGURE 4.8: Current through DC bus with prewarping discretization (top) and no prewarping (bottom) at turn on transient, $Ts = 0.2ns$, $L_w = 10nH$, $R_w = 0.01\Omega$ and $C_p = 3pF$

- Turn off

  Also, turn off transient must be obtained by the same methodology. In this case, discretization must start from a zero-different initial condition for current and voltage on the wire. In figure 4.9 traces showing calculated (red continuous) and simulated (blue dotted) currents are depicted for prewarping and no prewarping discretization. Once again, no prewarping yields better results. However, it is important to take into account variations in sample period T_s (large enough to avoid aliasing effects), in parameters of circuit (R_w, L_w and C_p) as well as discretization method and speed of transitions (varying gate resistance R_g). Finally, in figure 4.10 it is seen, for the same conditions, that zero order hold method does not fit so well as Tustin's discretization under the same conditions.

- Error analysis

  Measurement of current is not accomplished without any mistake. Also, it is important to keep measurement system without effect on the circuit. In this sense, capacitance of the probe must be in the order of picofarads, wire inductance in the

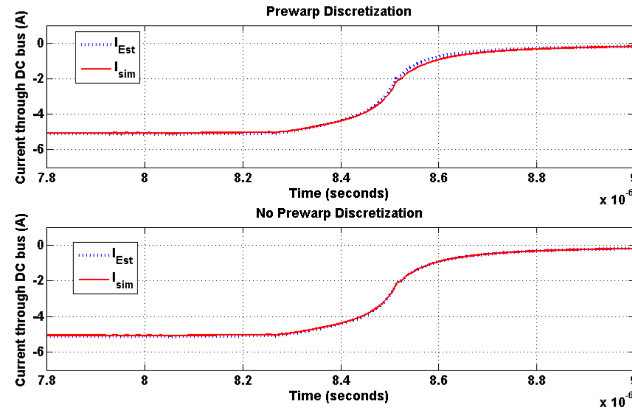


FIGURE 4.9: Current through DC bus with prewarping discretization (above) and no prewarping (below) at turn off transient, sample time $Ts = 0.2ns$, $L_w = 10nH$, $R_w = 0.1\Omega$ and $C_p = 3pF$

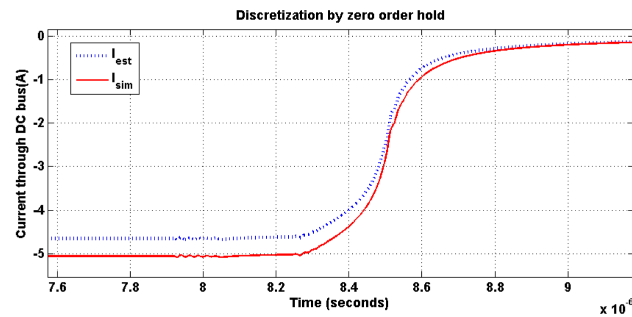


FIGURE 4.10: Current through DC bus with zero order hold discretization at turn off transient, sample time $Ts = 0.2ns$, $L_w = 10nH$, $R_w = 0.1\Omega$ and $C_p = 3pF$

order of few tens of nanohenries and also, wire resistance must be small enough. However, it is important to state the scope of the method here outlined by some plots. In figure 4.11 variation of average absolute error, given by equation 4.7, of estimation as a function of wire inductance is shown for several values of wire resistance and probe capacitance. It must be noticed that as wire inductance gets larger average error gets larger, especially at low values of wire resistance. It is seen also, that probe capacitance does not affect measuring at low values of both wire resistance and wire inductance, however, it is not worthy a value of 100 nF for a voltage probe.

$$AbsError = 100\%|\sum \frac{\hat{I_{mes}} - I_{mes}}{I_{mes}}| \tag{4.7}$$

By observing at figure 4.12 it can be seen that a choice of a sample period of 2 nanoseconds is good enough to take measurement of current, no matter what value of wire inductance is. This in regards to the other traces for smaller sample

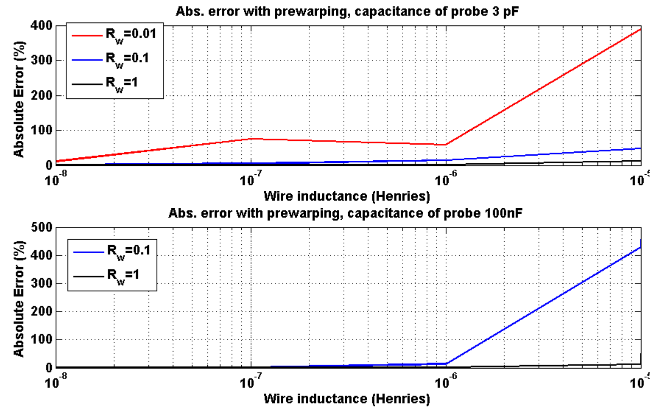


FIGURE 4.11: Average absolute error at calculating current as a function of wire inductance for several wire resitance values. $Ts = 0.2ns$, $C_p = 3pF$ (above), $C_p = 100nF$ (below).

periods (0.2 nanoseconds and 20 picoseconds). Also, it is seen that either applying discretization by prewarping or not prewarping means little in regards to the average absolute error at calculation of current.

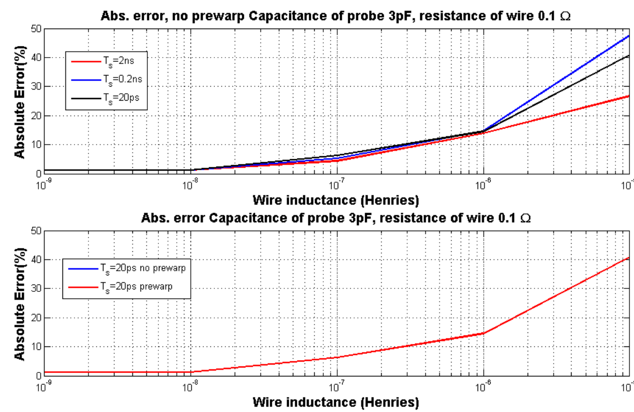


FIGURE 4.12: Average absolute error at calculating current as a function of wire inductance for various sample periods. $C_p = 3pF$, $R_w = 0.1\Omega$ (below).

4.4 Experimental verification

In this section main results of experimental verification of measurement method are presented. First, experimental diagram is presented, where needed equipment and elements used are specified. Then, experiment procedure is explained by using Taguchi's methodology. In this way, L-array used and variance table construction are presented. Finally, experimental results are shown.

4.4.1 Hardware description of experiment

Diagram of experiment performed is shown in figure 4.13. As in the case of simulation, down IGBT switches by the action of a signal applied on the gate, while up IGBT is used as freewheeling diode.

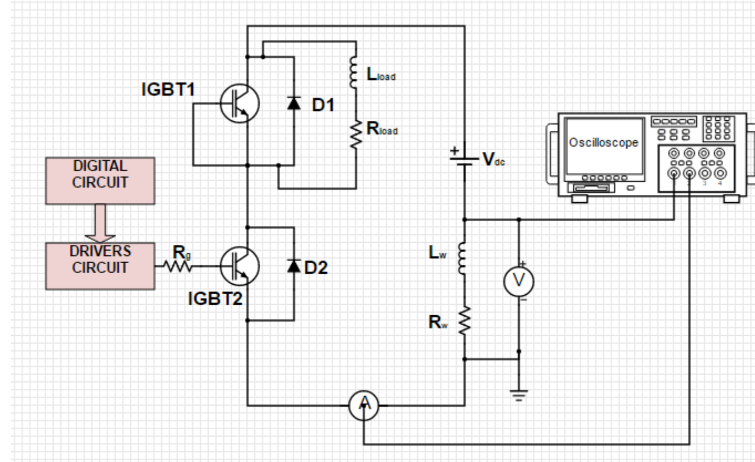


FIGURE 4.13: Experimental diagram

Digital circuit is a microcontroller Dspic30f4012 of microchip whose digital outputs are of 5 volts level. Drivers circuit is built by a Texas Instrument ISO5500 whose digital inputs are of 5 volts and output of 15 volts. IGBT is a irg4pc50ud of International Rectifier. Loads used are a power resistance of 6Ω and a power inductor of $6mH$. Wire used to perform measurement across it is a 80/20 nichrome wire which resistivity is $\rho = 1.39\mu\Omega m$, diameter $d = 1mm$ and melting point about $1700K$ [61] that makes it capable of carrying currents over 20 amperes, 3 wires of $10cm$, $15cm$ and $20cm$ will be used and, therefore, both self-inductance and resistance must be estimated for each. In table 4.2 these elements are described.

TABLE 4.2: Equipment and elements used

Element	Description
DIGITAL CIRCUIT	Dspic 30f4012 microchip
DRIVER CIRCUIT	ISO5500 TI
R_g	10Ω smd 1206
L_{load}	power inductor $6mH$
R_{load}	power resistor 6Ω
L_w, R_w	Nichrome wire 80/20
V_{dc}	DC power supply $30A$ $0-60DC$
Oscilloscope	MSO 4034b $350MhZ$ 4 channels
V	Voltage probe $500MhZ$, $10x$, $3pF$
A	Current probe $120MhZ$, $30A$

4.4.1.1 Wire inductance and resistance estimating

Measuring of inductance is performed by taking several values of voltage across wire at different frequencies (see R_w and L_w at figure 4.14). These voltages are generated by a signal generator v_{gg} sweeping frequencies from 2 to $25MhZ$. R_{int} is the internal resistance of signal generator, while R_s is a known smd resistance whose value is 10Ω.

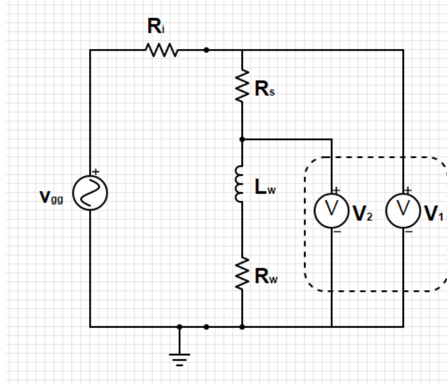


FIGURE 4.14: Circuit diagram to estimate wire inductance.

Procedure followed for measuring inductance is to take waveform of voltage across both known resitance and wire (node 1 in figure 4.14) and voltage across wire only (node 2 at figure). At each frequency, ratio of V_2 and V_1 is computed to calculate gain in dB and also phaseshift between both waves are taken to compute degrees. Only inductance of wire is considered as attenuating of wave V_1 since resistance of wire is much less than known resistance used $(100 - 200m\Omega << 10\Omega)$. In this way, inductance of wire is found by taking frequency at 3 dB of attenuation of V_1 in regards to V_2 and 45 f phaseshift. Inductance is estimated by knowing that frequency at which 3 dB is reached is given by $f = \frac{2(R_w+R_s)\pi}{L_w}$. In figure 4.15 bode diagrams are shown for every wire in which both phase and magnitude diagrams are plotted. In this way, by taking data from figure 4.15, table 4.3 is built. Another column has been added to the inductance value of wire that represents resistance of wire. Also, wire resistance R_w has been measured by 4-wire measurement method of resistance.

TABLE 4.3: Wire parameters measured and estimated

Wire (cm)	$L_w(nH)$	$R_w(\Omega)$
10	63	0.13
15	122	0.19
20	190	0.27

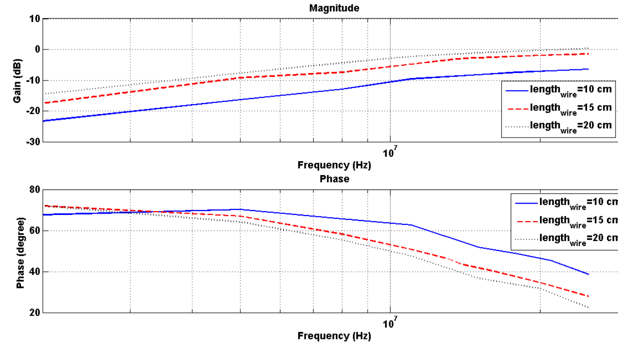


FIGURE 4.15: Bode diagram for each wire.

4.4.2 Experimental procedure

Experiment is performed by following Taguchi's methodology. In this sense, the process diagram depicted in figure 4.16 represents factors, input variables, input signals and outputs required. The procedure followed to obtain $\hat{i_{mes}}$ is similar to the path described in simulation verification (figure 4.7), except that interpolation is no longer needed since oscilloscope signals, and specifically, v_{mes} is obtained constantly sampled. Input signal i_{mes} is obtained by current probe and it is assumed as the pattern in order to obtain $RMSE$. Voltage's probe capacitance C_p is assumed constant and its value $3pF$ as shown in table 4.2 for voltage probe specifications. Next, a description of factors and sample time obtainment is presented.

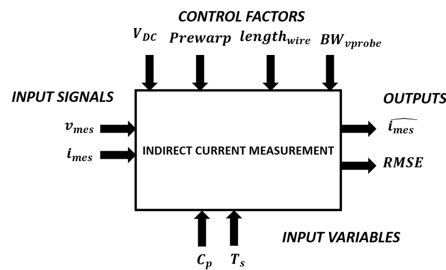


FIGURE 4.16: Diagram process of experiment.

4.4.2.1 Factors definition

Factors that will be analysed during the experiments are shown in table 4.4. Length of wire is the factor F_1, which levels will be represented by the three wires of 10, 15 and 20 cm of length. Factor F_2 will be level of dc bus voltage, taking levels of 20, 30 and 40 volts. Factor F_3 is the limit bandwidth of voltage probe across wire, being limited

and not limited to 20 MhZ and 350 MhZ respectively. Finally, factor F_4 is a variation in discretization method, being prewarped or not prewarped (yes or no).

TABLE 4.4: Levels and factors of experiment

Factor \ Level	1	2	3
$F_1 = Length_{wire}$ (cm)	10	15	20
$F_1 = V_{dc}$ (Volts)	20	30	40
$F_1 = BW_{vprobe}$ (MhZ)	350	20	NA
$F_1 = Prewarp$	yes	no	NA

Seeing at table 4.5, it can be seen that levels and factors take all possible values without repeating any row of L-array. In this way, level 1 of factor F_1 only will be varied along first 3 experiments, none of which will be repeated in the subsequent treatments. In last column, it can be seen that there is a variable that will take values upon each experiment ($RMSE$). This variable can represent variance of data and it shall be used instead of $SN\,ratio$ as a matter of easy for computing. This variable is calculated via equation 4.8 in which $\hat{I_{mesk}}$ represents instant current calculated by method outlined last section and I_{mesk} is the instant effective current measured through the nichrome wire, assuming it accurate enough; and N is the number of points that will be taken at measurement. Both currents are obtained at k instant.

$$RMSE = \sqrt{\frac{\sum(\hat{I_{mesk}} - I_{mesk})^2}{N}} \tag{4.8}$$

TABLE 4.5: L9-array used and arranging of levels of factors

Experiment \ Factor	F_1	F_2	F_3	F_3	$RMSE$
1	1	1	1	1	r_1
2	1	2	2	2	r_2
3	1	3	1	2	r_3
4	2	1	2	1	r_4
5	2	2	1	1	r_5
6	2	3	2	2	r_6
7	3	1	1	2	r_7
8	3	2	2	1	r_8
9	3	3	1	1	r_9

Also, in table 4.6, variance table is expressed by several fractions in each cell. These fractions represent variation of $RMSE$ at every level of every factor. For instance, at

TABLE 4.6: Variance table

Level \ Factor	F_1	F_2	F_3	F_4
1	$\frac{r_1+r_2+r_3}{3}$	$\frac{r_1+r_4+r_7}{3}$	$\frac{r_1+r_3+r_5+r_7+r_9}{5}$	$\frac{r_1+r_4+r_5+r_8+r_9}{5}$
2	$\frac{r_4+r_5+r_6}{3}$	$\frac{r_2+r_5+r_8}{3}$	$\frac{r_2+r_4+r_6+r_8}{4}$	$\frac{r_2+r_3+r_6+r_7}{4}$
3	$\frac{r_7+r_8+r_9}{3}$	$\frac{r_3+r_6+r_9}{3}$	NA	NA

level 1 of factor F_1, only $RMSE$ values of first three rows of table 4.5 are taken since that level is only varied in the three first experiments. In this way remaining fractions are calculated without filling cells of level 3 for F_3 nor F_4 since there is no third level for these factors.

4.4.2.2 Sample time and rise time

Given a record length of oscilloscope of 10000 points at every screen capturing, sample time is obtained by dividing time interval within screen capturing into record length. Time interval will be of $4\mu s$. In this way, sample time is $T_s = 0.4ns$, or equivalently a sample rate of $f_s = 2.5GhZ$ which is good enough to acquire data with minimum aliasing.

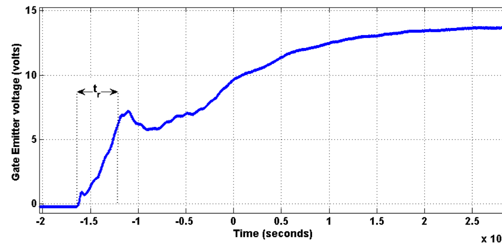


FIGURE 4.17: Gate voltage and time to charge C_{ge}.

In figure 4.17 gate emitter voltage across IGBT1 V_{ge} measured signal is shown for $V_{dc} = 20volts$ and a wire of 10 cm and it is measured by 350 MhZ voltage probe. It is important to note that gate emitter voltage is a good indicative of how fast is current signal and if 120 Mhz current probe is a good pattern to compare results. This is because collector current and gate emitter voltage are almost linear related in active region by IGBT transconductance. In figure the time to charge gate emitter capacitance of IGBT is measured as $t_r = 42ns$. This result compared to rise time of measurement system $t_{rsys} = \frac{0.35}{350MhZ} = 1ns$ and rise time of current probe $t_{rcurrent} = \frac{0.35}{120MhZ} = 3ns$ is slow enough (42 times and 14 times smaller) to consider measuring reliable.

4.4.3 Experimental results

Now, by applying methodology above explained, main results of experiments are shown. L-arrays are filled in accordance to the results collected. For instance, in figure 4.18 waves of current and voltage are shown for full bandwidth of voltage probe, level 1 of factor dc bus voltage 20 volts and the shortest wire (10 cm). These traces are shown when capturing turn on transient of IGBT. As it can be seen there, resolution of voltage probe is good enough to take true variations of voltage across nichrome wire.

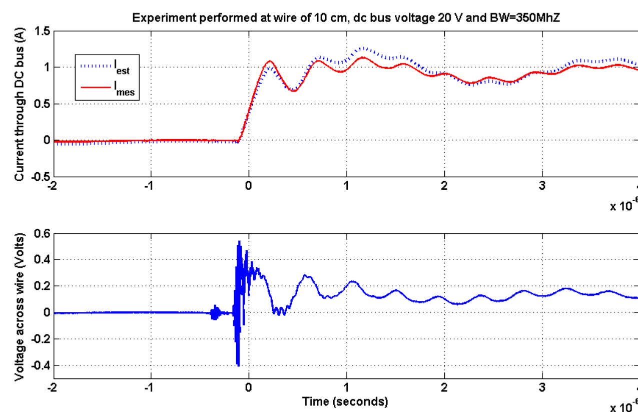


FIGURE 4.18: Current through dc bus measured (red continuous) and calculated (dotted blue) and voltage acrosss measurement wire. V_{dc}=20 volts, $wire_{length}$=10 cm, BW=350 MhZ and no prewarping.

At turn off, and now at maximum level of voltage, waveforms of current are plotted in figure 4.19. It is now seen that estimation of current at long wires (15 and 20 cm) yields large errors at the beginning of turn off transient (about $0.2^{-}6s$ horizontal coordinate in figure). However, at capturing oscillations, waveforms tend to converge for any length of wire used.

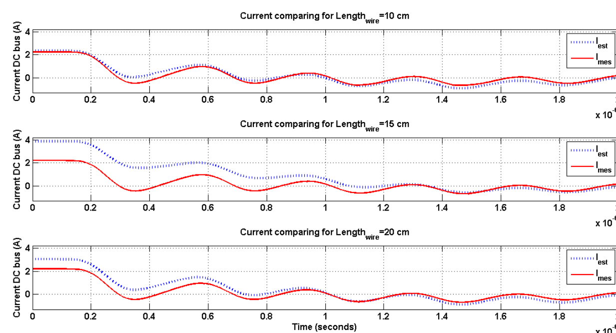


FIGURE 4.19: Current through dc bus measured (red continuous) and calculated (dotted blue) at turn off period. V_{dc}=60 volts, BW=350 MhZ and no prewarping.

After performing every experiment planned by path shown in table 4.5, L-array of experiment is obtained. This can be seen in table 4.7, where $RMSE$ value for each combination of levels of factors is calculated. Something that could be seen there is the great variance of the measurement around true value (assuming true the measure of current by current probe) when wire used is long. In table 4.8 these results could be seen one at a time by looking every column and analysing the influence of each factor on variance.

TABLE 4.7: L-array filled

Experiment \ Factor	F_1	F_2	F_3	F_3	$RMSE$
1	10	20	350	yes	0.051138
2	10	40	20	no	0.069542
3	10	60	350	no	0.091488
4	15	20	20	yes	0.569552
5	15	40	350	yes	0.627591
6	15	60	20	no	0.642212
7	20	20	350	no	0.253192
8	20	40	20	yes	0.531576
9	20	60	350	yes	0.534826

TABLE 4.8: Variance table experiment results

Level \ Factor	F_1	F_2	F_3	F_3
1	0.070722	0.291293	0.311647	0.462936
2	0.613112	0.409567	0.453220	0.264108
3	0.439864	0.422842		

4.5 Conclusions

By the development of these experiments it is seen that current through semiconductor could be measured indirectly by choosing proper wire in series. Given the results, wire must be short enough to avoid side effects not considered such as induced voltages. It is also important to point out the necessity of making inductance small enough in order to avoid a great influence of power losses and switching behaviour as seen in chapter 3, but, as seen in simulation results, resistance value of wire is also important and error becomes greater for short values of ohmic resistance (figures 4.11 and 4.12).

Besides the fact that variance is greatly influenced by length of wire, it is also very important to notice that error gets larger for large values of voltage (see column F_1 at table 4.8). This is confirmed also by seeing at third experiment of table 4.7, where $RMSE$ value is greater than values at low levels of voltage for the same short wire. Also, it is important to notice that resolution (see figure 4.18) of voltage probe is not as contingent as effects of large current and voltages across a wire that could induce and cause undesired effects both on measurement and also on behaviour of circuit. Also, factor F_3 (bandwidth) gives us an indicative information of the importance of having a wide bandwidth of measurement of voltage across wire, regardless of noise induced. Finally, it has been seen, as in latter section, that prewarping is not needed at all, and maybe it might damage the measurement accuracy.

Additionally, stray inductance and resistance could be estimated by the use of this procedure by just using a high frequency voltage probe at low values of dc bus voltage. Furthermore, a characterization of semiconductor could be performed and investigation of factors like those treated in chapter 3 could be carried out by properly using results of this experiment. It is remarkable also, that strict practices of PCB design must help in avoiding side effects of self-inductance of wire and measurement can be dramatically improved.

Chapter 5

Conclusions and future works

It has been seen that turn on losses can be found by the solution of the model developed. This is because parameters, namely, storage time, diode capacitance and conductance and IGBT capacitances could be used with average absolute errors below 30 % for an optimal value of diode capacitance of 1.4 nF. However, these results are up to almost any condition of current, voltage, gate resistance and stray inductance within topology studied. Results show also that estimation of parameters agree with simulation results, getting errors around 10% at estimating diode conductance, and below 10% for storage time. Both as a function of stray inductance. In this way, model fits well and can be used reliably as a good tool for estimating switching behaviour at turn on without the need of long simulation routines, especially when analysing power losses in a specific switching scheme.

This also applies for turn off losses. However in this case, polynomial regression is needed to be performed. It has been seen that switching times vary with current and voltage and it has been backed up with statistical analysis of effects on tail time, and on pre tail time. $p - value$ has been evaluated for each factor. This is especially important when operating a converter within a switching scheme. Either if it is a voltage source converter or a current source converter, variation in time, and consequently its outcomes in calculating turning off power losses can be met by applying the procedure described in this work.

Finally, in chapter 4 a procedure for measurement of current has been carried out. This procedure is intended to measure high frequency current during transient period

of a semiconductor. An IGBT has been used to verify reliability of procedure within a clamped-inductive circuit fed by a constant DC bus. Simulation and experimental results has been shown and they agree with calculation of current by a signal of voltage across a wire of known resistance and inductance. Taguchi's methodology carried out to verify experimentally has shown the most important factors that affect accuracy at measuring current. These factors are bandwidth of voltage probe, voltage magnitude of DC bus, length of wire used and prewarping at discretization method. By right choice of factors, this procedure can be applied to verify results of power losses model carried out in chapter 3.

By the development of this work, remaining results and works to be carried out in future works might include:

- Total power losses model in a specific converter. For this, conduction losses and switching scheme are needed to be taken into account.
- Experimental verification of power losses model in a two level converter of known switching scheme.
- Investigation of non-linearity and dynamics of diode capacitance during reverse recovery process.
- Temperature effect on parameters of differential equations.
- Experimental verification of measurement procedure at high voltages and high currents and validation of model developed by employing this method.

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